Design of the Fam using Modified Booth Recoder in Digital Energy Meter

G. Kohila
PG Scholar, VLSI Design
Sona College of technology
Salem, India

Dr. B. Gopi
Professor and HOD of ECE
Sona College of technology
Salem, India

***Abstract*— Digital signal processing carry out a large number of arithmetic operations. Many of the applications were based on the booth recoder, which is focused on optimizing the design of the FAM. But existing system has the conventional design which performs the product of sum separately. In the FAM operator the design is made by using hybrid adder for increasing the performance. When comparing the existing system with the FAM designs, the proposed technique yields considerable reductions in critical path, complexity in hardware design, area and power consumption. This proposed technique can be used in the field of digital energy meter, which is used to calculate the power consumed with the help of FAM design.**

Keywords*— Fused** *Add-Multiply (FAM); Modified Booth Recoder (MB); Carry Save Adder (CSA); Carry Look Ahead Adder; Digital Signal Processing(DSP);Hybrid Add-multiply(HAM)**

I. INTRODUCTION

Nowadays the hybrid adder multiplier is used in several commercial purposes. There are many pairs of concurrent addition and multiplication instructions in programs, which can be usually executed in parallel. In the past a majority of researches focused on the reduction of the overall latency with respect to the conventional FAM unit and at the same time the accuracy is increased over the traditional implementation. In many digital signal processing (DSP) and multimedia applications, multiplication and addition are the most commonly used operations. Therefore, multiply-add fused unit plays an important role in improving performance by combining multiplication and addition operation into a single unit in the modern embedded processors. The research proposes a hybrid add-multiply (HAM) unit that integrates a multiplier and an adder into a single unit. That is, they built a "bridge" circuits between multiplier and adder for combining the results from multiplier and adder as the final output result of HAM. On the other hand, we propose a new architecture for designing a Digital Energy Meter using Hybrid Adder multiplier unit. This proposed technique can be used in the field of digital energy meter, which is used to calculate the power consumed with the help of FAM

II. SYSTEM IMPLEMENTATION

A. Fused Add-Multiply Implementation

In this paper, we focus on FAM units which implement the operation Z=X.(A+B) . The hybrid design of the FAM operator (Fig. 1(a)) requires that its inputs A and B are first to an adder and then the input X and the sum Y=A+B are driven to a multiplier in order to get Z. In this work, we present a new technique for direct recoding of two numbers in the MB representation of their sum and finally hybrid adders (CSA and CLA) were used. As a result, significant area savings are observed and the critical path delay of the recoding process is reduced, low power can be minimized, and decoupled the inputs from the band width.

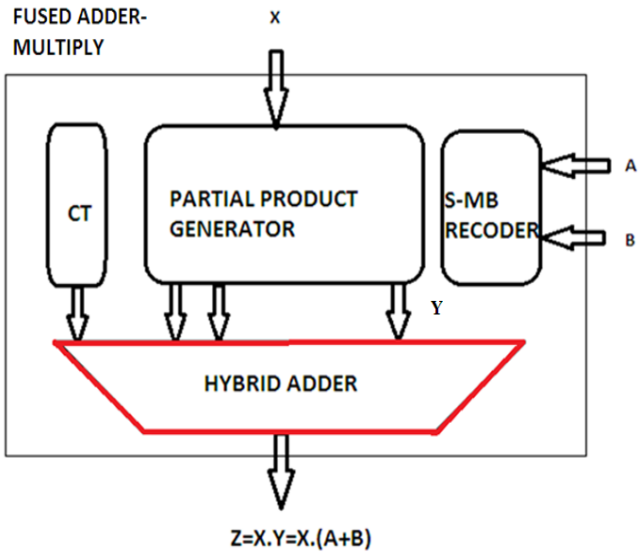

Fig.1. Fused design using hybrid adder

After implementation of FAM techniques, write the Verilog code for FAM method. To analysis power, area reduced, Utilize the power consumption using FAM for simulation purpose and it also used as a tools for execution. Then FPGA is used as the hardware implementation. Therefore the design can be implemented in to an application also that is DIGITAL ENERGY METER.

III. APPLICATION BLOCK OF FAM

A. Digital Energy Meter

The application of the proposed techniques includes digital energy meter. Therefore, digital energy meter which is

used to calculate the power. The power which is equal to the voltage (V) is multiplied with the current (I) ((i.e.) P=(V*I).Therefore the digital energy meter performs the multiplication operation. Here the FAM technique is used for multiplication process. In an application block ((i.e.) digital energy meter), voltage sensors measure AC and/or DC voltage levels. It can receives voltage inputs and produce output as an analog voltage, analog current levels, and switches or audible signals and therefore current sensor is used to detect and converts current to an easily measured output voltage, is proportional when the current in measured path.

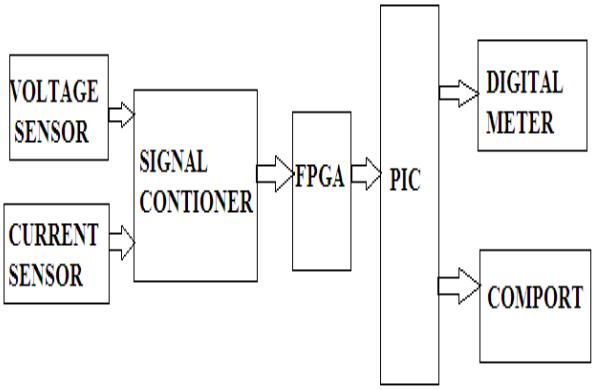

Fig.2. Digital energy meter

Voltage sensor and current sensor which is connected to the signal conditioner. Signal conditioner is used for analog to digital conveter.After converting AC to DC; the DC values are given to FPGA controller. FPGA controller is used to perform the multiplication unit by reading the units measured in Voltage sensor and current sensor and Power units will be increased by adder process. So finally Hybrid Adder Multiplier operation is executed using FPGA controller. FPGA are connected to the PIC controller. The FPGA is given to input of PIC MICROCONTROLLER, where the PIC microcontroller produced output in digital meter and comport. And the output can be displayed in digital meter.

IV. SIMULATION RESULT OF FAM UNIT

We compare the performance proposed recoding schemes is very efficient. And includes each of the recoding schemes in a fused Add-Multiply (FAM) operator (Fig. 1(a)) and implemented them using structural Verilog HDL for FAM unit. Comparing the FAM designs with the existing recoding schemes, the proposed technique yields the reduction interms of critical delay in the system level, hardware complexity and power consumption in FAM unit.

Fig.3. Simulation of FAM unit using hybrid adder. A & B is the input can be recoded in a sum-modified booth algorithm. The output of A & B can be multiply with X partial product can be produced and this partial product can produced the output of Z

B. Power Analysis of FAM Unit

When compared to the existing recoding scheme, power can be reduced in the FAM unit. Therefore the total required in FAM unit is 0.034w

Fig.3. Power analysis report

c. Application Block Simulation Result

1) Current level : The current level of Digital energy meter is 3.2A

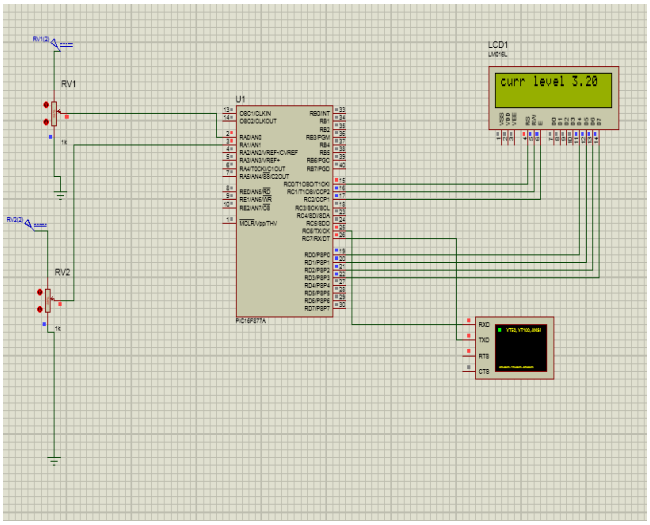

Fig.4. Current level value

2) Voltage level : The voltage level of Digital energy meter is 2.95V

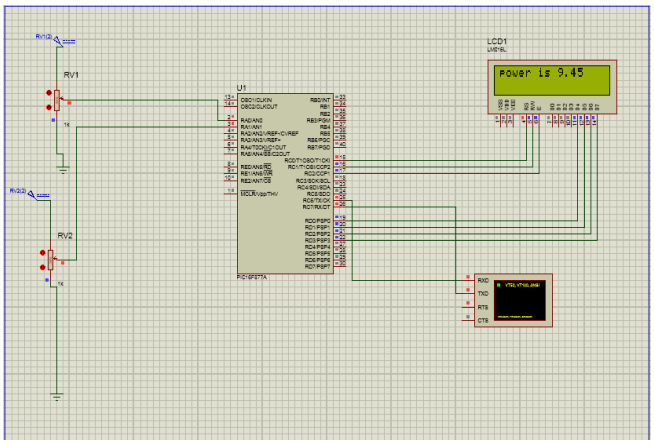

Fig.4.Voltage level value

3) Total Power Level : The total power value of Digital energy meter is 9.45

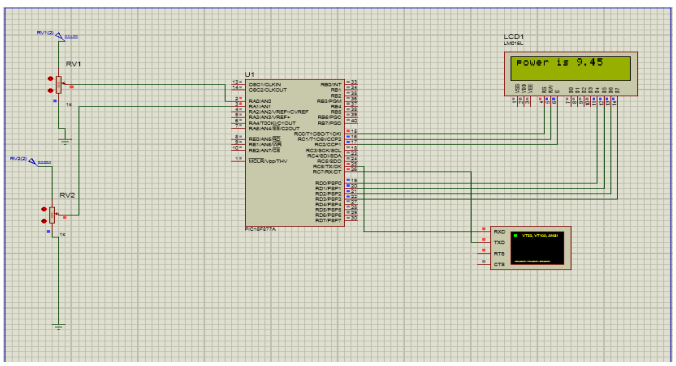

Fig.6. Total Power Value

V. CONCLUSION

This paper focuses on optimizing the design of the Fused-Add Multiply (FAM) operator. We propose a structured technique for the direct recoding of the sum of two numbers to its MB form. The designs of the proposed S-MB recoder and compare them to the existing ones ,the proposed recoding schemes of FAM designs, yield considerable performance improvements in power and area. This proposed technique can be used in the field of digital energy meter, which is used to calculate the power consumed with the help of FAM design.

REFERENCES

[1] A. Amaricai, M. Vladutiu, and O. Boncalo, "Design issues and implementations for floating-point divide-add fused,"IEEE Trans. Circuits Syst. II–Exp. Briefs, vol. 57, no. 4, pp. 295–299, Apr. 2010.

[2] E. E. Swartzlander and H. H. M. Saleh, "FFT implementation with fused floating-point operations," IEEE Trans. Comput.,vol.61,no.2,pp. 284–288, Feb. 2012.

[3] L.-H. Chen, O. T.-C. Chen, T.-Y. Wang, and Y.-C. Ma, "A multiplication-accumulation computation unit with optimized compressors and minimized switching activities," inProc. IEEE Int, Symp. Circuits and Syst., Kobe, Japan, 2005, vol. 6, pp. 6118–6121.

[4] O. Kwon, K. Nowka, and E. E. Swartzlander, "A 16-bit by 16-bit MACdesign using fast 5: 3 compressor cells,"J. VLSI Signal Process. Syst.,vol. 31, no. 2, pp. 77–89, Jun. 2002.

[5] Y.-H. Seo and D.-W. Kim, "A new VLSI architecture of parallelmultiplier–accumulator based on Radix-2 modified Booth algorithm,"IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 18, no. 2, pp.201–208, Feb. 2010.

[6] W.-C. Yeh and C.-W. Jen, "High-speed and low-power split-radixFFT,"IEEE Trans. Signal Process., vol. 51, no. 3, pp. 864–874, Mar.2003.

[7] W.-C. Yeh, "Arithmetic Module Design and its Application to FFT,"Ph.D. dissertation, Dept. Electron.Eng., National Chiao-Tung University, ,Chiao-Tung, 2001.

[8] R. Zimmermann and D. Q. Tran, "Optimized synthesis of sum-of-products," inProc. Asilomar Conf. Signals, Syst. Comput., Pacific Grove,Washington, DC, 2003, pp. 867–872.

[9] M. Daumas and D. W. Matula, "A Booth multiplier accepting both aredundant or a non redundant input with no additional delay," in Proc.IEEE Int. Conf. on Application-Specific Syst., Architectures, and Processors, 2000, pp. 205–214

[10] C. N. Lyu and D. W. Matula, "Redundant binary Booth recoding," in Proc. 12th Symp. Comput. Arithmetic, 1995, pp. 50–57

[11]"An Optimized Modified Booth Recoder for Efficient Design of the Add-Multiply Operator "Kostas Tsoumanis, Student Member, IEEE, Sotiris Xydis, ConstantinosEfstathiou, Nikos Moschopoulos, and KiamalPekmestzi, vol. 61, no. 4, April 2014.