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Design of Successive Approximation Analog to Digital Converter with Modified DAC

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***Abstract*- This paper presents successive approximation analog to digital converter with modification in DAC module, hence it is important to select right architecture. Successive approximation Analog to Digital Converter has been preferred in most of the application because of their compact circuitry as compared with other ADC which makes this SAR ADC inexpensive. It has been observed that power dissipation is high in digital to analog module. Hence modification is proposed in digital to analog (DAC) architecture to achieve excellent power efficiency for a relatively moderate resolution. This SAR ADC is designed in 0.18µm CMOS technology achieves 500 KS/s will be useful for high speed with medium resolution and low power consumption application.**

Keywords: Analog to digital converter, Low power, Resolution, Successive Approximation analog to digital converter.

I. INTRODUCTION

Analog to digital convertor (ADC) and digital to Analog Convertors are important block in many portable systems, Analog-to-Digital Converters (ADC) are required for interfacing analog signals to digital circuits [1]. ADC provides connection between hardware systems and digital signal processing systems. Among different ADC architectures the SAR-ADC gives a common solution for application demanding low power, medium resolution and moderate speed. SAR ADC is known for its simple structure, thus consuming less power and saving more die size [2].

Fig.1 shows Successive Approximation (SAR) is very suitable for resolutions ranging from 8 bits to 16 bits and sampling rates ranging from 50 KHz to 100 MHz [3]. The most effective way to create a Giga rate application with 8 to 16 bit resolution is the pipeline ADC architecture. In the past few years, demand of SAR ADC is increased because most of applications are built with very stringent requirements on power consumption. For electronic devices, such as wireless systems, data acquisition system or mobile devices, one of most important factors is the power dissipation.

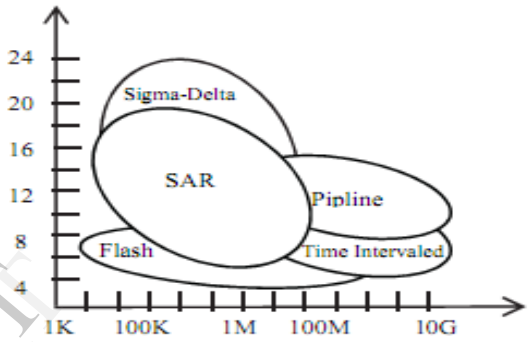


Fig.1 (a) Sampling rate versus bit resolution of different ADC's

Sigma Delta ADC architectures are very useful for lower sampling rate and higher resolution (approximately 12-24 bits). The common applications for Sigma-delta ADC architecture are found in voice band, audio and industrial measurements [4]. The most effective way to create a Giga rate sampling rate with 8 to 16 bit resolution is the pipeline ADC architecture. In the past few years, demand of SAR ADC is increased as numbers of applications are built with very stringent requirements on power consumption. The conventional SAR ADC, as shown in Fig. 1(b), use charge redistribution DAC. Speed of conversion is limited as it requires N-clock cycles to convert N-bits. The bulky binary weighted capacitor arrays employed in fig.1 architectures require large silicon area.

Recently presented ADC in [1] has Low power Successive Approximation ADC for MAV'S. Here MAV's is a Micro Air Vehicle system. In the proposed low power low voltage Novel SAR ADC architecture (LFSR logic), the charge distribution based DAC has been replaced instead of segmented current steering DAC approach to minimize the area, power consumption and improves the speed of the design

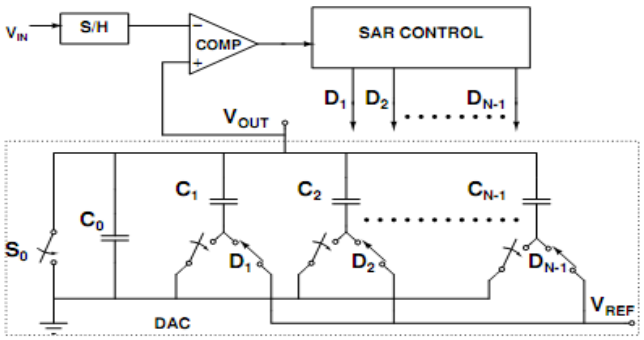


Fig. 1 (b) Conventional SAR ADC

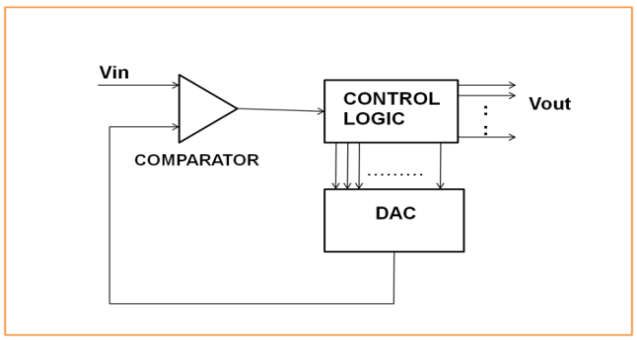


Fig. 1(c) Proposed block diagram for SAR ADC

The ADC presented in [2] use in Ultra Wide Band(UWB) radio technology. In this ADC, there is use of split capacitor array DAC which is used for increasing the speed and reduces the switching energy.

The ADC presented in [3] designed for low-power, medium-quality applications such as data acquisition system. The DAC required in the ADC design is based on R-2R ladder. Although only one op-amp is actually required, two op-amps are used so that one of the output can be used for measuring the performance of the DAC. Fig. 3 shows the block diagram of proposed SAR ADC which achieves 10 bit resolution.

Comparator used in proposed ADC is 2 bit comparator in which one of the input is output of modified DAC module and other is analog input Vin which is already sampled through sample and hold circuit. The output of comparator which is digital signal is given to control logic circuit where SAR logic is present.

In SAR ADCs, the primary sources of power dissipation are the digital control circuit, comparator and capacitive reference DAC network. Power consumption becomes lower with the advancement of technology. Technology scaling also improves the speed of digital circuits. Hence to achieve minimum power consumption in ADC, power dissipation in DAC network should be reduced. So in order to achieve low power dissipation modification is proposed in DAC network.

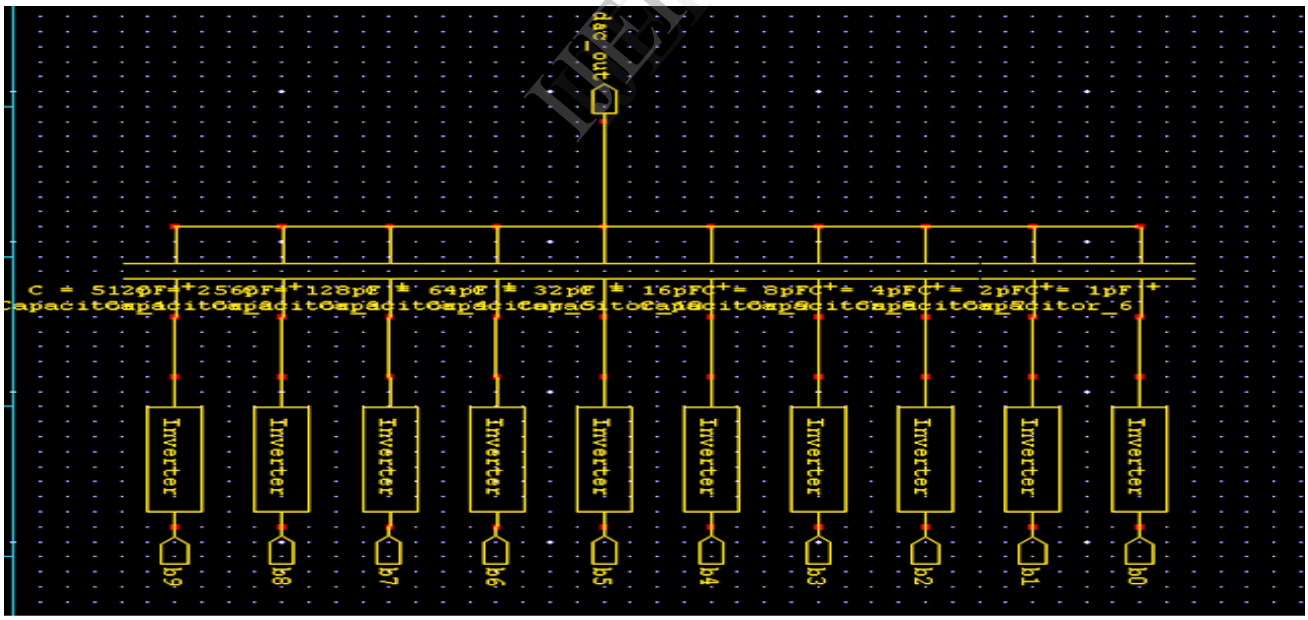


Fig.2 (a) Architecture of proposed minimum capacitor method for DAC

II. PROPOSED DAC ARCHITECTURE

The proposed DAC architecture schematic is as shown in fig. 2(a).This architecture has been derived on the basis of DAC split capacitor switching technique.

DAC architecture uses ten capacitors and ten inverters are connected in series with each other. The key idea of the proposed DAC module is to use minimum capacitor so as to minimize power consumption in DAC architecture which

ultimately results overall low power consumption for SAR ADC.

Converting a signal from digital to analog can degrade the signal. Therefore details are chosen so that errors are negligible.DAC with capacitor arrays are widely used in SAR ADC designs. Compared to the conventional voltage driven R-2R techniques, the capacitor arrays are more easily fabricated with less mismatch errors and save more power based on charge-redistribution techniques [6]. Fig. 2(b) shows a binary-weighted capacitor (BWC) array, the operation of the circuit has two modes.

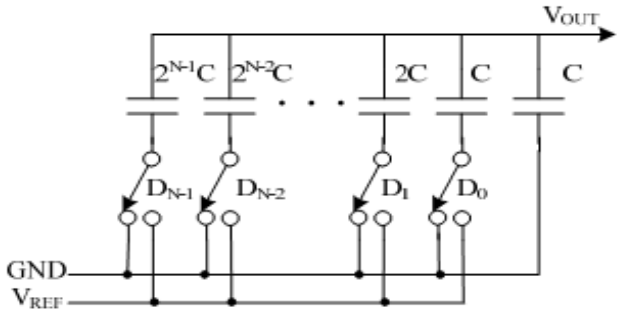


Fig. 2(b) Binary-weighted capacitor array

During the reset mode, all the switches are connected to ground, allowing the bottom plate of the capacitor arrays to discharge. During the conversion mode, the digital codes determine which switches change connection from ground to VREF. The charge redistributes through the conversion period. Since the total capacitance of this array rises exponentially with the increase of the resolution, the accuracy of the BWC DAC is limited to 8 to 10 bits.

Digital to analog convertor has been simulated in 0.18µm CMOS technology with minimum capacitor technique. Fig. 2 (c) shows the simulation and FFT of digital to analog converter. The output of the simulation is analog signal converting from digital signal. The proposed DAC module is designed with minimum capacitor technique and it consumes very less power.

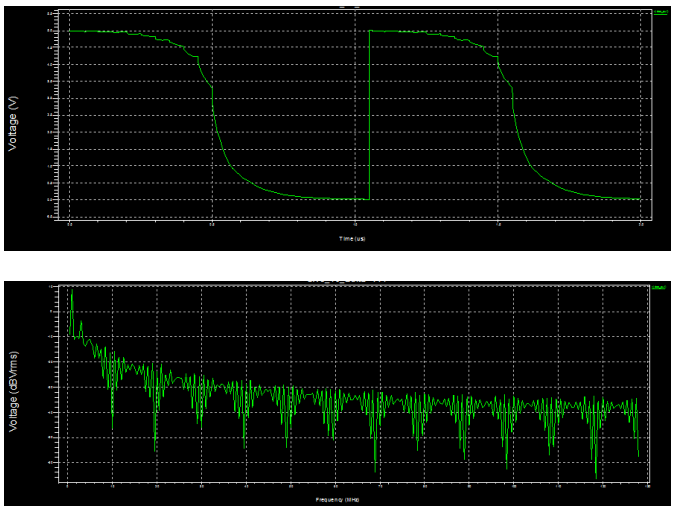


Fig.2 (c) Simulation and FFT of Digital to Analog converter

III. COMPARATOR

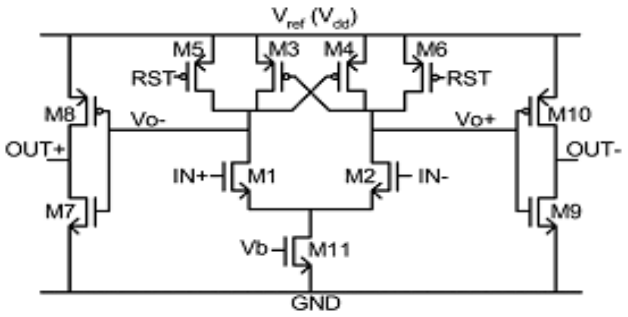


Fig. 3(a) Schematic of the comparator

The schematic of comparator circuit shown in Fig. 3(a) is based on a paper presented by Peluso et al. [11]. During the reset phase (RST low), nodes +Vo and -Vo are forced to Vdd by M5 and M6. When RST goes high, due to the differential input voltage comparison operation is started and +Vo and –Vo slew toward ground at unequal rates. Latch the comparator when nodes +Vo and -Vo are low enough, the pMOS positive feedback load devices M3 and M4 activate.

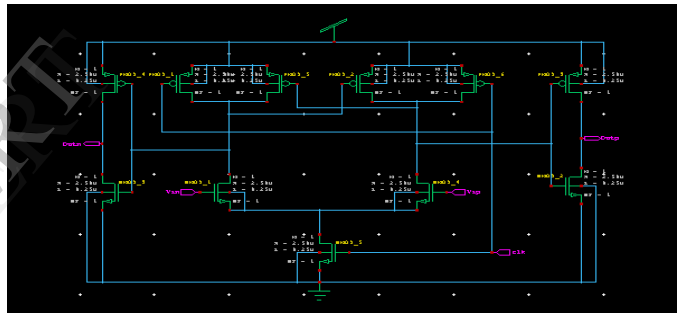
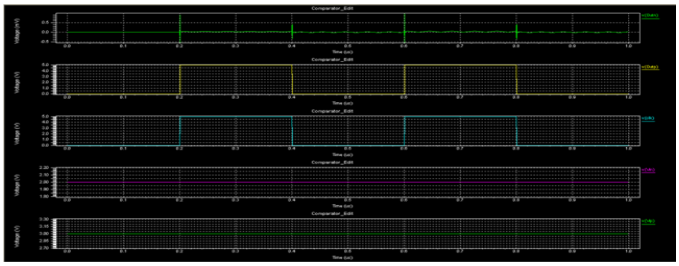


Fig. 3(b) Design of comparator circuit

The bias current in M11 is the critical design variable for the comparator. Noise, speed and power consumption of the comparator circuit are determined by this current value. There is always a tradeoff between selecting a small bias current value for low power dissipation and a larger value to minimize noise and maximize the comparison speed. By referring noise and a comparison time of about 100 ns, the designed value of 1µA for the tail current results in approximately 0.05 LSB of input. For this current, comparator noise does not limit the ADC resolution, and speed is more than sufficient for a 10-kHz sampling rate. The comparator designed is 2 bit comparator comparing two signals. In the simulation result two signals Vp and Vn is faded in the input. The output is high at the active clock pulse if Vp is greater than Vn.



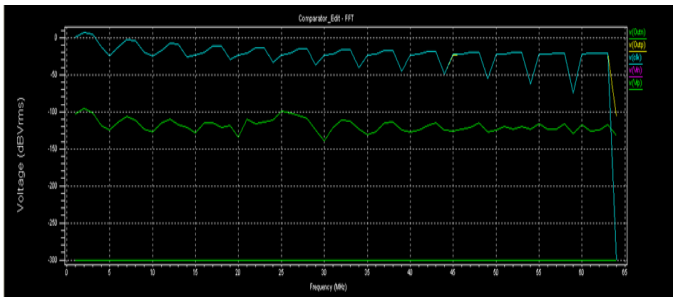


Fig. 3(c) Simulation output and FFT of comparator

IV. SIMULATION RESULTS

Analog to digital converter has been simulated in 0.18 µm CMOS technology with minimum capacitor technique. Fig. 4(a) shows the simulation of analog to digital converter. The output of the simulation is digital signal converting from analog signal. Performance of proposed ADC is evaluated on the basis of total power dissipation which is 691.98 nW achieves sampling rate 500 KS/s. Performance of ADC is summarized in TABLE I.

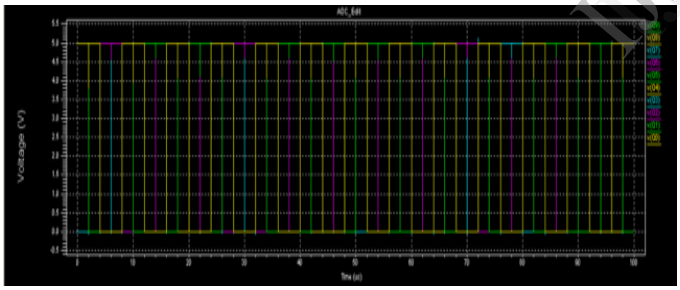


Fig. 4(a) Simulated Digital Analog converter

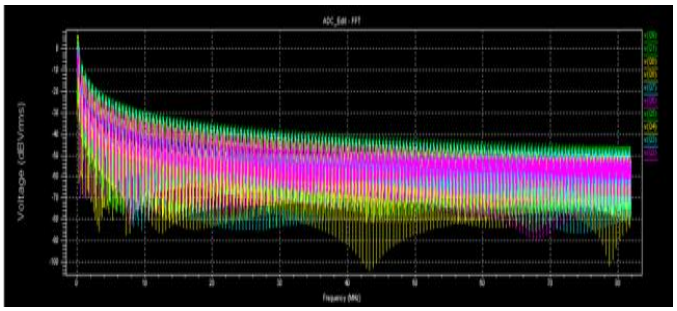


Fig. 4(b) Measured FFT spectrum of digital to analog converter

Fig. 4 (a) (b) shows the simulation result and FFT spectrum of the digital to analog converter. Simulation result is digital signal converted from analog signal.

TABLE I SPECIFICATION SUMMARY

Specification	**Proposed work**
Architecture	SAR
Resolution	10 Bit
Power Supply	0.6 V
CMOS Technology	0.18µm
Total Power Dissipation	691 nW
Sampling Rate	500 KS/s

TABLE II PERFORMANCE COMPARISON

Specification	**[12]**	**Proposed work**
Architecture	SAR	SAR
Resolution	10 Bit	10 Bit
Power Supply	0.6 V	0.6 V
CMOS Technology	0.18µm	0.18µm
Total Power Dissipation	1.04 µW	691 nW
Sampling Rate	200 KS/s	500 KS/s

V. CONCLUSION

In this paper we proposed an efficient capacitor switching technique for DAC module in SAR ADC. The proposed switching technique leads to both lower switching energy and smaller total capacitance. DAC module is designed with minimum capacitor technique in which inverter is connected with capacitor. In future, SAR ADC using minimum capacitor technique for DAC will be energy efficient and cost effective. Proposed SAR ADC achieves a 500 KS/s operation speed with power consumption of less than 1 µW. It consumes power of 691 nW which reduces power dissipation by 33.56% and improves sampling rate by 2.5 times as compared to reference [7].

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