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Design of SRAM and DRAM Volatile Memories using 45nm Technology for FPGA Architecture

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***Abstract*—The VLSI design of volatile memories SRAM and DRAM has been carried out with 180nm and 45nm CMOS technology for FPGA architecture. The design of the schematics and layout has been carried out using Cadence CAD-Tools. The simulation results of the memory design showing timing analysis and attributes are examined. The power and delay time estimated for the two cases are compared. The results of the VLSI design of the SRAM and DRAM memories show significant reduction in power and delay time for the 45 nm technology compared to 180 nm technology**

Keywords— SRAM, DRAM, Volatile Memory, FPGA Architecture, CMOS technology

I. INTRODUCTION

Memory devices are basically classified as primary memory and secondary memory. Primary memory holds the data and instructions on which the device is currently working and is also called as main memory. It has limited capacity, high speed but the data is lost when power is switched off i.e. they are volatile in nature (i.e. RAM, ROM). It is considered as the working memory of the device as it is impossible for the device to work without the primary memory. While secondary memory is used to store data/information permanently and is known as external memory. It offers high memory capacity per area, data is stored even if power is switched off but is slower than primary memory (i.e. flash memory).

II. VOLATILE MEMORY

First, Volatile memory is a memory that requires power to maintain the stored information. The memory holds the data only when the device is powered and it loses the data when the power is switched off. Most RAM (random access memory) used for primary storage is volatile memory. Volatile memory has several uses, in addition to usually being faster volatility protect sensitive information, which becomes unavailable on power-down.

Volatile memory is computer memory that requires power to maintain the stored information. Most modern semiconductor volatile memory is either Static RAM (SRAM) or Dynamic RAM. (DRAM) retains its contents as long as the power is connected and is easy to interface to but uses six transistors per bit. Dynamic RAM is more complicated to interface to and control and needs regular refresh cycles to prevent its contents being lost. However, DRAM uses only one transistor and a capacitor per bit, allowing it to reach much higher densities and, with more bits on a memory chip, be much cheaper per bit. SRAM is not worthwhile for desktop system memory, where DRAM dominates, but is used for their cache memories. SRAM is common place in small embedded systems, which might only need tens of kilobytes or less. Forthcoming volatile memory technologies that hope to replace or compete with SRAM and DRAM include Z-RAM, TTRAM, A-RAM and ETARAM.A detailed comparison of the attributes of volatile memories SRAM and DRAM is given in table 1.

Memories are important in the design of electronics for storage and retrieve of data. Random Access Memory is of two types Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM). SRAM is static in nature and faster compared to DRAM. Static Random Access Memory (SRAM) is one of the most important memory technologies. They are fast, robust, and manufactured in standard logic processes commonly used for microcontrollers and microprocessors. SRAM consume less power and more transistors per bit of memory. Continuous attention is paid to the design of low power and high performance memories. SRAMs are used extensively in modern processors as on chip memories due to their large storage density and small access latency[5, 6].

TABLE I: ATTRIBUTES OF VOLATILE MEMORY

	SRAM	**DRAM**
Non Volatility	No	No
Cell Size (F)	50-80	6-8
Read time (ns)	1-100	30
Write time (ns)	1-100	50
Endurance	10	10
Write power	Low	Low
Other power consumption	MOS sub-threshold leak	Refresh current

DRAMs are dynamic in nature and slower compared to SRAM. DRAM consume more power and require less transistor per bit of memory DRAM memory cell is used for read and write operation for single bit storage for circuits. A single DRAM cell is capable of storing 1 bit data in the capacitor in the form of charge. Charge of the capacitor decreases with time .Hence refresh signals are used to refresh the data in the capacitor. When a read signal reads the data it refreshes it as well. Many different cell designs exist for modern day DRAM cell. These designs are differentiated by the number of transistors used in their designing. As the number of transistors increase, power dissipation also increases. The charge stored in memory cell is time dependent. For high density memories DRAM cell with low power consumption and less area are preferred. DRAM is most

common and cost efficient random access memory used as main memory for workstations[5].

CMOS devices have been scaled down over a period of time to achieve higher speed, performance and lower power consumption. As the integration density of transistors increases, power consumption has become a major concern in today's processors. Low power on-chip memories have become the topic of substantial research as they can account for almost half of total CPU dissipation, even for extremely power-efficient designs. However, static power dissipation is becoming an significant fraction of the total power. The absolute and the relative contribution of leakage power to the total system power is expected to further increase in future technologies because of the exponential increase in leakage currents with technology scaling[4].

III. 180NM AND 45NM TECHNOLOGY

There has been a continuous scaling trend of semiconductor devices in order to keep pace with Moore's law and this seems to an end. This is due to various design pitfalls like short channel effects (SCE) and variations in process design parameters leading to high leakage currents. The design of low power circuits, battery operated and portable electronic systems has become a challenge for the VLSI circuit designers with scaling trends. The recent venture by Intel in silicon material processes technology, in the manufacture of 45nm Metal Oxide semiconductor Effect Transistor (MOSFET) has extended Moore's Law for some more years. Circuit designing using MOSFETs at deep sub micron levels, needs a careful study of the behavior of channel length leading to high leakage currents and poor performance of devices. The possibility of scaling down of transistors further has been achieved by replacement of silicon oxide with high-k dielectric gate material by Intel in 45nm devices. Detailed comparisons of the attributes of various CMOS technologies are summarized in table 2.

IV. PES AND FPGA

Programmable Elements (PEs) in an FPGA comprise a significant portion of the overall FPGA area and are used to configure its functionality. The PE contains RAM memory cells and can be programmed to realize any function of multiple variables. The two core components of an FPGA which depend on PEs are the logical elements (LEs) and the routing switches that connect the logic elements together. The functions are stored in the truth table form in LUT (Look Up Table) which is known as LE. The speed, power, area, and functionality of these components will depend on PE used. The memory is located in the PE, controls the LE through programmable interconnects programmable interconnects[2].

It is PEs in which the memory elements like SRAM or DRAM can be placed for programming. Memories play a vital role reflecting the central concepts and performance characteristics of FPGA. Volatile memories placed in PEs are used for data configuration. Figure 1 shows how two logical elements can be connected together using a switch that is controlled by a PE

The paper presents VLSI design of SRAM and DRAM memory circuits and makes a comparative study of 45nm and 180nm CMOS transistors with respect to reduction in power and delay time. The simulations studies have been carried out using Virtuoso Cadence Spectre Simulator.

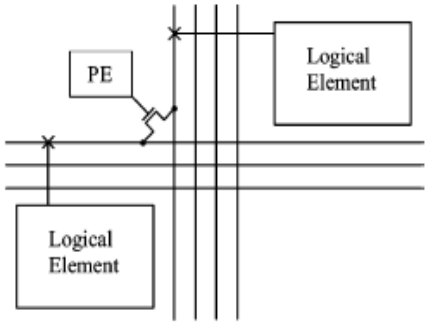

Fig 1: Programmable Elements in FPGA

V. VLSI DESIGN FLOW

A single Cadence design Systems is electronic design automation software and engineering Services Company that offers various types of design and verification tasks which includes Virtuoso Platform which is a Tool for designing full-custom integrated circuits, that includes schematic entry, behavioral modeling (Verilog-AMS), circuit simulation, full custom layout, physical verification, extraction and back-annotation. Used mainly for analog, mixed-signal, RF, and standard-cell designs[3]. The proposed work is done in Virtuoso platform using gpdk180nm and then using gpdk45 nm technology. The flow of design is as shown in figure 2.

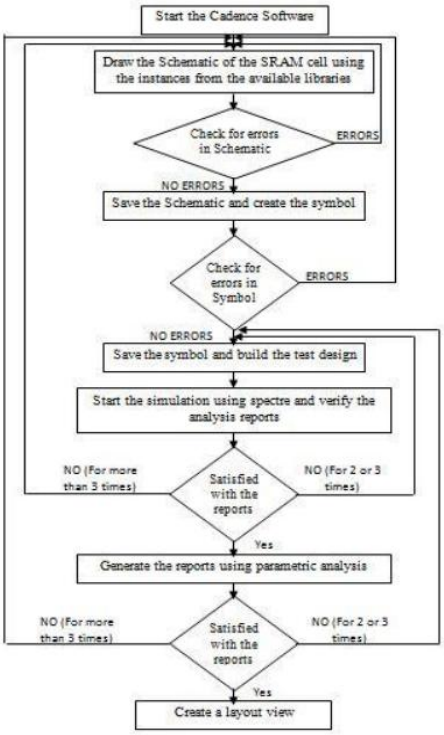

Fig 2: VLSI design flow chart

A. SRAM Circuit design for 45nm Technology

Single bit storage SRAM cell is designed first by schematic design then symbol is created for it is tested using the test design. In test design the simulations are carried out for the circuit.

TABLE II: ATTRIBUTES OF VARIOUS CMOS TECHNOLOGIES

Technology	180nm	130nm	90nm	65nm	45nm	32nm	22nm
Characteristics							
Feature size (microns)	0.25	0.18	0.15	0.12	0.10	0.9	0.8
Gates per chip(millions)	2	5	10	15	20	25	30
Gate length	130nm	90nm	53nm	32nm	22nm	16nm	11nm
Gate material	poly sio2	poly sio2	poly sio2	polysiON	Metal High K	Metal High K	Metal High K
Gate atoms	10	8	6 - 7	5	5 - 10	5 - 10	5 - 10
levels of interconnect	5	5 to 6	5 - 6	6	6 - 7	7	7-8
power supply	1.8	1.2	1.1	0.9	0.8	0.7	0.6
Memory point (μ^2)	4.5	2.4	1.3	0.6	0.3	0.15	0.08

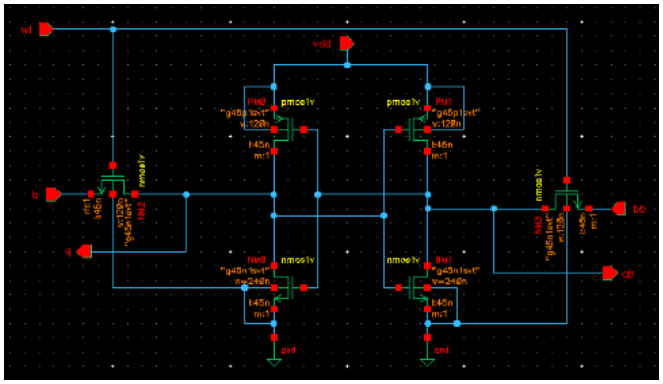

Fig 3: SRAM Schematic design

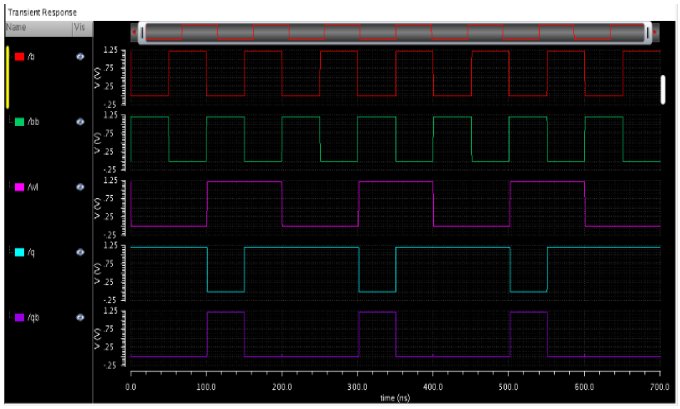

Fig 4: Timing analysis of SRAM circuits

Operational Characteristics

The SRAM core circuit is shown in figure 3. The value is stored in the middle four transistors, which form a pair of inverters connected in a loop. The other two transistors control access to the memory cell by the bit lines. When select (word line) is zero, the inverters reinforce each other to store the value. A read or write is performed when the cell is selected.

To read, bit and bit' are precharged to VDD before the select line is allowed to go high. One of the cell's inverter will have its output at high, and the other at low, which inverter is high depends on the value stored. If, for example, the right-hand inverter's output is low, the bit' line will be drained to VSS through that inverter's pull down and the bit line will remain high. If the opposite value is stored in the cell, the bit line will be pulled low while bit' remains high.

To write the bit and bit' lines are set to the desired values, and then select is set to high. Charge sharing forces the inverters to switch values, if necessary, to store the desired value. The bit lines have much higher capacitance than the inverters, so the charge on the bit lines is enough to overwhelm the inverter pair and cause it to flip state.

The wave forms generated at bit, bit', word line and outputs are shown in figure 4. It is seen from the figure that when word line is high it follows the bit line. If the word line is low the output is zero. For the designed SRAM circuit on 45 nm Technology, the Power, Delay and area are estimated. The power dissipation is found to be ~ 129nW and the Delay time ~ 40ns

B. DRAM Circuit design for 45nm Technology

Using the flow design in cadence virtuoso schematic tool, the DRAM 1 transistor and 1 capacitor design was done. Figure 5 shows the schematic for 1T DRAM using cadence virtuoso schematic editor. After the schematic the test bench was done using the symbol created by schematic and the analysis was done in various aspects.

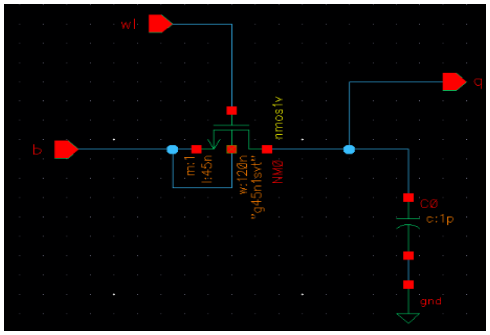

Fig 5: DRAM Schematic design

Operational Characteristics

Figure 5 shows the circuit diagram of a one-transistor DRAM core cell. The cell has two external connections: a bit line and a word line. The value is stored on a capacitor guarded by a single transistor. Setting the word line high connects the capacitor to the bit line.

To write a new value, the bit line is set accordingly and the capacitor is forced to the proper value. When reading the value, the bit line is first precharged before the word line is activated. If the storage capacitor is discharged, then charge will flow from the bit line to the capacitor, lowering the voltage on the bit line.

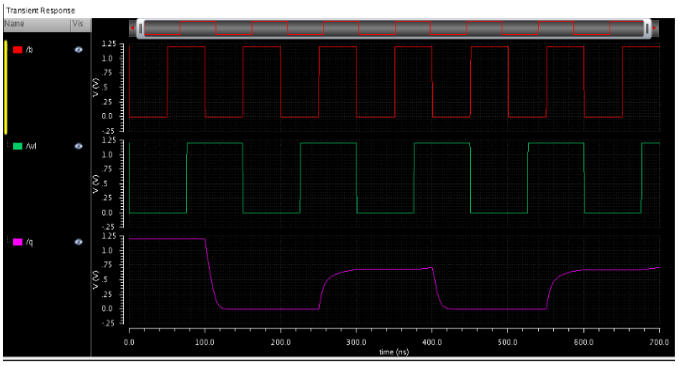

Fig 6: Timing analysis of DRAM circuits

The wave forms for bit line, wordline and output are shown in figure 6. It is seen from the figure that when word line and bit line are high the capacitor charges and gives an high output while with low bit line the output becomes zero. When word line is low the present and the previous output remains same.

For the designed DRAM circuit on 45 nm Technology, the Power and Delay are estimated. The power dissipation is found to be ~ 3.073µW and the Time Delay ~ 30.66ns

VI. Results and Discussions

A detailed comparison between the SRAM and DRAM designed for the two 180nm and 45nm technology is made in table 3. The results of the performance shows that for SRAM there is an reduction in power from 325µW to 130nW which is ~ 4 x 10^{-2} times lower for the 45 nm technology . The delay time for the SRAM shows a reduction from 120ns to 40 ns which is ~3 times lower for the 45 nm technology. Similarly the results of the performance show that for DRAM there is a reduction in power from 13µW to 3µW which is ~ 0.23 times lower for 45 nm technology. The delay time for DRAM shows a reduction from 50ns to 30 ns which is ~0.6 times lower for the 45 nm technology.

TABLE III: Comparision of 180nm and 45nm Technology for SRAM and DRAM circuits

	SRAM		DRAM	
Parameter	180nm	45nm	180nm	45nm
Power	325µW	130nW	13µW	3µW
Delay	120ns	40ns	50ns	30ns

VII. Conclusion

From the timing analysis of the simulation carried out in the paper the following conclusions can be drawn:

a) The VLSI design of SRAM shows that there is a significant power reduction of ~ 4X10^{-2} times for the 45 nm technology compared to 180 nm technology

b) The VLSI design of SRAM shows that in the delay time there is a significant reduction of ~3 times for the 45 nm technology compared to 180 nm technology Selection

c) The VLSI design of DRAM shows that there is a significant power reduciton of ~ 0.23 times for the 45 nm technology compared to 180 nm technology

d) The VLSI design of DRAM shows that the delay time is significantly reduced by ~ 0.6 times for the 45 nm technology compared to 180 nm technology.

e) By designing the PE element using 45nm technology the FPGA configuration time decreases and speed up overall FPGA process.

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