Design of Sliding Window Spatial Filtering System based on FPGA for Impulse Noise Suppression Meeting the Real Time Requirements

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Abstract—Aiming at the one of the most habitual issue of effective denoising production and rapid operating expedition in the processing of digital image noise reduction process for the requirement of real time results to provide high quality image as it has been using in major applications this method was proposed. Sliding window spatial filter known as median filter is a robust method to abolish the impulse noise from an acquired image but it is computationally intensive operation and it is hard to implement the real time. To prevail over, FPGA approach is proposed for easy implementation, optimization of speed, area, power and furnishes support in technical discipline of noise trimming in image to meet high real time requirements. According to the characteristics of structures and design of FPGA, for simulation Xilinx Software and verilog language is used for coding purpose.

Keywords— FPGA, Median Filter, Image Processing, Verilog, Real Time Filtering, Impulse noise, Xilinx.

I. INTRODUCTION

Regarding complex aspects of an image deploying algorithms to enhance the peculiarity of an image as it is effectively used in real time applications.[1] The crucial problem lifted in this is impulse noise when image is wicked. Predominantly in digital image processing, two types of filtering systems are used in digital image processing: spatial domain and frequency domain, spatial domain is stand on direct exploit of pixels where as frequency domain is to modifying the Fourier transform of the image.[2]. A popular technique to negotiate impulse noise is by using non linear filters because non linear filters cannot thoroughly eliminate impulse noise whereas digital execution of linear filter can be bulky and slow when compared to linear filters [3].so median filter is a nonlinear filter which works in spatial domain was introduced by Tukey in 1971[4] has been using in many applications in image processing. Aiming at the abolishing fixed value impulse noise from corrupted image filters are opted corresponding to their noise pattern. By examine and comparison of different filtering discussed in algorithms are previously quite a few literatures and number of different algorithms are put facilitated [5].But it is hard to implement in hardware for real time applications. So, to prevail over, FPGA approach is proposed for easy implementation, optimization of speed, area, power and yield technical support to suppress the noise in the image with high real time requirements

II. MEDIAN FILTER

SMF is a rank selection filter [4] which venture to eradicate noise spike by value of center pixel luminance of filtering window with median. Filtering images S={s(i,j)} from SMF can be described as below calculation.

\[ S(i,j) = \text{median}(k, l) \in W_m,n[D(i+k,j+l)] \]

Where \( W_m,n \) is a sliding window of size \( m \times n \) pixels centered at coordinates \((i, j)\) and \( ns=m \times n \) samples.

To arrange samples in ascending or descending in sorting algorithm such as quick sort or bubble sort are used normally where \( n \) is large. The median value of \( N \times N \) is find out by using \( 3/8(n^2-1) \) comparison operations which to be performed in conventional algorithm. If the comparison number will extend, then the data processing operations is not quick in FPGA. so, merged insertion sort is preferred and number of comparisons were minimized in sort algorithms insertion sort is faster than others. we can amplify the compare number by instanting the insertion sort units.

III. ALGORITHM FOR INSERTION SORT

LA is linear array with ‘N’ elements and ‘K’ is a positive integer. Such that \( K \leq N \), this algorithm in to the \( k^{th} \) positive in LA.

1. [Initialize counter] set \( J=N \)
2. Repeat step 3 and 4 while \( J\geq K \).
4. [Decrease counter] set \( J=J-1 \)
5. [Insert element] set \( LA[K]=ITEM \)
6. [Reset N] set \( N=N+1 \)
7. Exit.
IV. HARDWARE ARCHITECTURE

In the hardware implementation it is consisting FPGA chip, RAM, sliding window, noise detection filtering, UART, control unit, PC.

A. RAM

Misplacement of image data may occurred when image data is directly processed due to the unevenness of reading and writing time. To buffer the data between SDRAM and FPGA, FIFO is placed which is asynchronous. To contrive cached data, FIFO is adapt to deployed on pipeline structure of ping pong operation. For subsequent supply of display data to acquire the 8 bit image data succeeding sliding window concurrently, a dual port like read port and write port is emulated is SDRAM. Write port is used for the purpose of collecting the image data, whereas for VGA display read port is placed with formerly mitigate information of image commensurate with admissible timing signal by casting a accomplished frame buffer.

B. SLIDING WINDOW MATRIX MODULE GENERATION

In system module, in the stimulation of pipeline processing algorithm, it is compulsory to assure that 25 pixel values in the window to be attain simultaneously. To design the hardware of 5×5 sampling window, there is a need of 4 shift registers and 25 registers.

C. UART

UART stands for universal asynchronous transmitter receiver which converts parallel data to serial data. UART sequentially transmits bytes of data, one bit at a time from source and receive the byte of data by at the destination by decoding the sequential data with control bit. As the entire process needs no clock input source hence it is designated as asynchronous communication. Its transmission speed is measured by baud rate.

D. CONTROL UNIT

To have higher implementation speed with good performance control unit is used to control of data transfer between input and output.

5. EXPERIMENTAL RESULTS

In this paper, Verilog source code has been used and it has been simulated in Xilinx software. By this proposed method enhanced results has been achieved. In the figures attached below views the experimental results and final image results shown.
6. CONCLUSION

By comparing the past test results, this paper minimizes the area and optimizes power, speed. It furnishes the hardware support and trims the noise as per the real-time requirements.

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REFERENCES


