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Design of Shift Registers using SEU-tolerant Isolated-DICE latch

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***Abstract* --- Latch is a circuit which retains whatever output state results from a momentary input signal until reset by another signal. Soft errors that occur in the latch circuit may result in the corruption of data stored in it, inorder to overcome from soft errors several methods are pre-proposed. In this paper Serial-In-Serial-Out (SISO), Serial-In-Parallel-Out (SIPO) Parallel-In-Serial-Out (PISO), Parallel-In-Parallel-Out (PIPO) shift registers are designed using the SEU-tolerant Isolated-DICE latch which shows the designed registers have low power and delay characteristics than the Serial-In-Serial-Out (SISO), Serial-In-Parallel-Out (SIPO), Parallel-In-Serial-Out (PISO), Parallel-In-Parallel-Out (PIPO) shift registers of conventional latch circuit. The simulations had been done in Cadence Virtuoso using 90nm technology and 45nm technology. Comparison had been done between existing SISO, SIPO, PISO, PIPO shift registers and designed SISO, SIPO, PISO, PIPO shift registers under 45nm and 90nm technologies and results are tabulated.**

Keywords----Soft error, Single event upset, Isolate-DICE, latch

I. INTRODUCTION

As advancement in the integration of MOS technology in IC's is growing rapidly the digital circuits are becoming much more susceptible to noise due to reduced supply voltage and increase in the transistor density. Alpha particles and cosmic rays are the sources that are responsible for soft errors [2-7] that occur in the circuit of an VLSI environment. The development in the nano-scale technology results in increased circuit density along with improved performance and reduced cost. However the reduction in transistor size and power supply voltage cause the parasitic capacitance at internal nodes of the circuit to decrease which results in the critical charge reduction (The minimum charge that is required for maintaining the correct logic state is called critical charge). Consequently, instantaneous voltage transient error occurs as the cosmic rays or low- energy alpha particles cause interference in circuit internal nodes as the reliability of circuits against soft errors gets lower. Soft errors are classified into two types according to the different locations they occur:
(1) Single event transients (SETs) occurs in combinational circuits
(2) Single event upsets (SEUs) occurs when the logic state of circuits changes undesirably in the storage elements such as latches or register nodes. WOV (Windows of Vulnerability) of sequential circuits is more than the combinational circuit, so combinational circuits are usually less susceptible to particle strikes than sequential circuits. In this paper a robust register design is presented that performs both superior soft-error resistant capability and lower power and delay. The design is made using the previously existing new method called Isolated-DICE technique because of its advantages of simplicity. This isolating technique is capable of masking soft errors in between the circuit internal and external nodes. It is also capable of masking SEU by cross-coupled inter-latching and isolation concept of containing more number of storage points

In a memory cell, a soft error changes logic state or a data value. A soft error does not damage the system's hardware. It only causes damage to the data that is being present at a particular point.
There are two types of soft errors
Chip-level soft error – These errors occurs as radioactive atoms in the chip's material decays and alpha particles are released into the chip. As the alpha particle consists of a kinetic energy and positive charge, the particle can hit a memory node and cause the node to change its logic state to a different value.
System-level soft error - These errors occur when the noise phenomenon hits the data that is stored is being processed. The wrong data bit can even be saved in memory and cause problems at a later time due to this soft error

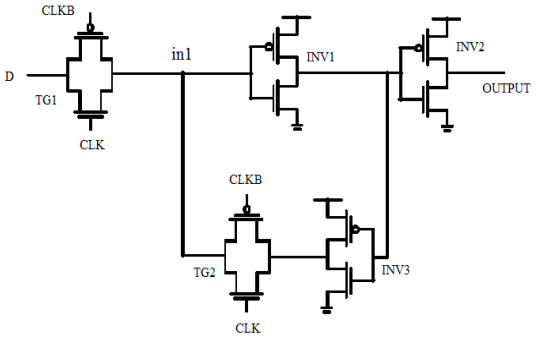

Fig. 1. Conventional latch

Fig. 1 shown above is a conventional latch which stores the logic value using the feedback path. The feed forward signal transmission path consists of two inverters and one transmission gate. One inverter and one transmission gate are present in the storage feedback path. TG2 turns off and TG1 turns on when the clk signal is '1' then the input data value is directly propagated from input D to output Q. TG2 turns on and TG1 turns of when the clk signal is '0'then the stored logic state in kept undisturbed. Out of the two modes available for operation while the circuit is in latching mode unexpected ionizing particles with higher energy are responsible for occurring of SEU that leads to transient voltages. According to the figure shown in Fig.1 in1 is the node that is having the minimum critical charge and it is one most likely to flip. Simplicity is the major advantage of this latch but while highly susceptible to SEU is main drawback of this latch.

II.EXISTING SEU-TOLERANT LATCH CIRCUIT DESIGN

The SEU-tolerant latch design uses the DICE design for further improvement in enhancing its SEU-tolerance. It is compatible to recover the SEU faults in storage node pairs in one another and also not to get affected by each other. The high energy particle strike is resisted by using isolation mechanism. In this method the output node q1 is made apart from q0, q2 and to isolate from SEU interference the signal propagation path is being cut during the latching mode.

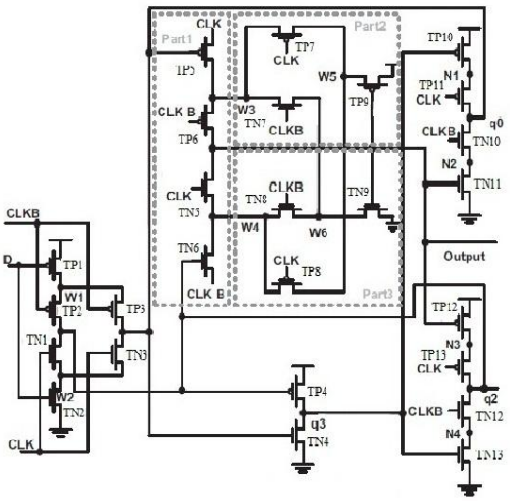

Fig. 2. The Isolated-DICE latch.

Fig.2. shows the isolated –DICE latch design, in this design the output node is made isolated by using the two additional MOS transistors TP6 and TN5 to maintain the stored logic state. The signal transmission paths to q1 form w4 and w3 are broken off when CLK = 0 and CLKB =1 and thus the logic state can be protected in the output node q1 from the impact of soft errors. To maintain the same logic state in w4 and w3 a feedback circuit is present, through this feedback circuit the logic state of w3 and w4 are set to inverse of q1 to avoid isolation mechanism getting destroyed by the single event upset.

In the latching mode, when the output q1 is at logic'1', transistor TP9 becomes off and the transistor TN9 becomes on, and nodes w4 and w3 are directly connected to VSS(ground voltage level) even when the SEU is affected the output node is not affected in the similar manner when the output q1 is at logic'0', transistor TP9 becomes on and the transistor TN9 becomes off, and nodes w4 and w3 are directly connected to VDD instead (supply voltage level) even when the SEU is affected the output node is not affected too. The isolation mechanism in this method is capable of tolerating multiple soft errors along with resisting of single particle strikes. The transistors TP6 and TN5 are turned off for preventing the faults of surrounding internal nodes to propagate to the output q1.

III.PROPOSED SHIFT REGISTERS

Shift registers are interns referred to as sequential logic were sequential circuits are not only affected by the present state but also the previous state that can be used for storing data in the form of binary numbers. In the other sense sequential logic remembers the past events too. These register includes certain discrete delay in the digital signal. The delay in the digital signal depends on the number of stages a register may includes for example a n-bit delay is obtained for a n-stage shift register, here the stage indicates that is a delay stage they are formed using D-flip flop /latch the basic schematic diagram of D latch is as shown in the figure 3

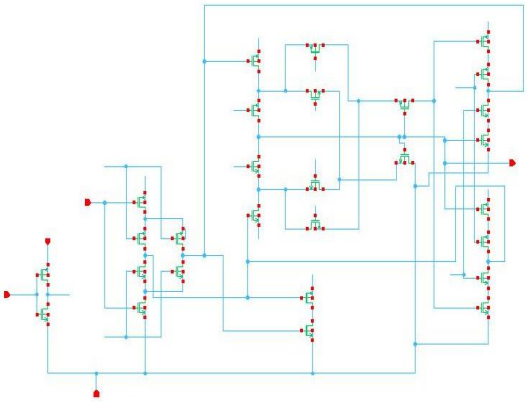

Fig.3. Schematic of Isolated-DICE latch

Shift registers are classified according to structure into following types they are as mentioned below

- *A.* Serial in / serial out
- *B.* Parallel in / serial out
- *C.* Serial in / parallel out
- *D.* Parallel in / parallel out

A. Serial in / serial out (SISO)

In this register the data is shifted serially from input to the output only one bit at a time under the clock control the block diagram of SISO register is as shown in the figure 4.

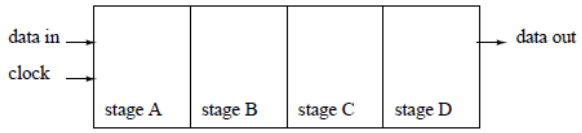

Fig.4. 4-stage SISO shift register

B. Parallel in / serial out (PISO)

In this type of register parallel data is loaded into the register simultaneously and is shifted out of the register in a serial manner under the clock control one bit at a time. The block diagram of PISO register is as shown in the figure 5.

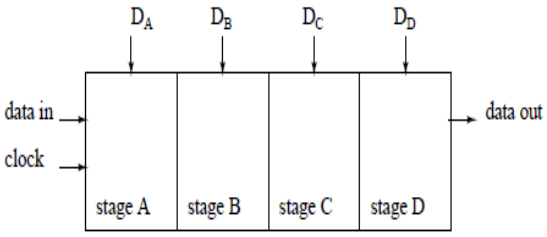

Fig.5. 4-stage PISO shift register

C. Serial in / parallel out (SIPO)

In this register the serial data is loaded, one bit at a time, with the stored data in the register is being available at the each individual output in parallel form. The block diagram of SIPO register is shown in the figure 6.

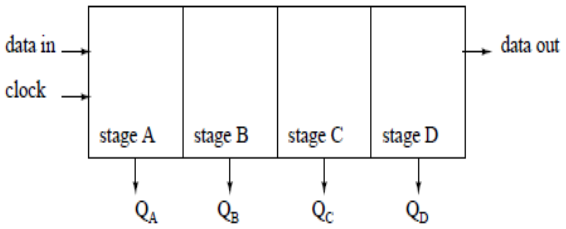

Fig.6. 4-stage SIPO shift register

D. Parallel in / parallel out (PIPO)

In this type of register parallel data is loaded into the register simultaneously, and the output data is transferred together to their respective outputs by the same clock pulse. The block diagram of PIPO register is as shown in the figure 7.

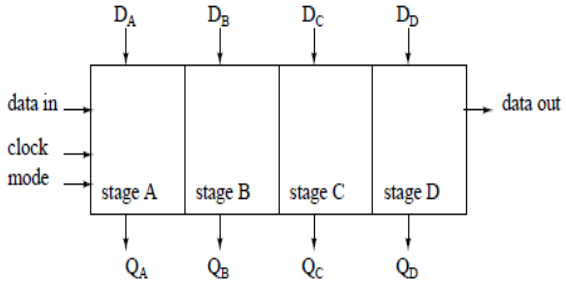

Fig.7. 4-stage PIPO shift register

IV.SIMULATION RESULTS

The design and Simulation is done in CADENCE virtuoso environment using 45nm and 90nm technology design rule which is suitable for operating are V_{DD} 0.7V-1.2V, a gate length of 45nm and 90nm, width of 360nm, 240nm and 120nm PMOS and NMOS respectively in order to provide efficient outputs. The four shift registers schematic and output waveforms are clearly mentioned

A. Serial in / serial out (SISO)

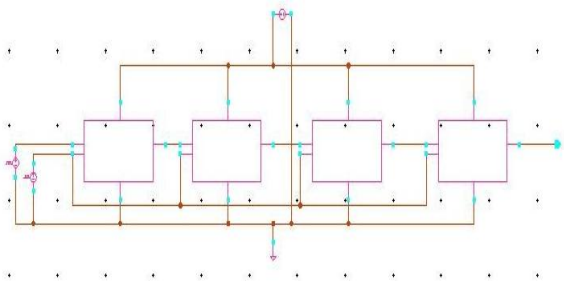

Fig.8.Schematic diagram of SISO shift register

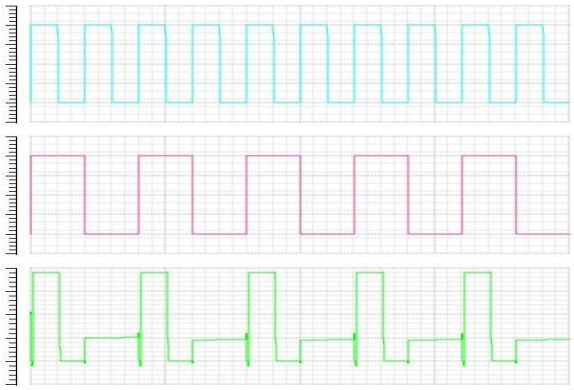

Fig.9. Simulated waveforms of SISO shift register

B. Parallel in / serial out (PISO)

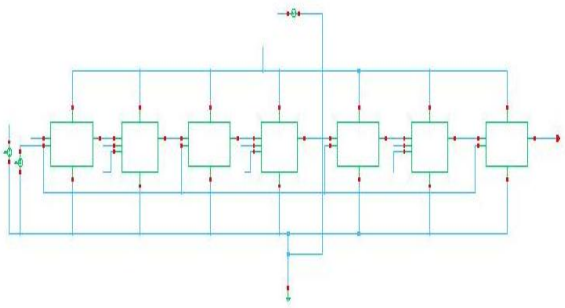

Fig.10. Schematic diagram of PISO shift register

Fig.11. Simulated waveforms of PISO shift register

C. Serial in / parallel out (SIPO)

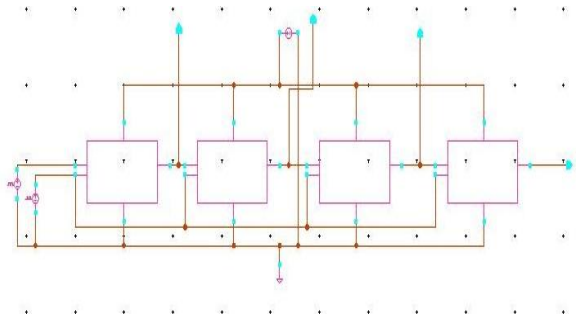

Fig.12. Schematic diagram of SIPO shift register

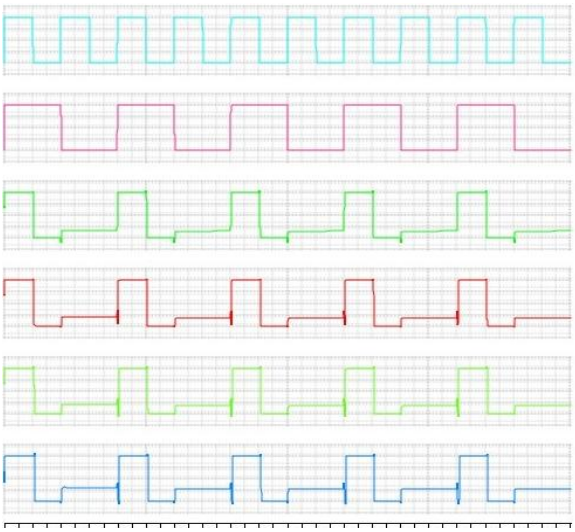

Fig.13. Simulated waveforms of SIPO shift registers

D. Parallel in / parallel out (PIPO)

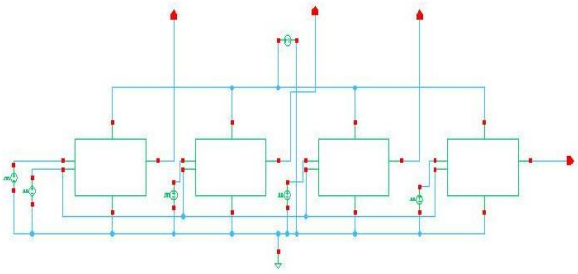

Fig.14. Schematic diagram of PIPO shift register

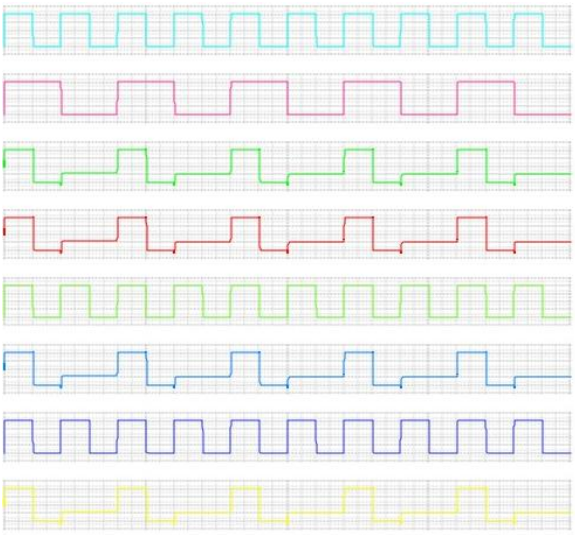

Fig.15. Simulated waveforms of PIPO shift register

Table.1. Average power observations

S.NO	SHIFT REGISTERS	BASIC LATCH (µw)	ISOLATED -DICE LATCH	
			90 nm (nw)	45 nm (nw)
1.	SISO	4.89	32.53	13.31
2.	PISO	20.25	34.25	16.47
3.	SIPO	4.89 4.95 5.04 5.12	30.94 31.62 31.75 32.53	12.79 12.90 12.94 13.31
4.	PIPO	20.49	30.79	13.08

Table.2. Delay observations

S.NO	SHIFT REGISTERS	BASIC LATCH (ps)	ISOLATED -DICE LATCH	
			90 nm (ps)	45 nm (ps)
1.	SISO	354.3	426.7	50.69
2.	PISO	394.3	82.66	41.45
3.	SIPO	107.5 203.3 299.1 354.3	97.83 201.2 329.5 426.7	30.82 34.02 36.49 39.89
4.	PIPO	066.7	78.93	36.88

V. CONCLUSION

In this paper SISO, PISO, SIOP and PIPO shift registers are designed using a robust SEU-tolerant latch design, under 90 nm and 45nm CMOS technology. Simulation results and tabulated observations shows that the newly designed shift registers are much more efficient in power and delay. However, the shift registers using basic latch consumes more energy and performs with larger delay. The proposed shift registers are capable of masking multiple SEU's when compared to the general shift registers.

REFERENCES

[1] A low power-delay-product and robust Isolated-DICE based SEU-tolerant latch circuit design I-Chyn Wey[a], Yu-Sheng Yang[c], Bin-Cheng Wu[c], Chien-Chang Peng[b] Volume 45, Issue 1, January 2014, Pages 1–13

[2] D. Rennie, D. Li, M. Sachdev, B.L. Bhuva, S. Jagannathan, S.J. Wen, R. Wong, Performance, metastability, and soft-error robustness trade-offs for flip-flops in 40 nm CMOS, IEEE Transactions on Circuits and Systems-I 59 (8) (2012).

[3] E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, T. Toba, Impact of scaling on neutroninduced soft error in SRAMs from a 250 nm to a 22 nm design rule, IEEE Transactions on Electron Devices 57 (2010) 1527–1538.

[4] M. Omana, D. Rossi, C. Metra, High-performance robust latches, IEEE Transactions on Computers 59 (11) (2010) 1455–1465.

[5] D.R. Blum, J.G. Delgado-Frias, Delay and energy analysis of SEU and SETtolerant pipeline latches and flip-flops, IEEE Transactions Nuclear Science 56 (June. 2009) 1618–1628.

[6] N. Miskov-Zivanov, and D. Marculescu, A systematic approach to modeling and analysis of transient faults in logic circuits, in: Proceedings of Quality of Electronic Design, pp. 408–413, 2009.

[7] S. Gangadhar, M. Skoufis, and S. Tragoudas, Propagation of transients along sensitizable paths, in: Proceedings of Fourteenth IEEE International On-Line Testing Symposium, pp. 129–134, 2008.

[8] P. Shivakumar, M. Kistler, S.W. Keckler, D. Burger, and L. Alvisi, Modeling the effect of technology trends on the soft error rate of combinational logic, in: Proceedings of the International Conference on Dependable Systems and Networks, pp. 389–398, 2002.

[9] R.C. Baumann, Radiation-induced soft-errors in advanced semiconductor technologies, IEEE Transactions on Device and Materials Reliability 5 (3) (2005) 305–316.

[10] P. Hazucha, C. Svensson, Impact of CMOS technology scaling on the atmospheric neutron soft error rate, IEEE Transactions on Nuclear Science 47 (2000) 2586–2594.