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Design of Seven Level Cascaded H-Bridge Inverter Using MLI with 3 phase DC Source by carrier overlapping

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***Abstract*- This project presents a new technique for getting a multilevel output and also uses PWM control techniques. This new type of converter is suitable for high voltage and high power applications.Multilevel inverter offers a new class of three phase seven level inverter by using the modulation technique to reduce the number of switches and find the performance parameters .However as the number of voltage levels grows the number of active switches reduces for the cascaded H-bridge multilevel inverter.The proposed topology results in reduction of the number of switches,losses,installationarea,and converter costIt provides a high equalization efficiency.This paper proposes three Carrier Overlapping PWM (COPWM) methods that utilize the (CFD) control freedom degree of vertical offsets among carriers. They are: COPWM-A, COPWM-B, COPWM-C these three methods are simulated by using the MATLAB/SIMULINK.**

Keywords— multilevel inverter; cascaded H-bridge; multicarrier pulse width modulation; carrier overlapping, cascaded neutral –point clamped inverter .

1.INTRODUCTION

The voltage source inverters produce an output voltage or current with levels either 0 or ±Vdc. They are known as the two-level inverter. To produce a quality output voltage or a current wave form with less amount of ripple content, they require high switching frequency. In high- power and high voltage applications these two level inverters, however, have some limitations in operating at high frequency mainly due to switching losses and constraints of device ratings. These limitations can be overcome using multilevel inverters. There are 3 types of multilevel inverters named as diode clamped multilevel inverter, flying capacitor multilevel inverter and cascaded multilevel inverter. Using multilevel technique, the amplitude of the voltage isincreased, stress in the switching devices is reduced and the overall harmonics profile is improvedAmong thefamiliar topologies, the most popular one is cascaded multilevel inverter. The cascaded multilevel inverter switching signals are derived from the proposed triangular-sampling current controller that results in a good dynamic performance under both steady state and transient operations.[5].These three types of multilevel inverters requires more no. of components such as switches, clamping diodes and capacitors.The research on multilevel inverter is ongoing further to reduce the number of switching devices count to reduce the manufacturing cost, capacitor voltage balancing .As the number of voltage levels m grows the number of active switches increases according to 2×(m-1) for the cascaded H-bridge multilevel inverters. Multilevel inversion is a power conversion strategy in which the output voltage is obtained in steps thus bringing the output closer to a sine wave and reduces the total harmonic distortion (THD).Multilevel inverter has drawn tremendous interest in high power applications because it has many advantages:it can realize high voltage and high power output through the use of semiconductor switches without use of transformer and without dynamic voltage balance circuits.when the number of output levels increases,harmonic of the output voltage and current as well as EMI decrease.Three PWM methods with different vertical and horizontal offset combinations are investigated in[1-3] leading to the quantification of their output harmonics.This paper presents a 3–Φ seven level cascaded H-bridge multilevel inverter based on an source and carrier overlapping . Compared with the existing cascaded multilevel inverters, the proposed inverter topologies can have enhanced performance by implementing the pulse width modulation (PWM) techniques. The gating pulses for the inverter is generated for various references and multicarrier overlapping pulse width modulation strategy (Type A, Type B and Type C). This paper also presents the most relevant control and modulation methods by a new reference/carrier based PWM scheme for MLI inverter and comparing the performance of the proposed scheme with that of the existing cascaded H-bridge multilevel inverter. The proposed inverter can significantly reduce the switch count as well as the number of gate drivers as the number of voltage levels increases. For a given number of voltage levels m, the cascaded inverter requires m+3 active switches, roughly half the number of switches.

II.PROPOSED SYSTEM

In this proposed system series-connected seven-level TCHB cells to reduce the switchcount and THD minimization [1]. The main of the proposed system is inverter provides higher output quality with relatively lower power loss as compared to the other conventional inverters with the same output quality.The general block diagram for the proposed inverter is shown in fig and the general configuration of the proposed

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inverter topology is shown in.Compared with the existing multi level inverters, the new MLI inverters can significantly reduce the switch count as well as the no. of gate drivers as the no. of voltage levels increases. For a given no. of voltage levels m, the new inverter requires m+3 active switches, roughly half of the no. of switches, clamping diodes, and voltage-splitting capacitors in the diode clamped configuration or clamping capacitors in the flying capacitor configuration.the comparison of the proposed MLDCL inverter and cascaded inverters based on required number of switches and number of levels. From this comparison it is clear that as the number of voltage levels, m, grows, the number of active switches increases according to m+3 for the inverter, compared to 2(m-1) for the cascaded H-bridge multilevel inverters.

BLOCK DIAGRAM

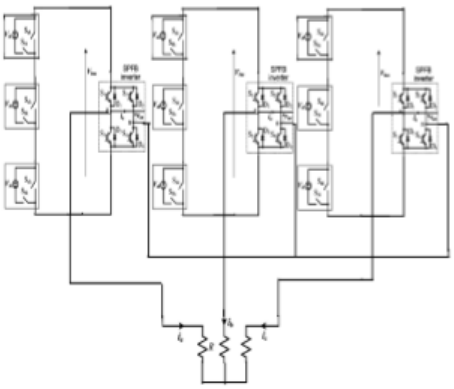

Table .2 Switching sequence for 1–Φ 7 level cascaded inverter

Output voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
0Vdc	1	0	1	0	1	0	1	0	1	0	1	0
Vdc	1	0	0	1	0	0	1	1	0	0	1	1
2Vdc	1	0	0	1	0	0	1	1	1	0	0	1
3Vdc	1	0	0	1	1	0	0	1	1	0	0	1
-Vdc	0	1	1	0	1	1	0	0	1	1	0	0
-2Vdc	0	1	1	0	0	1	1	0	1	1	0	0
-3Vdc	0	1	1	0	0	1	1	0	0	1	1	0

III. MODULATION TECHNIQUES FOR CONTROL SCHEME

There are many modulation techniques for multi-level inverters. Multilevel inverter has to synthesize a staircase waveform by using the modulation technique to have the controlled output voltage [1].Carrier based modulation (SPWM) technique is easy and efficient.The high number of switches composing a multilevel converter may lead to the conclusion that complex algorithms are necessary. The modulation algorithm used to drive the multilevel converter has to be aimed to give the voltage level required for each leg; the translation in the proper switch configuration is done by other algorithms which can be hardware or software implemented. The modulation strategy used here is the multicarrier carrier overlapping pulse width modulation This paper presents three COPWM methods that utilize the CFD of vertical. offsets among carriers. They are COPWM-A, COPWM- B, COPWM-C. The above three methods are simulated in this paper. For an m-level inverter using carrier overlapping technique, m-1 carriers with the same frequency fc and same peak-to-peak amplitude Ac are disposed such that the bands they occupy overlap each other: the overlapping vertical distance between each carrier is Ac/2. The reference waveform has amplitude of Am and frequency of fm and it is centered in the middle of the carrier signals.The amplitude modulation index ma and the frequency ratio mf are defined in the carrier overlapping method as follows:

$$ma = Am/((m/4)* Ac)$$

$$mf = fc / fm$$

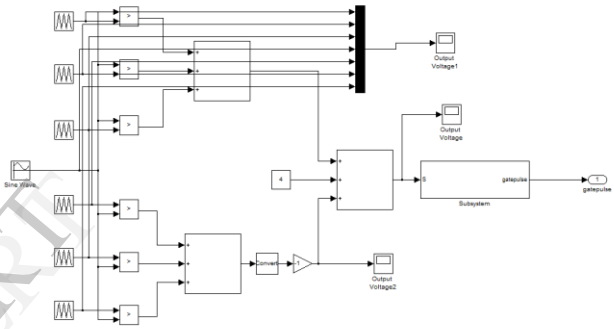

Fig 1.Simulink for copwm method A

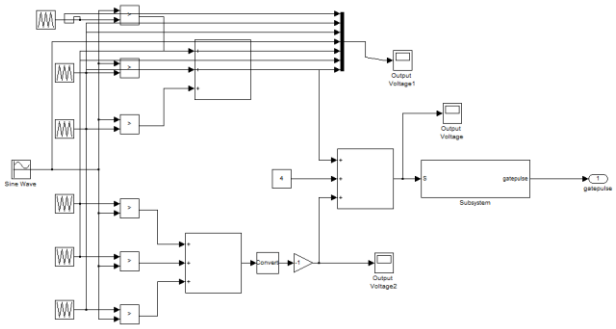

Fig 2.simulink for copwm method B

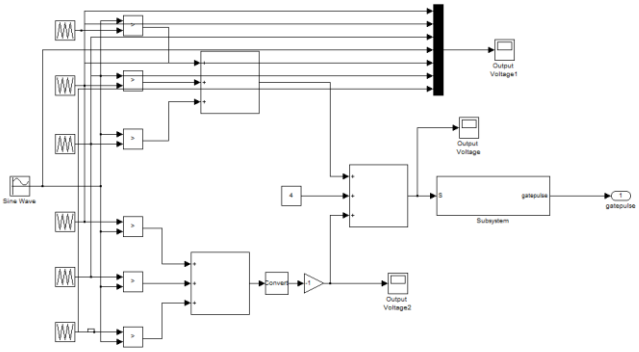

Fig 3.simulink for copwm method C

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1V. SIMULATION RESULTS

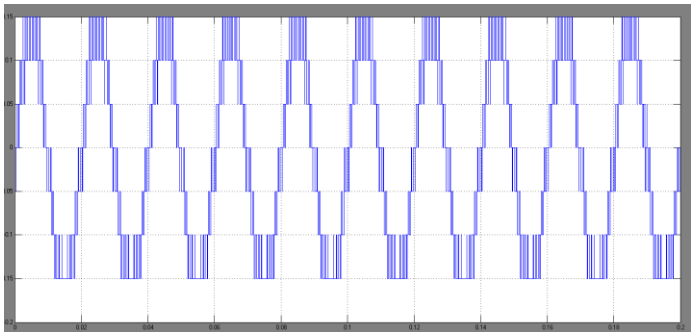


Fig 4.Output current waveform of the proposed Three-phase 7-level inverterusing PWM

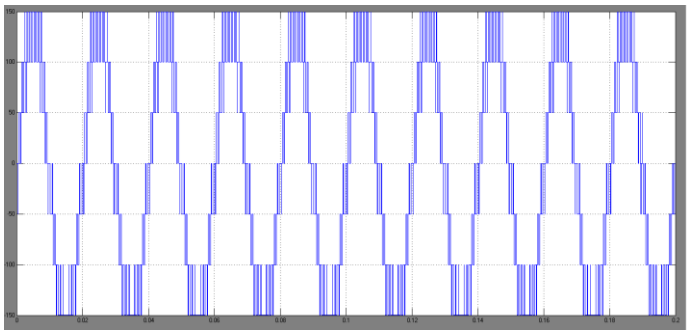


Fig.5.Output voltage Waveform of theproposed Three phase 7-level inverter using PWM

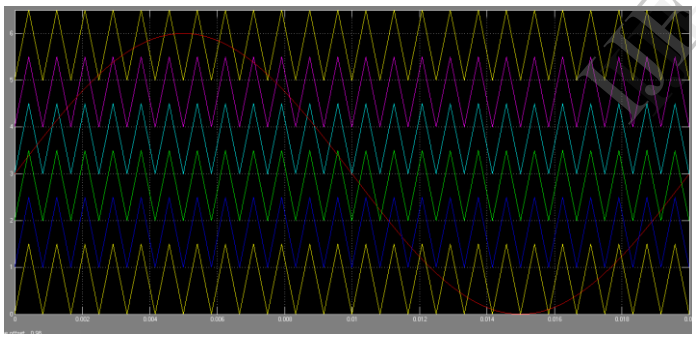


Fig 6 COPWM –METHOD A (m=1)

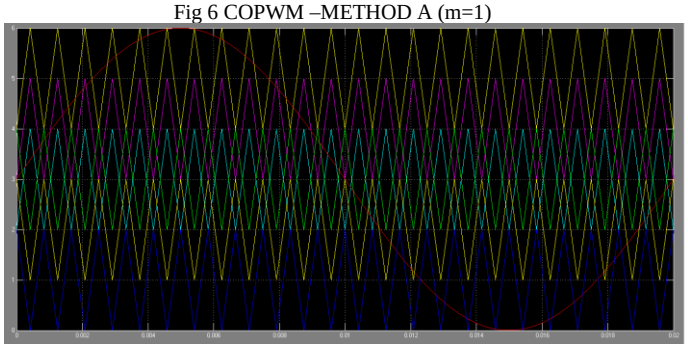


Fig 7.COPWM-METHOD B (m=1)

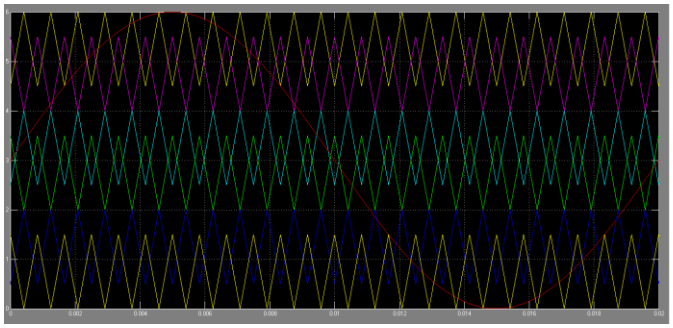
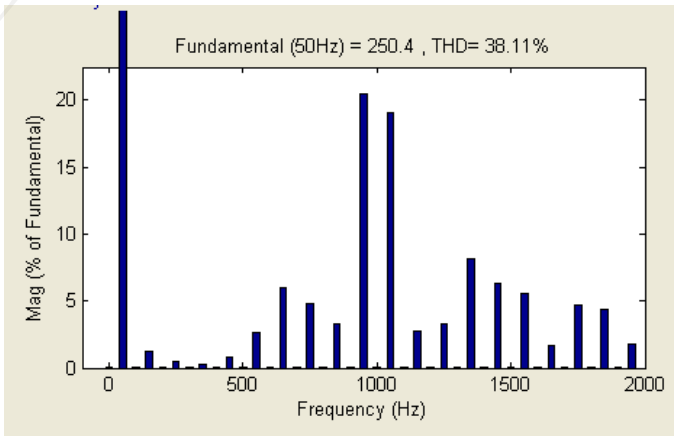


Fig 8.COPWM-METHOD C (m=1)

V. ANALYSIS AND COMPARISON OF PROPOSED WITH CONVENTIONAL MLI

In the proposed 7-level multilevel inverter topology the number of switches is only one more then the 7-level single phase cascaded H-bridge inverter. To produce the same output voltage the cascaded H-bridge has to use the two cells where as only one cell is required with the proposed topology. The total harmonic distortion produced by the proposed inverter is 38.11% only, Fig.6 shows the THD in % for three phase 7-level proposed multilevel inverter which is very low as compared to the single unit of conventional H-bridge inverter having THD of 70.99%.In order to produce the nine levels in the output voltage the conventional H-bridge requires three cells where as the proposed topology requires only two cells.



V1.CONCLUSION

The presented seven level MLDCL inverters can eliminate roughly half the number of switches, their gate drivers compared with the existing cascaded MLI counterparts. Cascaded 3-phase 7level are simulated for sinusoidal PWM technique with COPWM-A, COPWM-B, COPWM-C .The COPWM-A method provides lower THD than the other methods for moderate ma whereas for high ma(1).Compared with other inverters the cascaded inverter has given good fundamental output voltage with reduced THD.

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