DESIGN OF SAMPLE AND HOLD FOR 7 BIT 100MHz FLASH ADC

ASHNA A
Asst.Professor, Dept.of Electronics and Communication Engg,
MES Institute of Technology and Management,
Chathannoor, Kollam,
ashna009@gmail.com

***Abstract*—The highest bandwidth signal that can be digitized by an analog-to-digital converter is often govern by the performance of a preceding sample-and-hold circuit. Comparators in a flash converter generate what is commonly known as a thermometer code. The encoder is used to convert the thermometer code, generated by the comparators, into a binary code that approximates the input signal. In this paper, the fully differential sample and hold circuit has been designed and simulated on 90nm CMOS technology in order to meet the given specications. This design is free from the non-linearities such charge injection, clock feed-through etc that are present in open-loop or single ended configuration. The circuit designed is capable of sampling the input with the precision of 7-bits, having Flash ADC with clock frequency of 100MHz.**

I. INTRODUCTION

ADCs are utilized broadly in signal processing systems for converting analog signals in to digital signals. An ADC is a device that uses sampling to convert a continuous quantity to a discrete time representation in digital form. It may also provide an isolated measurement such as an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current. The function of an ADC is to accurately convert an analog input signal into digital output represented by a coded array of binary bits. The output bits are generated by processing the analog input signal through a number of comparator steps. The number of bits in the generated code represents the resolution of ADC.

II. FLASH ADC

A Flash ADC (also known as a Direct conversion ADC) is a type of fastest analog-to-digital converter that uses a linear voltage ladder with a comparator at each "rung" of the ladder to compare the input voltage to successive reference voltages. Often these reference ladders are constructed of many resistors; however modern implementations show that capacitive voltage division is also possible. The output of these comparators is generally fed into a digital encoder which converts the inputs into a binary value. Flash analog-to-digital converters, also known as parallel ADCs. Flash ADCs are suitable for applications requiring very large bandwidths and consume considerable power, have relatively low resolution, and can be quite expensive. This limits them to high-frequency applications that typically cannot be addressed any other way. The design consists of the following components,

a)Sample and hold circuit
b)Comparator
c)Encoder

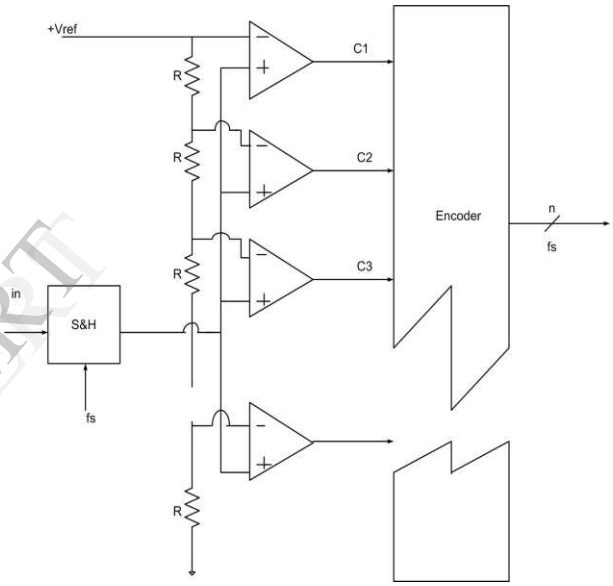

Figure 1: Architecture of Flash ADC

Flash ADCs are made by cascading high-speed comparators. For an N-bit converter, the circuit employs 2^N-1 comparators. A resistive-divider with 2^N resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a 1 when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is 0. This architecture is known as thermometer code encoding. This name is used because the design is similar to a mercury thermometer, in which the mercury column always rises. to the appropriate temperature and no mercury is present above that temperature. The thermometer code is then decoded to the appropriate digital output code. The comparators are typically a cascade of wideband low-gain stages. They are low gain because at high frequencies it is difficult to obtain both wide bandwidth and high gain. The comparators are designed for low-voltage offset, so that the input offset of each comparator

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is smaller than an LSB of the ADC. Otherwise, the comparator's offset could falsely trip the comparator, resulting in a digital output code that is not representative of a thermometer code. A regenerative latch at each comparator output stores the result. The latch has positive feedback, so that the end state is forced to either a 1 or a 0.

III. SAMPLE AND HOLD CIRCUIT

The function of the sample and hold circuit is to sample the unknown analog signal and hold that sample while the ADC decodes the digital equivalent output. When the SHA is used with an ADC the SHA performance is critical to the overall dynamic performance of the combination, and plays a major role in determining the SFDR, SNR etc of the system. The SHA is used to maintain the input to an ADC at a constant value during conversion. That is ,a sample-and-hold samples the continuous-time input and holds it for half a clock cycle.

A) Need for Sample and hold

If we are directly feeding an analog signal to an ADC, it cannot make correct decision because the analog input is changing the value instantaneously, so we are sampling the value of an analog input and holding the value for sometime so that ADC get enough time to take decision. For this we are making use of sample and hold circuitry.

B) Factors which affect the performance of Sample and Hold Circuit

a) Sampling pedestal (hold step)

This error occurs when the circuit switches from sample mode to the hold mode. During this change in operation, there is always a change in voltage being held that makes it different from the input voltage at the time of sampling. It is important to know that this error must be independent from input signal. This error may cause nonlinear distortion.

b) Slew Rate and 3db bandwidth

The speed at which a sample and hold can track an input signal in sample mode. This parameter is limited by the slew rate and the -3db bandwidth in both small signals and large signals. It is necessary to maximize SR and 3db bandwidth for high speed performance.

c) Aperture jitter (aperture uncertainty)

This error is the result of effective sampling time changing from one sampling instance to the next and becomes more pronounced for high speed signals.

d) Droop rate

This error is a slow change in output voltage when in hold mode, caused by effects such as leakage current due to the finite base currents of bipolar transistors and reverse biased junction. In CMOS design droop rate is small and can be ignored.

C) Design Issues of CMOS Sample and Hold

a) Sampling Moment Distortio

Clock rising/falling time results in distortion

$$4V_s = 2 \times t_{rise} \times \frac{a}{V_{clock}}$$

b) Clock Feed-through

Overlap capacitance of MOS Switch creates an sampling error during clock transition time.

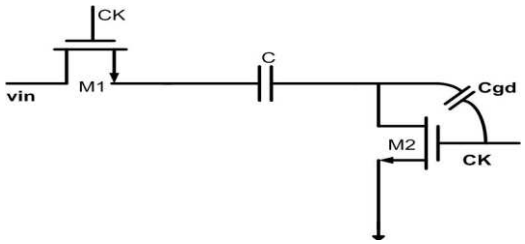

Figure 2: Clock Feed-through

c) MOS Switch Charge Injection

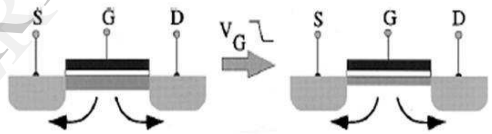

Figure 3: MOS Switch Charge Injection

Some charge in the MOS channel flow to Source and Drain, then result in an error It leads to 3 type of errors such as gain error, DC offset and non-linearity.

$$\triangle Q = Cox\ (Vgs - Vth),\ V_{hold} = \frac{\triangle Q}{C_h}$$

The circuit suffers from a gain error of approximately,

$$\text{Gain Error} = \frac{1}{1 + \text{Loop Gain}}$$

d) KT/C noise

During the "on" phase, the switch can be modeled as a resistor. The equivalent thermal noise of this resistor (R_{on}) has a one-sided, white-noise-like power spectral density.

$$\text{Total Noise Power} = V^2 = \frac{KT}{C}$$

In order to avoid the above design issues, we are going for another kind of sample and circuit which is fully differential.

D) Differential Sample and Hold

It is used to avoid the design issues occurs in normal Sample and hold. It consists of

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1. Op-amp
2. CMFB circuit
3. Sample and Hold network

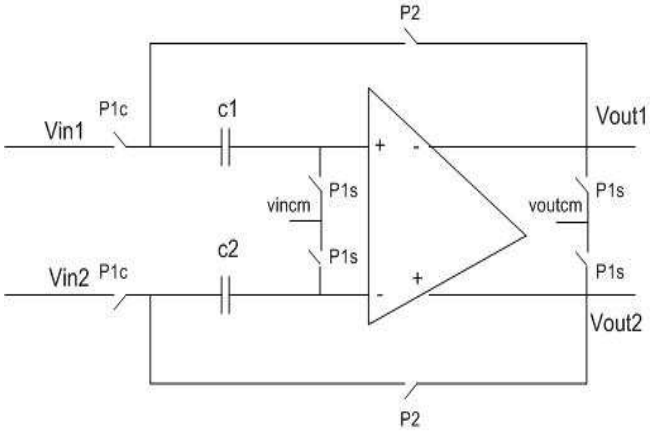

Figure 4: Sample and Hold

Here we are providing two common modes input common mode and output common mode. During the sample mode the switches P1c and P1s gets closed and switch P2 is opened and the capacitors c1 and c2 gets charged to Vi-Vincm. During the hold mode the switches P1c and P1s gets opened and switch P2 gets closed. During this time the output gets charged to Voutcm- (Vin-Vincm). From Figure, during the sample phase the switches P1c and P1s gets closed at the same time. During the hold phase the P1s gets opened earlier in order to avoid charge injection. That is during the starting of hold mode there is a chance that a charge packet will move from input to the capacitor and causes a change in the stored charge. But if the switch P1s opens earlier there is no path for the capacitor to get charge so charge injection effect can be avoided.

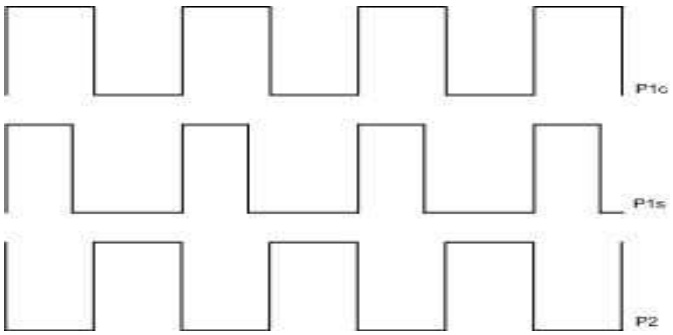

Figure 5: Clock for Sample and Hold

E) **Op-amp**

Fully differential op-amp which have a differential input and produce a differential output. They are widely used in Integrated circuits because they have some advantages over their single ended counterparts, They provide larger output voltage swing and are less susceptible to common mode noise. Also even order non-linearities are not present in the differential output of a balanced circuit. The disadvantages of fully differential op-amps is that they require two matched feedback networks and a common-mode feedback circuit to control the common-mode output voltage. For getting high gain and output swing two stage fully differential op-amp is selected. In first stage of the amplifier, I have used fully differential telescopic op-amp to provide provides high gain because of high output resistance and the common source amplifier is used in second stage to get maximum output swing.

a) ***Design of Opamp***

- First stage Telescopic Op Amp

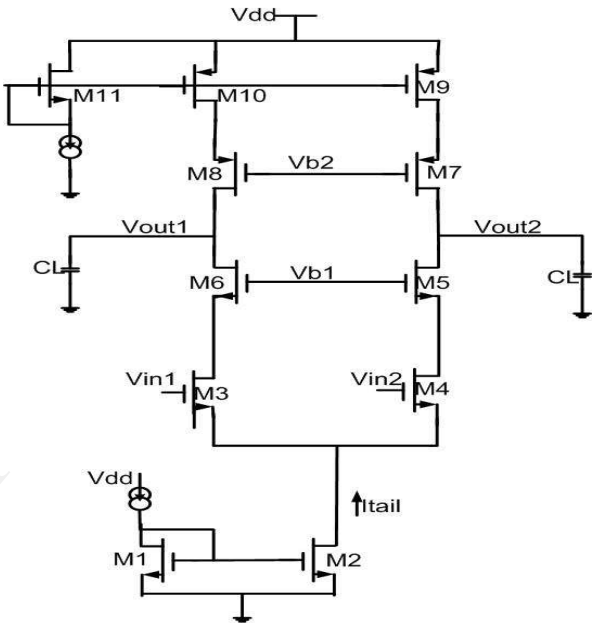

Figure 6: First Stage Telescopic Op-amp

Power(P)=5mW, Vdd(V)=1:2V
P = V x I
i.e., I = P/V =5mW / 1.2V = 4mA
ie, tail current is 4mA.
Required swing at each output node is 0.3V
A marginal value of 50mV is applied to each transistor on each side
50mV x 5= 0.25V
Total voltage available for Vdsat
1.2-0.3-0.25= 0.6V = 650mV
Vdsat (M9) +Vdsat (M7)+Vdsat (M5)+Vdsat (M4)+Vdsat (M2)=600mV
Vdsat (M2)=250mV
Vdsat of pmos = 2Vdsat of nmos
So,2Vdsat(M4)+2Vdsat(M5)+Vdsat(M5)+Vdsat(M4)=650mV
6 x Vdsat=400mV
Therefore Vdsat=66.6mV for nmos
For pmos, Vdsat=2 x Vdsat of nmos = 133.32mV

From this we can calculate the bias voltages and the width and length of each transistors so that each transistor operate in saturation region. Width and length is calculated with the help of equation of current in saturation region.

$I_D = 1/2u_nCoxW/L(VGS-VTH)^2$

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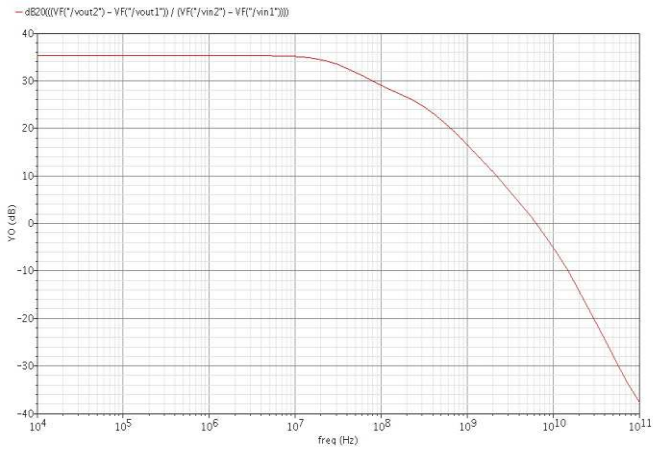

Figure 7: Gain plot of First stage

Gain obtained = 37.01dB

- ***Two stage Op Amp without compensation***

The output swing of the telescopic opamp is limited. So a common source amplifier is connected to the output of second stage. The transistors are properly biased to work in saturation and the output common mode is set at 600mV to obtain the maximum swing.

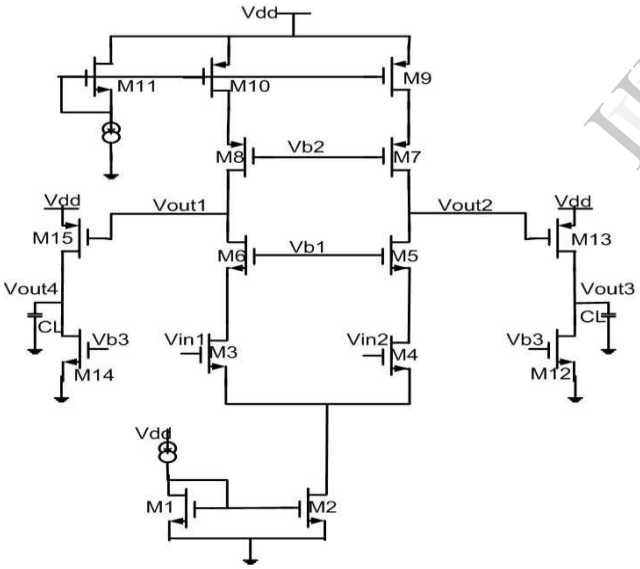

Figure 8: Two stage Op-amp

Vdsat (M13) +Vdsat (M12)=650mV
So, 2Vdsat (M13)+2Vdsat (M12)=650mV
3xVdsat=400mV
Therefore Vdsat=216:67mV for nmos
For pmos, Vdsat=2Vdsat of nmos=433:3mV
Gain obtained = 61.1 dB
Unity Gain Bandwidth = 3 GHz

Before compensation, phase margin of the circuit is -15.29. So the system is unstable. For a system to be stable,the gain cross over frequency should lie before phase cross over frequency. From the graph we understand that the phase cross over frequency (Px) should lies before gain cross over frequency Gx) and got poles which is marked approximately in graph. So the system is unstable. Frequency compensation is used to increase the phase margin of the system.

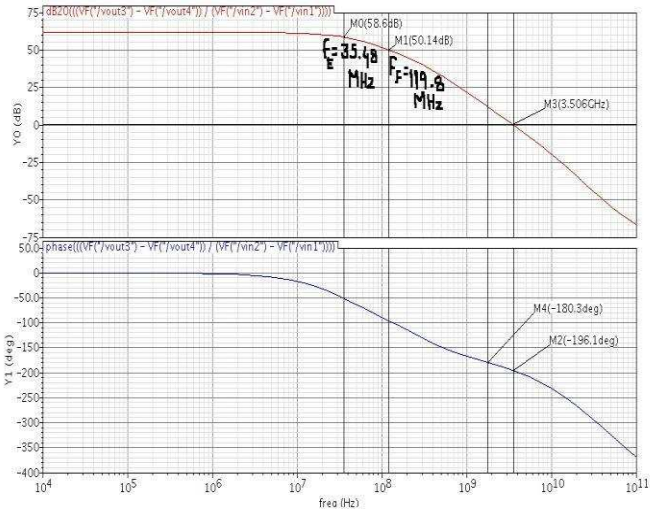

Figure 9: Gain plot of Second stage before Compensation

- ***Frequency Compensation***

Compensation is the process of increasing the phase margin of the system. Here use Miller Compensation with a series resistance to eliminate the zero. At first, I have placed the capacitor only. Because of this capacitor, an additional zero is generated. To eliminate the zero due to feed forward through capacitor, a resistor value of R=150 can be connected in series with the compensation capacitor Cc=3.6pF. After compensation, the system is stable. Here the gain crossover lies inside phase crossover and got two poles which is marked approximately in graph.

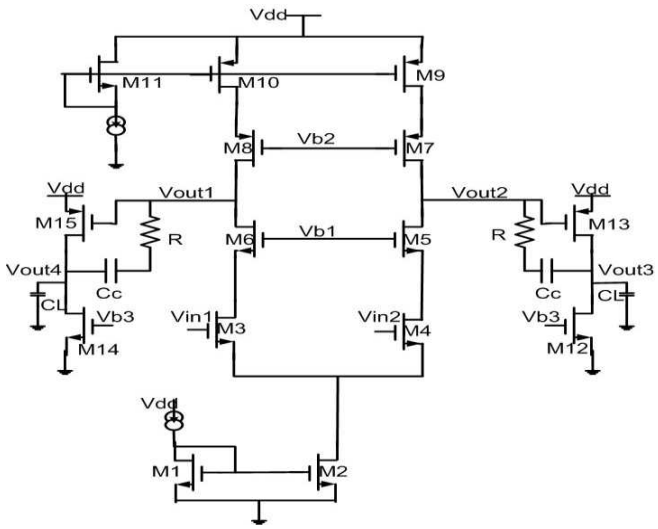

Figure 10: Two Stage Op-amp with Miller Compensation

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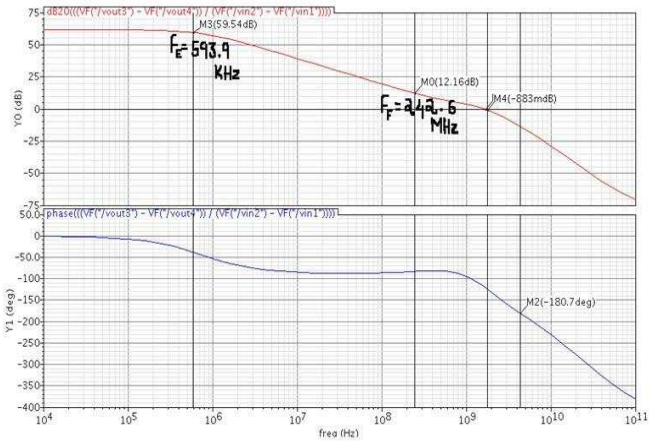

Figure 11: Gain plot of Second stage after Compensation

Phase margin= 60
Unity Gain BW = 1.82 GHz

F) Common Mode Feedback (CMFB)

CMFB is used for stabilizing the output.It control the common mode output voltage. It is used to improve the Common Mode Rejection Ratio (CMRR) and Input Common Mode Range (ICMR). The CMFB circuitry senses the CM output voltage and uses negative feedback to set the CM output voltage to a value that maximizes the opamp output voltage swing. A continous time CMFB is used in this design. CMFB is also used in both stages of op-amp . The schematic of a CMFB circuit using Differential-Difference Amplifier (DDA) is shown figure. Advantages of this CMFB circuit include that it exhibits large transconductance and it does not resistively load the op-amp output. But it reduces the output swing. The matched differential pairs Mf1-Mf2 and Mf3-Mf4 connect to the op-amp outputs Vout1 and Vout1, sense the CM output voltage [Voc = (Vout1+Vout2)/2] of the op-amp, and compare Voc with the desired CM output voltage, Vcm. A negative feedback loop sets Voc to be about equal to Vcm by adjusting a bias current in the op amp that is related to the CM control-signal output of the CMFB circuit, which is Icm.

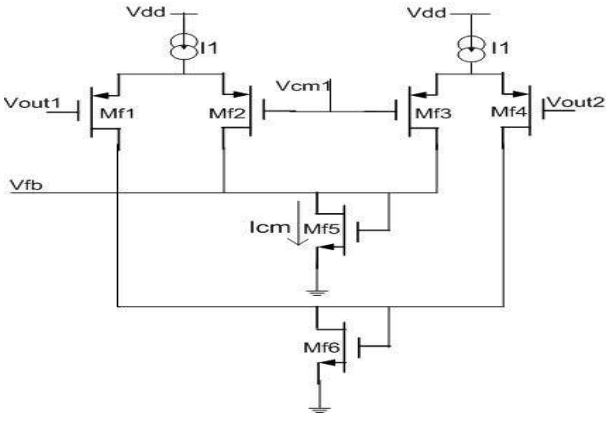

Figure 12: Common Mode Feedback circuit

The basic operation of the CMFB circuit can be illustrated by modeling Mf1-Mf4 as ideal, linear transconducting elements. Since the drain current in Mf5 comes from the drain currents of Mf2 and Mf3, we get Id5 = Icm = I_1 + gm(Voc - Vcm) = I_1+ gmVerr, where gm is the small signal transconductance of Mf1-Mf4 and Verr = Voc - Vcm.

b) *Design of CMFB*

1) *First Stage CMFB*

A Common mode feedback (CMFB) circuit is used for gain stabilization.The source-coupled pairs Mf1-Mf2 and Mf3-Mf4 together sense the CM output voltage and generate an output that is proportional to the difference between dc CM output voltage Voc and V_{CM} . This output is fed as the tail current to the basic telescopic amplifier, hence achieving gain stabilization.

- First apply common mode voltage as input to the CMFB circuit. Here Vcm1= 707.5mV. Size the transistors so as to obtain the output current from CMFB is equal to the gate current of transistor M9 of basic telescopic amplifier. And ensured that all the transistors were in saturation. Initially we set the input voltages of the CMFB as Vout1=Vout2= 707.5mV.
- After sizing the transistors of CMFB, we got the output current of CMFB is approximately equal to the gate current of M2. Then replace the inputs of CMFB with the output voltages (ie, Vout1 and Vout2) from the telescopic amplifier.
- DC and AC analysis were done. Then, gain of 37 dB was obtained.707.5mV

2) *Second Stage CMFB*

- First apply common mode voltage as input to the CMFB circuit. Here Vcm2= 600.6mV. Size the transistors so as to obtain the output current from CMFB is equal to the gate current of transistor M9 of second stage common source amplifier. And ensured that all the transistors were in saturation. Initially we set the input voltages of the CMFB as Vout3 =Vout4 = 600.6mV.
- After sizing the transistors of CMFB, we got the output current of CMFB is approximately equal to the gate current of M2. Then replace the inputs of CMFB with the output voltages (ie, Vout3 Vout4) from the telescopic amplifier.
- DC and AC analysis were done. Then, gain of 61.6 dB and Unity gain BW of 2.16 GHz were obtained.

G) Design of Sample and Hold

The specifications given are
Sampling frequency= 100MHz
Conversion rate= 100Msp
Sampling period= 5ns
Holding period= 5ns

$\alpha + \beta = \chi$. (1) (1)

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The design of the sampling capacitor is based on KT/C noise (sometimes also called the sampling noise) .The noise on the resistance actually is the deciding factor of the value of the capacitor. For example, in this design our accuracy is of 7-bit, that means we have a margin of 9mV around the exact value. we can use the below formula for calculating the value of the sampling capacitor V 2 = KT/C, where K is the Boltzmann's constant and T is the Sampling clock period.

IV . SIMULATION RESULTS

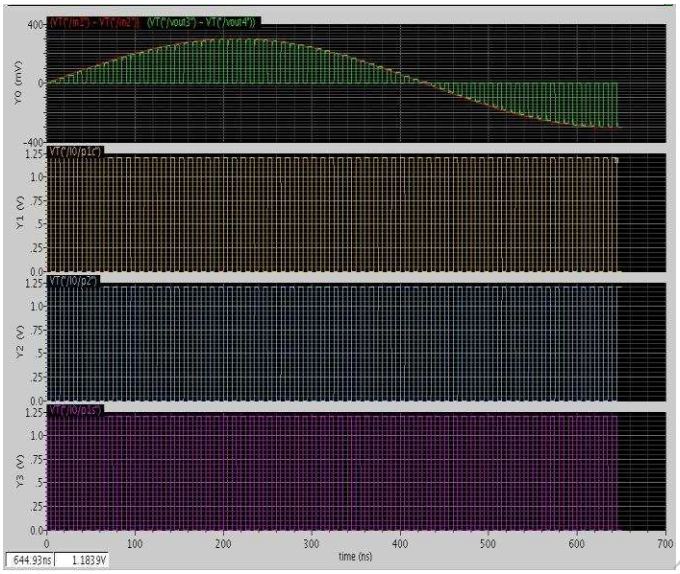

Figure 13: Simulation result of Sample and Hold

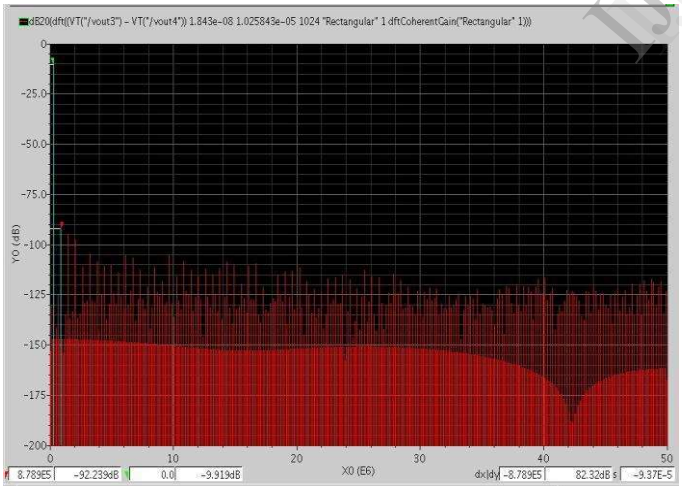

Figure 14: FFT of Sample and Hold

Achieved specification of Sample and Hold circuit are
SFDR = 82.32dB
Output swing = 600mV
Settling time = 1.014ns
Slew rate = 289.56 V/uA
Gain of Op-amp = 61.6dB
Phase margin = 60degrees
Load capacitance of Sample and Hold is 8pF because it is the capacitance obtained from the 127 comparators.

CONCLUSION

With the increasing demand for high-resolution and high-speed in data acquisition systems, the performance of the S/H circuits is becoming more and more important. This is especially true in ADCs since the performance of S/H circuits greatly affects the speed and accuracy of ADCs. The fastest S/H circuits operate in open loop, but when such circuits are implemented in CMOS technology, their accuracy is low. S/H circuits that operate in closed loop configuration can achieve high resolution, but their requirements for high gain circuit block, such as an op-amp, limits the speed of the circuits . As a result, better and faster S/H circuits must be developed.

REFERENCES

[1] Yun-Ti Wang and Behzad Razavi, Member, IEEE, "An 8-Bit 150MHz CMOS A/D Converter", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 35, NO. 3, MARCH 2000.
[2] CHUA-CHIN WANGt, CHENN-JUNG HUANG and PO-MINGLEE, Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan 80424.
[3] A 400-MHz Input Flash Converter with Error Correction, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 25, NO. 1, FEBRUARY 1990, CHRISTOPHER W. MANGELSDORF, Member, IEEE.
[4] 1.5GSPS 4-bit ash ADC using 0.18m CMOS, Khaled Ali Shehata , Hanady Husien , Hani Fekri Ragai.
[5] A 1-GS/s 6-bit Flash ADC in 90 nm CMOS, Mohamed O. Shaker, Soumik Gosh, and Magdy A. Bayoumi ,The Center for Advanced Com-puter Studies University of Louisiana at Lafayette Lafayette, LA 70504, USA .Email: mos5248, sxg5317, mab@cacs.louisiana.edu.
[6] Vipul Katyal, Randall L. Geiger and Degang J. Chen, A New Low O_set Dynamic Comparator for High Resolution High Speed ADC Ap-plication, Semiconductor Research Corporations Student Symposium 2006.

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