Design of RTL Synthesizable 32-Bit FIFO Memory

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Abstract: First-In First-Out (FIFO) memory structures have been the dominant mechanism to control the flow of data between source and destination. The function of FIFO runs around memory element and control circuitry. There are many methods to design FIFO but our focus is on designing single bit memory cell there by 8x32 buffer to be used in synchronous or asynchronous FIFO. Conventional FIFOs use dual port RAM as memory element for FIFO. This work presents a unique idea for storing the data suitable for FIFO to function correctly resulting in increased performance. The novelty of the architecture includes Extra hardware signal Almost Full signal is asserted to avoid overflow (Credit based Information). We have implemented and synthesized Synchronous FIFO in register-transfer-level (RTL) using Verilog along with few sequential latches and digital logic gates and simulation is carried out at the gate-level using Xilinx-ISE 13.3 tool to deliver delay, power and area estimates for the same.

Keyword: Fifo, Synchronous, Rtl.

I. INTRODUCTION

FIFO (first-in, first-out) is a mechanism to handle program work requests from queues or stacks so that the oldest request is handled first. In hardware it is either an array of flops or Read/Write memory where data is written to memory in one clock domain and on request data is read from memory in another clock domain following same order as written. FIFO is said to be SYNCHRONOUS if read and write operations are performed using same clock signal and FIFO is said to be ASYNCHRONOUS if read and write operations are performed using different clock signals The clock domain that supplies data to FIFO is often called as WRITE CONTROL LOGIC and the clock domain that reads data from the FIFO is often called as READ CONTROL LOGIC. FIFOs are used in designs to transfer data words from one clock domain to another or to control the flow of data between source and destination when the input data can not be forwarded right away to the output port. As shown in Fig 1 synchronous FIFO has a single clock port for both data-read and data-write operations. Both write and read events take place at the rising edge of clocks.
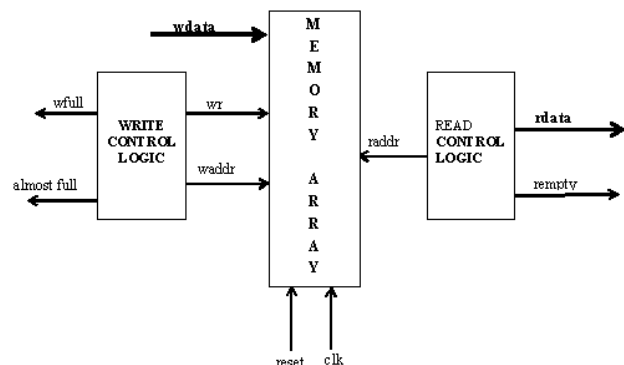

Fig 1. Block diagram of Synchronous FIFO

A Synchronous FIFO has a single clock port for both data-read and data-write operations. Both write and read events take place at the rising edge of clocks. Data can be read out of the FIFO via the module's data-output port in the order in which it was written by asserting read-request prior to a rising clock edge. The RESET signal clears internal control logic and the status flags. In this paper 32-bit Memory-Based synchronous FIFO is designed that could perform read and write operation at same time. After the FIFO is RESET, winc (write enable) signal and rinc (read enble) signal are set to high, wdata is the input data written to FIFO memory in seqential order at rising edge of the clock signal whenever write enable (winc) is high and FIFO is not full; and *rdata* is the output data read from the FIFO memory in same order as written whenever read enable (rinc) is high and FIFO is not empty; Otherwise previous data is available at the output port. FIFO *wfull* and FIFO *rempty* are status flags that represent the status of the FIFO. No data should be written in full condition and no data should be read in empty condition, as it can lead to loss of data or generation of non-relevant data. The ***almost Full*** signal will be HIGH when one location is empty to write data. The *almost full* and *full* signal will eliminate the overhead of sending credit information at every cycle. There are many methodologies to design FIFO memory like using RAM or Using register files. But the proposed FIFO memory is efficient and shows high speed and also minimizes the area. Table 1 shows different input and output signals with their description.

Table:1 Signal description

Signal	Direction	Description
For FIFO		
Reset	input	Resets the FIFO
clk	input	Clock input to FIFO
wdata	input	(32:0) 16 bit data input to the FIFO
rdata	output	(32:0) 16 bit data output from the FIFO
winc	input	Write enable (write request)
rinc	input	Read enable(read request)
Almost full	output	Sets when one location is left to write
full	output	Sets when FIFO is full
For FIFO Memory		
waddr	input	Address of the memory location where the data is to be written into.
raddr	input	Address of the memory location where the data is to be written from.
wr	input	Write enable

II. PROPOSED MEMORY FOR FIFO

This paper presents a novel memory cell structure of for storing single bit. Single bit memory cell consist of D-type flip flop, 2:1 mux and 2- input AND gate. Multiplexer is used to close and open a feedback loop around flip-flop under control of the enable signal. This technique would save a fair amount of power dissipation.
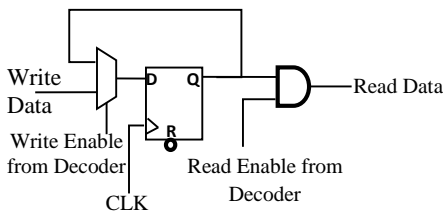

Fig.2 1-bit Memory cell for FIFO

When we want to write data (either '0' bit or '1' bit) into memory then a write enable signal high will be generated though a decoder using write address provided by pointer manager. Similarly in order to read data we will generate read enable through decoder using read address given by pointer manager of FIFO controller.
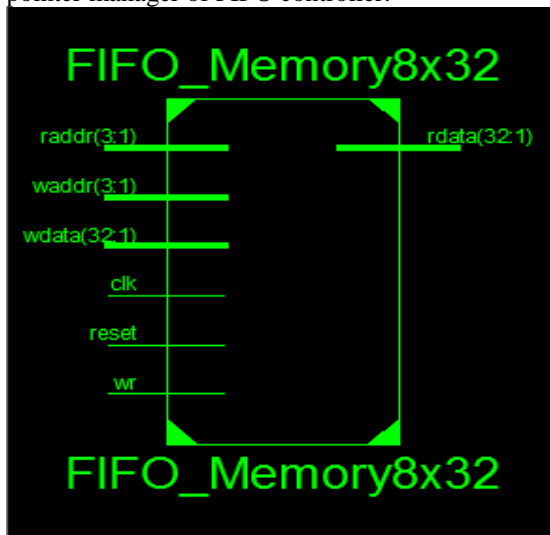

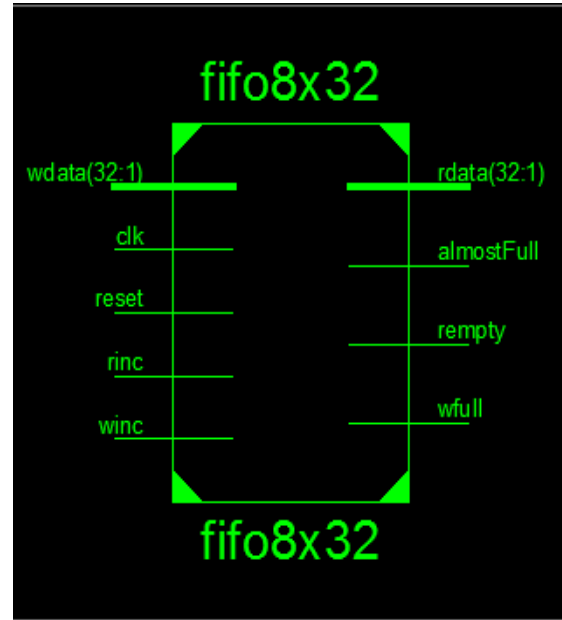Fig.3 RTL diagram of 8x32 FIFO memory
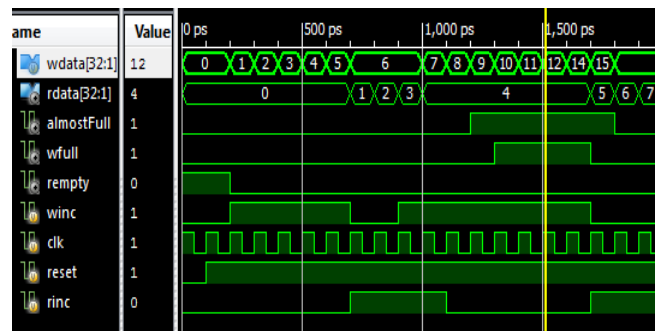

Fig.4   RTL diagram of 8x32 synchronous FIFO

Fig.5 FIFO read and write operation depicting full and empty conditions

Fig.3 shows the RTL diagram of 8x32 FIFO memory which consist of 1-bit memory cells. The depth of the FIFO is 8 while the word length is 32 bit. First of all 32 bit buffer is designed using 1 bit memory cell and then 8x32 FIFO memory is designed and this memory is used to implement synchronous FIFO (fig.4).

III. PERFORMANCE EVALUATION

We use Xilinx Spartan 3E devices to design and implement the FIFO with layout adjustments to fulfil the
timing constraints which are mandatory for the correct operations of the circuits. Firstly, to verify the functionality of the synchronous FIFO, the gate-level simulation of the eight-stage, 32-bit is carried out as shown in Fig. 5. indicating the empty/full conditions.

TABLE2:   FPGA area utilization estimate

Logic utilization	used	Available	Utilization
Number of Slice registers	270	4800	5%
Number of Slice LUTS	401	2400	16%
Number of fully used LUT-FF pairs	267	404	66%
Number of bonded IOBs	71	102	69%
Number of BUFG/BUFGCTRLs	1	16	6%

Area estimation can be done from device utilization summary illustrated in table 2. Dynamic power analysis calculated with the help of Xilinx ISE tool 13.3 is illustrated with the help of fig.6. It can be observed that dynamic power of the dsesign is 4 mw when 100 MHz. Also delay of our design is 5.041ns.
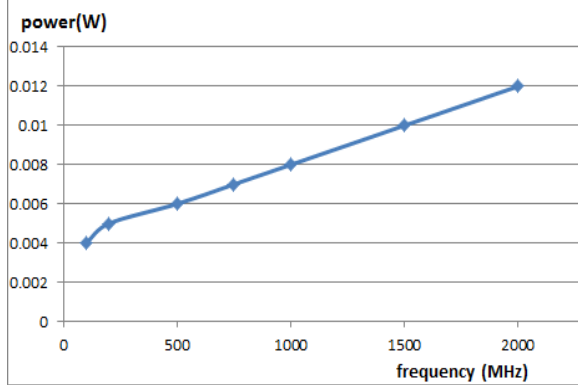

Fig.6 Dynamic power frequency relation

IV. CONCLUSION

A synchronous FIFO design is presented in this paper. The novel memory structure presented in the design enhances the performance of the FIFO in terms of area delay and power. This structure enables the design to reduce a power consumption of 4 mw at frequency of 100MHz. The circuit components (LUTs) are utilized in the range of 5% to 66%. This circuit also reduces the delay period of 5.041ns.

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