Design of Power Efficient 2-4 Decoder for Rom Memories

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***Abstract*--Several pass-transistor logic families have been introduced recently, but no systematic synthesis method which doesn't take signal arrangement on circuit performance into consideration. In the pass transistor logic, a Karnaugh map based method which efficiently synthesized Pass Transistor Logic (PTL) circuits, that have balanced loads on true and complementary input signals was developed. The method was applied to the generation of basic two-input and three-input logic gates in Complementary Pass Transistor Logic (CPL), Double Pass Transistor Logic (DPL) and Dual Value Logic (DVL). These methods were general and can be extended to synthesize any pass-transistor network which consumed more power. In this project, Complementary Pass Transistor logic is used which contains only NMOS transistor to design 2-4 Decoder circuits. Decoder based CPL is used to design low power memories. Usage of memories is to store the information and it is one of the intermediate of processor and external interface. Since CPL is being used, the power is reduced. CPL based decoder for memories is designed and its performance metrics of high speed and low power is analyzed using MICROWIND 3.1 Tool. The proposed design of CPL is to reduce the transistor count and also achieve the Power, area and delay performance.**

Index Terms – Pass Transistor Logic, CPL, Decoder, Memories.

1. INTRODUCTION

1.1 PASS TRANSITOR CIRCUIT

In conventional logic families input is applied to gate terminal of transistor but in PTL it is applied to source/drain terminal. Here the width of PMOS is taken equal to NMOS so that both transistors can pass the signal simultaneously in parallel. Signal degradation occurs in pass transistor logic. The main advantages of pass transistor are fewer devices to implement the logical functions as compared to CMOS.

When control signal g=1 and input s=0 then we get d=0. If the input s=1 then we get degraded output d. Thus, NMOS pass transistor is called Poor 1 and good 0 switches. The diagram is shown in fig 1.1.

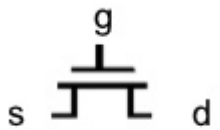

Figure 1.1 NMOS Pass Transistor Logic

When control signal g=0 and input s=0 then we get degraded output d. If the input s=1 then we get d=1. Thus, PMOS pass transistor is called Poor 0 and good 1 switch the diagram is shown in fig 1.2.

Figure 1.2 PMOS Pass Transistor Logic

1.2 DECODER

The encoders and decoders play an essential role in digital electronics, encoders & decoders are used to convert data from one form to another form. These are frequently used in communication system such as telecommunication, networking, to transfer data from one end to the other end. Similarly, in the digital domain, for easy transmission of data, it is often encrypted or placed within codes, and then transmitted. At the receiver, the coded data is decrypted or gathered from the code and is processed in order to be displayed or given to the load accordingly.

The decoder is an electronic device that is used to convert digital signal to an analogue signal. It allows single input line and produces multiple output lines. The decoder allows N- inputs and generates 2 power N-numbers of outputs. For example, if we give 2 inputs that will produce 4 outputs by using 4 by 2 decoder.

1.3 MEMORIES

Memory is the process in which information is encoded, stored, and retrieved. Encoding allows information from the outside world to be sensed in the form of chemical and physical stimuli. In this first stage the information must be changed so that it may be put into the encoding process. Storage is the second memory stage or process. This entails that information is maintained over periods of time. Finally the third process is the retrieval of information that has been stored. Read-only memory (ROM) is a type of non-volatile memory used in computers and other electronic devices. Basic ROM structure is shown in fig 1.3.

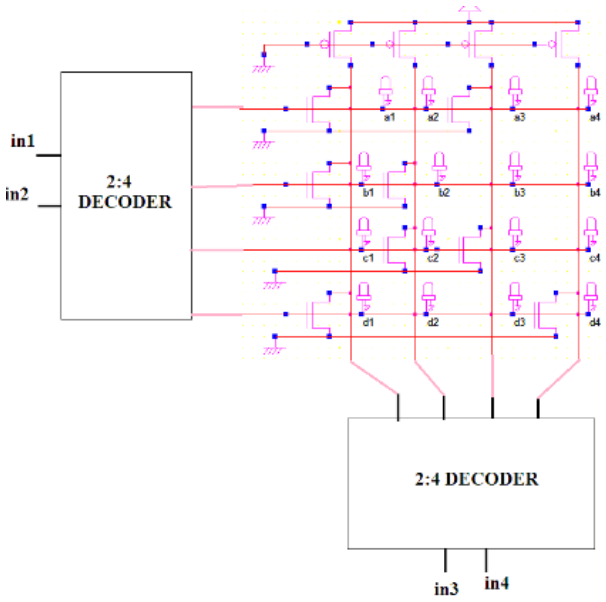

Figure1.3 Basic diagram of 4*4 ROM

2. COMPLEMENTARY PASS TRANSISTOR LOGIC

Complementary pass-transistor logic consists of complementary inputs/outputs, a NMOS pass-transistor network, and CMOS output inverters. The circuit function is implemented as a tree consisting of pull-down and pull-up branches. Since the threshold voltage drop of NMOS transistor degrades the "high" level of pass-transistor output nodes, the output signals are restored by CMOS inverters. CPL has traditionally been applied to the arithmetic building blocks and result in high-speed operation due to its low input capacitance and reduced transistor count.

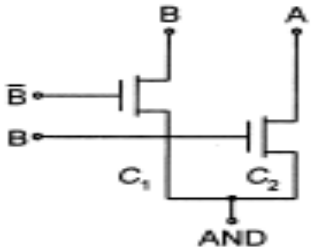

Figure 2.1 Circuit realization of two input AND function in CPL

In the fig 2.1, When B is "1", top device turns on and copies the input A to output F. When B is low, bottom device turns on and passes a "0".The advantage of CPL is fewer devices to implement some functions. The use of CPL as more power efficient than conventional CMOS design. However, new comparisons performed on more efficient CMOS circuit realizations and demonstrate CPL to be superior to conventional CMOS in most cases with respect to speed, area and power-delay products. This is basically explained by the fact that CPL gates uses less transistors, have smaller capacitances and faster than gates in complementary CMOS.

The advantage of high functionally with few pass transistors and of small input capacitances in the CPL style and less wiring overhead makes its better choice. CMOS is good in reliability, but on the other side CPL has the benefits of hardware reduction having lesser number of transistors. Thus CPL reduces the circuit delay and less number of components reduces the area and power consumption of the circuit.

3. DECODER

Decoders can detect a code and activate a single output to signal the presence of that code. Decoders have many applications, from producing system alerts in alarm systems to performing the task of driving multiple devices in microprocessor systems (e.g. memory). A device (or) program that translates encoded data into its original format (e.g., it decodes the data). The term is often used in reference to MPEG-2 Video and Sound data, which must be decoded before its output. Most DVD players, for e.g., include a decoder card whose sole function is to decode MPEG data. It is also possible to decode MPEG data in software, but this requires a powerful microprocessor.

3.1 Basis of 2-4 Decoders

Let's say we have N inputs to a decoder, the number of outputs will be equal to 2^N. Thus there will be one line at the output for each possible input. The encoders and decoders are designed with logic gates such as AND gate. There are different types of decoders like 4, 8, and 16 decoders and the truth table of decoder depends upon a particular decoder chosen by the user. The subsequent description is about a 4-bit decoder and its truth table. The four bit decoder allows only four outputs such as Y0, Y1, Y2 and Y3 and generates two outputs A, B, as shown the table 3.1.

TABLE 3.1 Truth table of 2-to-4 decoder

A	B	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

In this example, you can notice that, each output of the decoder is actually a minterm, resulting from a certain inputs combination, that is:

Y0 =A'B', (minterm m0) which corresponds to input 00

Y1 =A'B, (minterm m1) which corresponds to input 01

Y2 =AB', (minterm m2) which corresponds to input 10

Y3 =AB, (minterm m3) which corresponds to input 11

Similarly, it is done for 3 to 8, 4 to 16 and so on.

4. PROPOSED DESIGN OF CPL LOGIC 2-4 DECODER FOR ROM MEMORIES.

CPL logic for 2 to 4 decoder is implemented in 4*4 ROM memories. Dynamic logic is used instead of pseudo NMOS logic. Clock signal is being connected to all PMOS circuits. Only during the negative edge of the clock pulse PMOS will be active. As a result of which the power is minimized. The proposed CPL for 2*4 decoder implemented in 4*4 ROM memories is shown in the figure 4.1

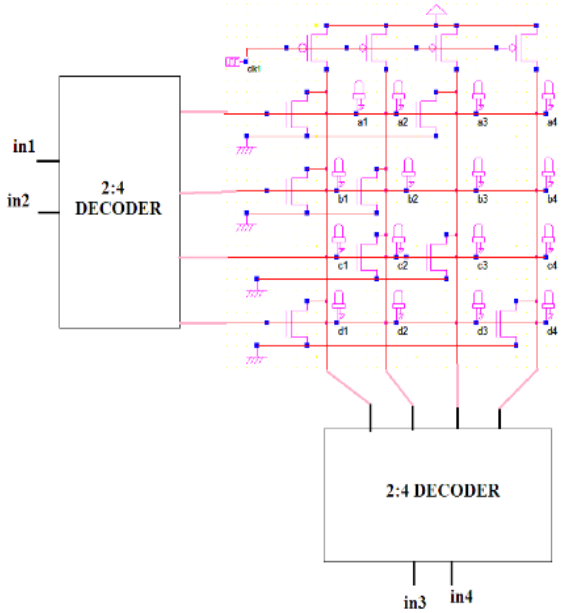

Figure 4.1 4*4 Read Only Memory.

The simulation results of existing and proposed design of 4*4 ROM memories are shown in the figure 4.2 & 4.3 respectively.

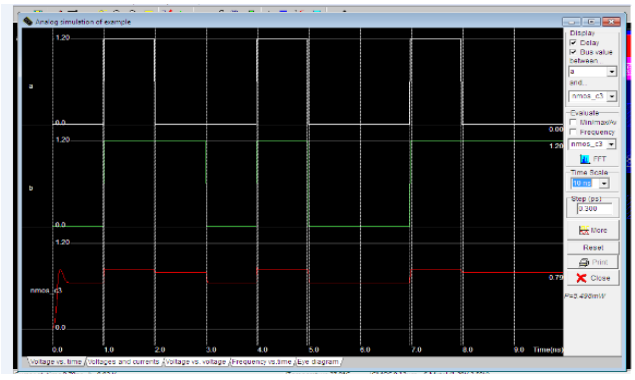

Figure 4.2 Existing design of 4*4 ROM memories

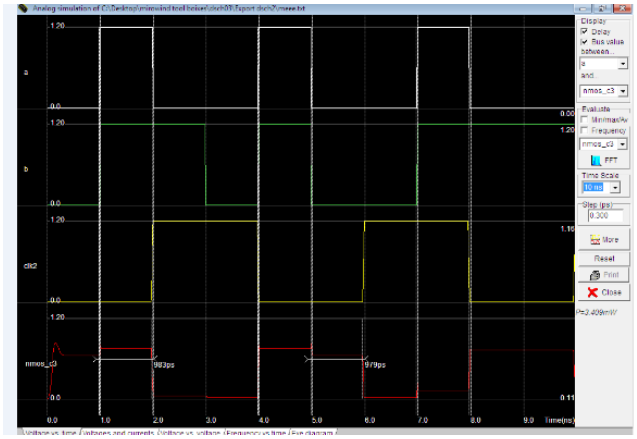

Figure 4.3 Proposed design of 4*4 ROM memories

The comparison of Existing and Proposed Design of 4*4 ROM Memories is shown in the table 4.1.

Table 4.1 POWER COMPARISON

ROM MEMORIES	COMPUTED POWER
Existing design of 4*4 ROM memory	5.498mw
Proposed design of 4*4 ROM memory	3.409mw

5. CONCLUSION

New logic CMOS families using Pass Transistors Circuit techniques have been recently proposed with the objective of improving speed and power consumption. In this paper, CPL for 2-4 decoder has been developed and implemented in ROM memories which minimizes the number of transistor and yet preserves the speed of the logic and also achieves the power performance.

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