Design of Optimized Digital Logic Circuits Using FinFET

M. MUTHUSELVI
Department of ECE
Jayaraj Annapackiam CSI College of Engineering
Nazareth-628617
muthuselvi.m93@gmail.com

R. MARIAAMUTHA
Department of ECE
Jayaraj Annapackiam CSI College of Engineering
Nazareth-628617
maria.amutha@gmail.com

C.MUTHUKUMARI
Department of ECE
Jayaraj Annapackiam CSI College of Engineering
Nazareth-628617
muthukumari.ece@gmail.com

J. MENICK JERLINE
Department of ECE
Jayaraj Annapackiam CSI College of Engineering
Nazareth-628617
jerlin30@gmail.com,

I. BLESSING MESHACH DASON
Department of ECE
Jayaraj Annapackiam CSI College of Engineering
Nazareth-628617
blessingmeshach@gmail.com.

Abstract-**In this paper a novel technique is used to reduce the short channel effects (SCEs) of CMOS. As technology scales down FinFETs will substitute bulk CMOS. FinFET achieves improved SCE, frequency and reduced power consumption and delay. In this work we have realized NAND logic design styles of Double Gate FinFET in 50nm technology and have analyzed various parameters like power, frequency, area and delay. We have compared the CMOS NAND with the four logic design styles of Double Gate NAND. Results show that power dissipation and area occupied is the least in LP mode logic design style. SG mode logic style has greater delay advantage over other logic styles. Optimal logic design style can be chosen according to the need.**

Keywords: Fin Shaped Field Effect Transistor (FinFET); Short Channel Effect (SCE).

1. Introduction

As the size of transistors scale down, so have many digital applications. Mobiles, laptops and many other applications are reduced in size over last decades and became more portable. As the chip density and operating frequency increases, power dissipation in portable devices has become a major concern. Even for non-portable devices, power consumption is important because of potential reliability problems. Due to diminishing device electrostatics CMOS suffers from scalability in sub 70nm which results in Short Channel Effect [1]. Primary complications to the scaling of bulk CMOS include sub threshold leakage, gate-dielectric leakage, device-to-device variations and I_{ON}/I_{OFF} ratio. It is expected that the use of FinFET will provide better control of Short Channel Effects, lower leakage and better yield in aggressively scaled CMOS process [2]. Therefore, at the process level, FinFETs are the promising alternative to conventional bulk MOSFET for CMOS technology. This paper explores how logic design styles based on FinFET, an emerging ransistor technology that is likely to supplement or supplant bulk CMOS at 70nm and beyond, offers less power dissipation and high frequency. Section II explains the structure of FinFET which gives expressions for channel length and width. Section III explains the logic design styles of CMOS NAND and Double Gate NAND. Section IV analyses the various parameters associated with the logic styles. Finally we conclude in Section V.

2. Device Structure

Double-Gate Field Effect Transistor (DGFET) is more versatile than traditional single-gate field effect transistors because it has two gates that can be controlled independently [3], [5]. The structure of FinFET is shown in Fig. 1. Where H_{fin} and T_{fin} are the fin height and thickness respectively, L_{gate} is the length of the gate, L_{ext} is the extended source or drain region. FinFET is like a FET, but Channel has been turned on its edge and made to stand up.

Effective channel length $L_{eff} = L_{gate}+2\times L_{ext}$
Effective channel width $W_{eff}= T_{fin}+2\times H_{fin}$

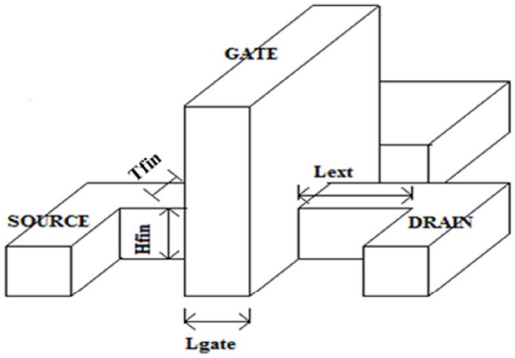


Fig. 1. FinFET Structure.

FinFET device consists of a thin silicon body, the thickness of which is denoted by T_{Si}, wrapped by gate electrodes. FinFET has confined channel which is surrounded by SiO_2 [6]. The thickness of the fin is equal to half of the channel length. The current flows parallel to the wafer plane, whereas the channel is formed perpendicular to the plane of the wafer. Due to this reason, the device is termed quasi-planar. The independent control of the front and back gates of the FinFET is achieved by etching away the gate electrode at the top of the channel. The effective gate width of a FinFET is 2×n×h, where n is the number of fins and h is the fin height. As the width of the channel increases, the current and the load capacitance increase making the delay invariant [7].

3. FinFET Logic Styles

In this paper, comparison of various parameters between an ordinary two-input CMOS NAND and Double Gate MOS two-input NAND are presented.

3.1 *CMOS NAND Gate*

A two-input CMOS NAND gate is implemented by placing two NMOS in series and two PMOS in parallel with inputs (A, B) and output (Out). The output is low when the two inputs are high. Here the channel is controlled by a single gate which is input to FET. The schematic for CMOS NAND is shown in Fig. 2.

3.2 *Double Gate NAND*

In Double Gate NAND four logic styles are available namely SG, IG, LP, IG/LP.

3.2.1 *Shorted Gate (SG) mode*

The shorted-gate (SG) mode FinFETs style is implemented by tying both gates, which leads to a three terminal device, achieving high current drive. It also eventually decrease transistor delay by applying high voltage to both gates of N-FinFETs and can have low leakage current with increase in threshold voltage of the front gate by back gate when both transistors are grounded. The SG – mode NAND gate can be obtained by directly translating the CMOS NAND design to FinFETs, while retaining the same size. The schematic for SG mode NAND is shown in Fig. 3.

3.2.1 *Independent Gate (IG) mode*

In independent-gate (IG) FinFET mode, the top part of the gate is etched out, giving way to two independent gates. Independent signals are used to drive the two device gates, hence the two independent gates can be controlled separately and it offers more design options. The back gate can be used independently as an input to reduce the number of transistors needed to implement numerous logic functions. This can be designed to have asymmetric rise and fall delays because only one transistor gate is used to pull-up but this can lead to large disparities under conditions of greater load. This may reduce the number of transistors [1]. The schematic for IG mode NAND is shown in Fig. 4.

3.2.3 *Low Power (LP) mode*

In this mode back-gate is tied to a reverse-bias voltage to reduce sub-threshold leakage, leakage power and the drive strength of every FinFET. A low voltage to n-type FinFET and high voltage to p-type FinFET is applied. This varies the threshold voltage of the devices, which reduces the leakage power dissipation at the cost of increased delay. The schematic for LP mode NAND is shown in Fig. 5.

3.2.4 *Hybrid (IG/LP) mode*

Hybrid (IG/LP) mode is a combination of LP and IG mode. Unlike the IG design, delays are balanced by reducing the strength of the complimentary series structure. This can be achieved by tying the back gates of FinFETs in series to a strong reverse bias [4]. The schematic for IG/LP is shown in Fig. 6.

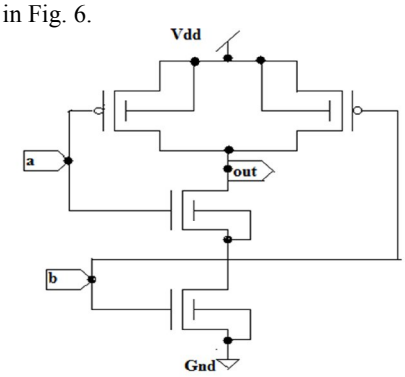


Fig. 2. CMOS NAND schematic

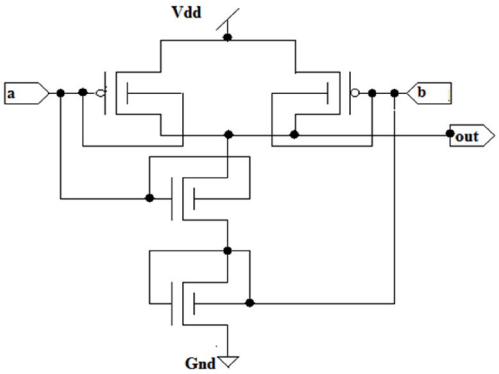


Fig. 3. SG mode NAND schematic

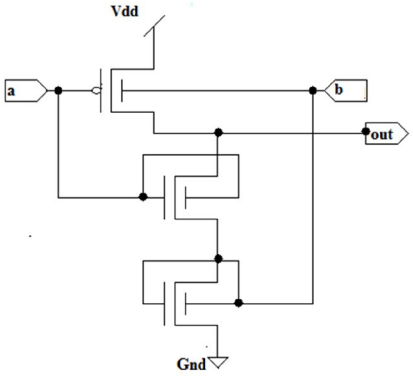


Fig. 4. IG mode NAND schematic

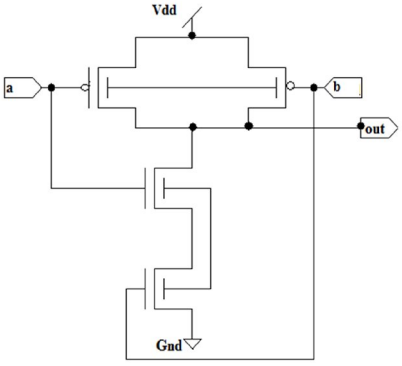


Fig. 5. LP mode NAND schematic

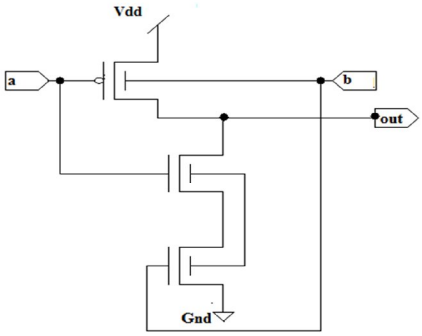


Fig. 6. Hybrid mode schematic

4. Simulation Results

The layout design of FinFET and ordinary CMOS were constructed using Microwind 3.0c tool, with 50nm foundry. Various parameters like power dissipation, frequency, area and delay were analyzed. The supply voltage is applied from 0.5V to 2.5V for various FinFET based NAND gate logic styles and also for the ordinary CMOS NAND gate. The layout simulated is shown from Fig. 6 to Fig. 10. Table 1 shows the power dissipation values of ordinary CMOS and the logic design styles of FinFET. These values are plotted in Graph 1. We observe that the power dissipation (μW) is less in the FinFETs logic design styles compared to ordinary bulk CMOS. Table 2 gives frequency and area of CMOS NAND and FinFETs logic. These values are plotted in Graph 2. We can observe that all the devices lie in the frequency range of 1000MHz-2510MHz with SG mode having the highest operating frequency. In Table 3 the fall time, rise time and average delay of all the devices are shown. These values are plotted in Graph 3.

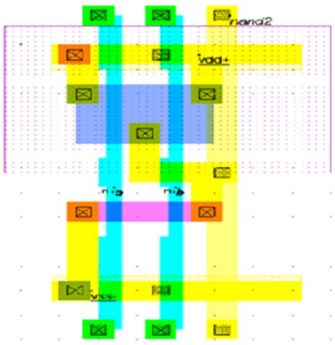


Fig. 6. CMOS NAND layout

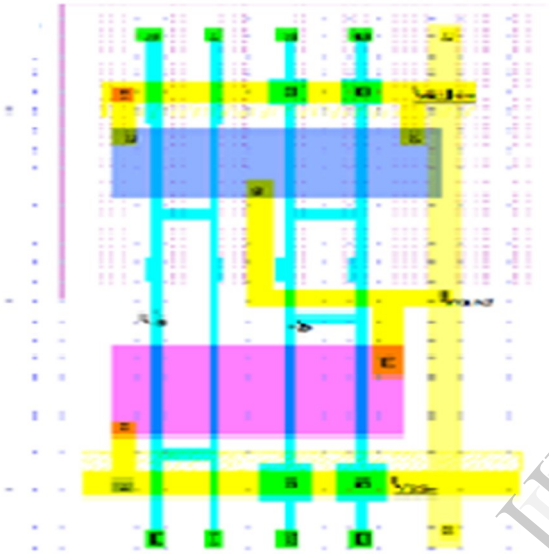


Fig. 7. SG mode layout

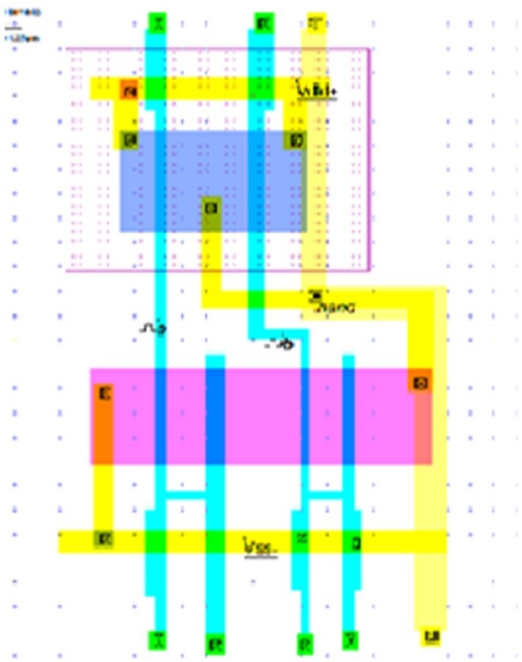


Fig. 8. IG mode layout

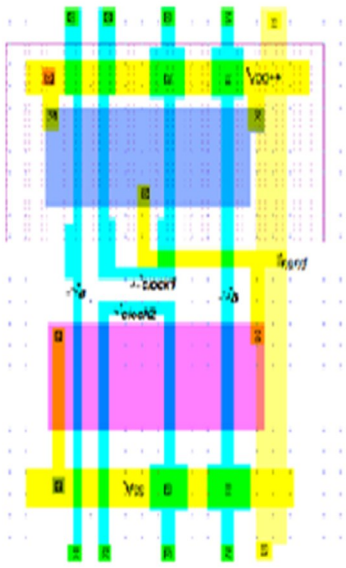


Fig. 9. LP mode layout

Design Mode	Fall Delay (ps)	Rise Delay (ps)	Average Delay (ps)
CMOS	7	4	5.5
SG	10	4	7.0
IG	11	4	7.5
LP	5	2	3.5
IG/LP	9	6	7.5

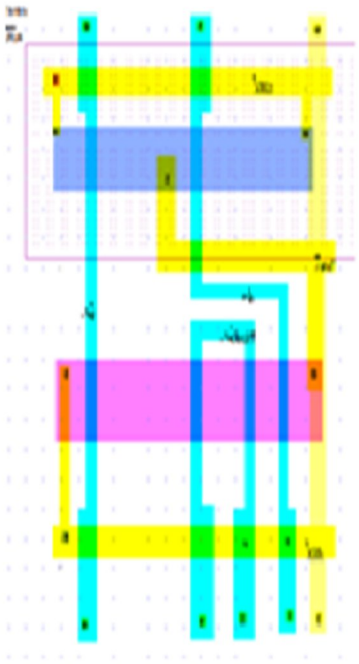


Fig. 10. IG/LP mode layout

Table 1. Power Dissipation for CMOS NAND and four modes of FinFET

V_{DD} (V)	CMOS NAND (µW)	SG Mode (µW)	IG Mode (µW)	LP Mode (µW)	IG/LP mode (µW)
0.5	0.17	7.34	9.84	0.28	0.75
1.2	19.88	0.16	0.12	4.45	9.94
1.5	20.03	0.14	13.99	5.44	12.79
1.8	20.18	53.85	18.46	7.34	16.67
2.0	20.28	74.42	23.25	9.61	20.28
2.5	20.53	204	176	115	110

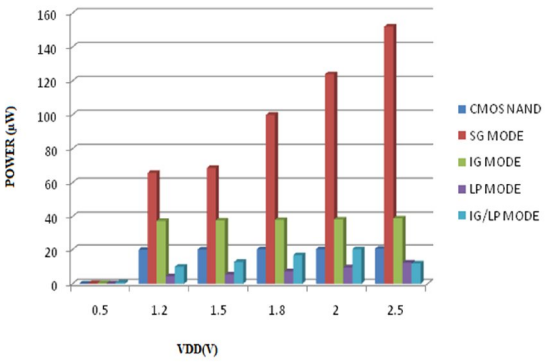
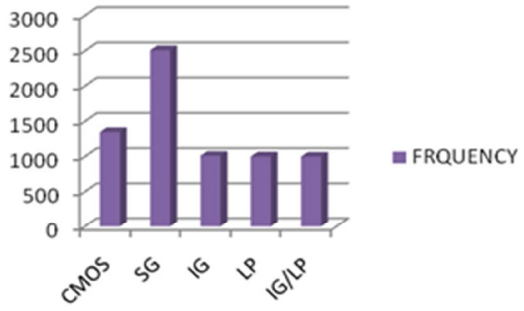
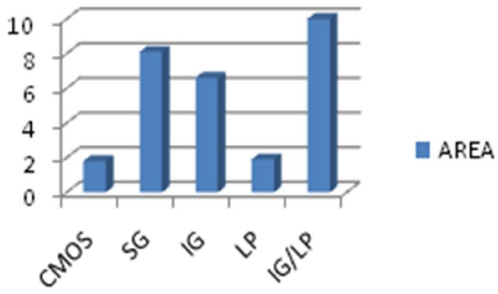


Table 2. Frequency and Area for CMOS NAND and four modes of FinFET



Graph 1. Frequency for different styles of FinFET



Graph 2. Area occupied by different modes of FinFET

5. Conclusion

We have compared the various logic design styles in FinFET by measuring the parameters such as power dissipation, frequency, area and delay. The simulation of various modes of FinFET with two input NAND logic design shows that, SG mode has the lower delay of 3.50ps than CMOS of 5.50ps also LP mode consumes low power of 0.281µm than CMOS of 0.174µm. LP mode occupies the same area as CMOS. The operating frequency of these devices ranges between 1000MHz to 2510MHz.

Design Mode	Frequency(MHz)	Area(μm^2)
CMOS	1348	1.8
SG	2510	8.1
IG	1012	6.6
LP	1002	1.9
IG/LP	1000	24.8

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