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Design of Octal to Binary Encoder using QCA

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***Abstract* -Advancements in the field of science and technology imparts the world to become smarter and scaling the hardware to a nano scale. This is being employed in the stream of applications regarding the design and fabrication of CMOS transistors per square centimetre. Several researches are on-going to reduce the CMOS technological applications to a smaller scale i.e., up to nano scale. In this drive this scaling is being made possible in this field with the evolution of quantum dots which has further lead to the concept of quantum dot cellular automata (QCA) from the knowledge of it. This paper presents the fundamental concepts regarding QCA which may also include basic cell and its types, majority gate, types and its usage, inverter and its type, clocking criteria. This paper proposes a design of octal to binary encoder with minimum possible crossovers consisting of nine (3 input) majority gates with 211 cells employing all the fundamental concepts discussed and its simulation results using related QCA designer tool.**

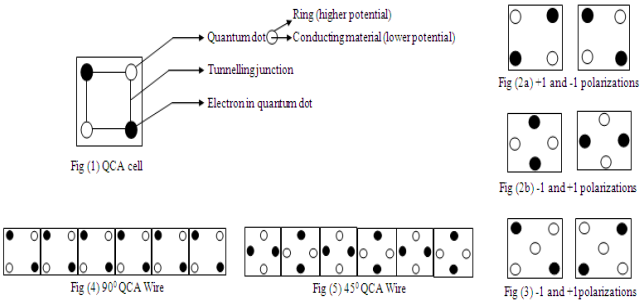
***Keywords-.Quantum dots, Quantum dot cellular automata, octal to binary encoder, QCA designer tool*.**

I. INTRODUCTION

Quantum dot Cellular Automata (QCA) was introduced by Lent *et al.,* [1] from University of Notre Dame in 1993.Researchers are being employed in the recent years voluminously in the field of CMOS technology for the future generation IC's out of which, one of the emerging technologies is QCA. Moreover this technology yielded a solution not only in the parameters regarding the scaling of size but also towards the power consumption reduction and the complexity of designing with multiple types of components. The computation is also based on the new method of computation and transformation of information. The power and principle of computation is based on the simple physical concept of columbic forces of interaction (repulsion and attraction) between the electrons in the QCA cells. Generally the transfer of information [5] takes place through the flow of charge that is by the movement of electrons. But in this technology it encodes the information (binary) in the configuration of the charge within the cells of QCA. It is new emerging architecture which transfers information only through the interaction between the cells. As there is no flow of charge [16] , there will be no flow of current between the cells and no voltage exists across the cells and no power or information is transferred or delivered within the individual internal cells. So the transfer of information is not by the transport of electrons but by the adjustment or re arrangement of electrons in a limited particular area that too in a nano scale i.e., of only a few square nano metres which are antithesis to electronics based upon transistors. QCA is conventional and studied to accomplish the parameters like consumption of low power, fast switching speeds, increase in the device density and eliminating the parameters concerning the thermal effect(overheating), scaling of size and performance of the device. The paper is organised as follows: section II describes briefly the fundamental concepts of QCA technological terms that includes four dot QCA cell, five dot QCA cell, majority gate and implementing AND, OR gates in it, QCA inverter and its reduced form, QCA crossovers and its types and concepts related to QCA clocking. Section III presents design and its simulation results of proposed octal to binary encoder along with its truth table and output logic functions. Conclusion is being stated in section IV.

II. FUNDAMENTAL CONCEPTS OF QCA

Based on the principle of the functioning of QCA i.e., to actualize a system that encrypts information from the knowledge of rearrangements of electron it is expedient to assemble a vessel in which the electron can be cornered



and counted as there or not there. A quantum dot capacitated this by constructing a region of low potential circumscribed by an arena or a brim of high potential. These brims of high potentials are known as potential wells which are capable to trap electrons of corresponding low energies/temperature. So these quantum dots are fabricated by establishing an enclave of conducting material surrounded by the brim of insulating material.

A. Four dot QCA cell

QCA cells are quadratic cells [2] that consists of four number of such quantum dots which are positioned to the four corners of the square. Each cell possess two number of electrons(mobile) which are able to adjust by the tunnelling among the peer quantum dots in the cell as depicted in figure(1). The tunnelling junction enables the tunnelling process which takes place only in a single cell but not between the cells. Electrons that are present in the quantum dots are cornered till they acquire required high potential to escape and tunnel from one dot to another dot. The two electrons inside the QCA cell tend to get placed to the antipodean dots i.e., the two electrons get adjusted or rearranged to the diametric dots in the cell by tunnelling due to the columbic forces of repulsions between the electrons. These cells are of two types namely 90^0 and45^0 respectively. Thus the cells attain the polarizations of +1 and -1as shown in the figure(2a) and figure (2b) respectively based on their diametric placements [13] . The polarization of the cell [3] is being defined as the extent up to which the charge distribution is arranged between any of the axes is represented in equation (1).

$$P = \frac{(\rho_2 + \rho_4) - (\rho_1 + \rho_3)}{(\rho_1 + \rho_2 + \rho_3 + \rho_4)} - (1)$$

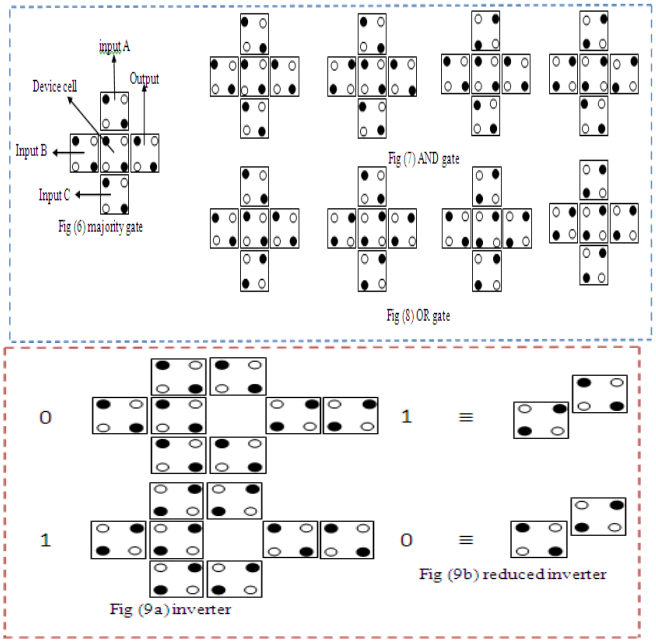
Where , $\rho_i$denotes the electronic charge at dot

B. Five dot QCA cell

This cell is also a two state QCA cell similar to the four dot cell but it is a wireless two state QCA cell [1] by Lent and Porode at Notre Dame. This five dot QCA cell is depicted in figure (3). In this type of cell tunnelling junctions are absent since it is employs wireless computations.

C. QCA wire

The information is being transmitted through these wires of certain length formed by the array of the QCA cells. These QCA wires are of two types namely 90^0wires and 45^0wiresas depicted in figure (4) and figure (5) respectively. In the 90^0wire all the cells of same polarization are being arranged and in 45^0 wire the cells of both the polarizations are to be arranged in an alternative manner. The information [2] that transmits in this type of wire will be as it is or gets inverted depending upon the number of cells arranged in the wire.



D. QCA majority gate

The basic structure of the 3-input majority gate using QCA cells is depicted in figure (6). It consists of five cells of them three are input cells, one output cell and a device cell which is located at the centre. The device cell [2] gets polarized based on the maximum surrounding cells polarization and hence it is also named as majority voter. AND, OR gate outputs are obtained from the knowledge of the majority gate itself. If any of the three inputs of the majority gate is fixed to +1 or -1 polarizations then the majority gate acts as OR, AND gates respectively. The results for these gates are being verified as depicted in figure(7) and figure(8).The basic 5-input majority gate from the QCA cells is also present where it uses eighteen number of QCA cells. In this gate also AND, OR operations are being performed by using the 3-d QCA cell the 5-input majority gate can be reduced to only seven QCA cells.

D. Inverter (NOT gate)

The basic structure to implement inverter using QCA is depicted in figure (9a).Also by making translations in the QCA cells the inverter [1] can be further reduced to only two numbers of cells as depicted in figure(9b).Another basic structure i.e., fan-out type of interconnection in QCA cells is depicted in figure (10).

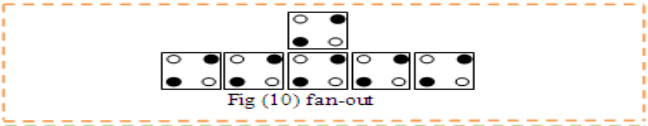


Fig (10) fan-out

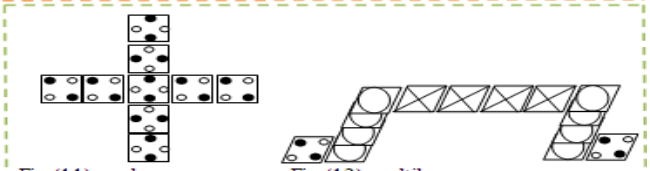


Fig (11) coplanar crossover Fig (12) multilayer crossover

E. QCA crossovers

Sometimes there may be a need to interconnection between one block of cells with another block. This is made possible with the concept of crossovers in QCA. These crossovers [5] are categorized in two ways namely coplanar crossing and multilayer crossing. Coplanar crossing is being employed only in a single layer where both 90° and 45° QCA cells are used which is depicted in figure (11). These wires are placed perpendicular to each other. This type of crossover does not exist in the conventional CMOS circuit designs. Multilayer crossing is being employed with three layers to interconnect between the cells where only a single type of cells are being used which is depicted in figure(12). This type of crossovers is easy to handle and understand but the fabrication of this type of crossover is not still in practice. But the usage of multilayer crossover yields the best results because coplanar crossovers may be very sensitive to the surrounding variations in the QCA cells. The bottom most layer is considered as main layer and the next layer is labelled as layer 1 and the successive as layer 2 and so on respectively.

F.QCA clocking

QCA clocking zones enables to convert the design of the device from parallel data lines in to serial DataStream. QCA methodology does not possess any particular control insisted on the system. The main purpose of clocking is to assign this control over the entire system which is divided into four clock zones namely clock 0, clock 1, clock 2 and clock 3 respectively. Here the external control in the sense it regards the control over potential wells of QCA cells. These four clocking zones of QCA are at a rate of 90° phase shift (out of phase) with each other. The four clock zones are switch, hold, release and relax phases where all the four corresponds to a one complete cycle and get refreshed after one complete cycle as depicted in figure(13). In the switch phase the inter-dot potential barrier is raised in a gradual manner. In hold phase the inter-dot potential barrier is placed at highest possible level by reducing the tunnelling of electrons in a gradual manner. In relax and release phases the inter-dot potential barriers are being reduced to its possible lowest state in a gradual manner where the cells remain un-polarized. However the polarization of the QCA. cell is being determined when they are in switch and hold phases only which are attained by the polarizations of the neighbours. So the remaining cells in QCA that are in release and relax phases are un polarized and they do not have any responsibility or effect in determining the QCA cell. state. In majority gate all the inputs are given to the same clock [4] so that all the inputs are applied to the gate at the same delay. The device cell and the output are allotted to the next successive clock. To avoid distortions and to gain exact outputs for the design at least two number of cells present in each clocking zone [15] individually that may be either a majority gate or inverter and for all other arrangements of QCA cells. It is very easy to allot clocking

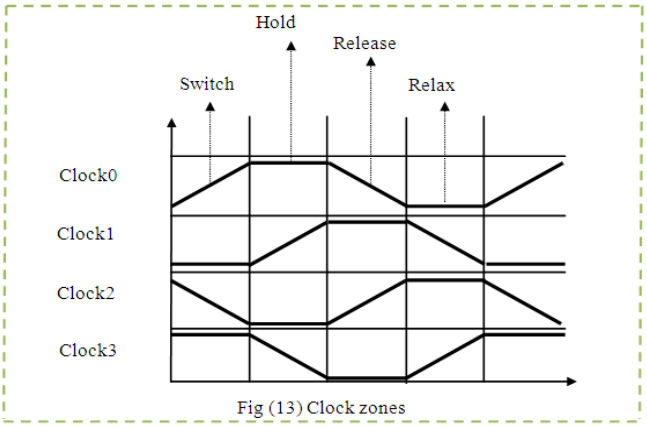


Fig (13) Clock zones

Octal to binary encoder

Octal input		Binary output		
		A_2	A_1	A_0
D_0	0	0	0	0
D_1	1	0	0	1
D_2	2	0	1	0
D_3	3	0	1	1
D_4	4	1	0	0
D_5	5	1	0	1
D_6	6	1	1	0
D_7	7	1	1	1

Fig (14) Truth table

zones for a forward design circuits that may a combinational logic design but it is very difficult to allot clocking zones for the design of the conventional sequential logics due to the existence of feedback in the designing. Apart from the majority gate in an inverter all the cells before the c shaped structure which is the beginning of the structure should be allotted to the same clock as that of the input clock. The entire C shaped block of QCA cells should be allotted to the successive clock of the input and the output should be in the subsequent clock of the C shaped structure. There is no constraint about the maximum number of cells in the individual clocking zone apart from the parameter i.e., radius of effect but the maximum number of QCA cells that can be allotted to the individual clocking zone is up to 12 to 14 without noise in that area.

III. DESIGN OF OCTAL TO BINARY ENCODER

A. Design

In an octal to binary encoder it consists of eight possible combinations of octal inputs namely D_0, D_1, D_2, D_3, D_4, D_5, D_6, and D_7 respectively. And the output of the encoder gives the binary digits namely A_0, A_1, A_2 respectively. The truth table is depicted in figure (14) and the output logic functions in equations (2,3 & 4).

$$A_2 = D_4 + D_5 + D_6 + D_7 \quad -(2)$$

$$A_1 = D_2 + D_3 + D_6 + D_7 \quad -(3)$$

$$A_0 = D_1 + D_3 + D_5 + D_7 \quad -(4)$$

D_0 is not present in any of the equations since D_0 is a don't care case.

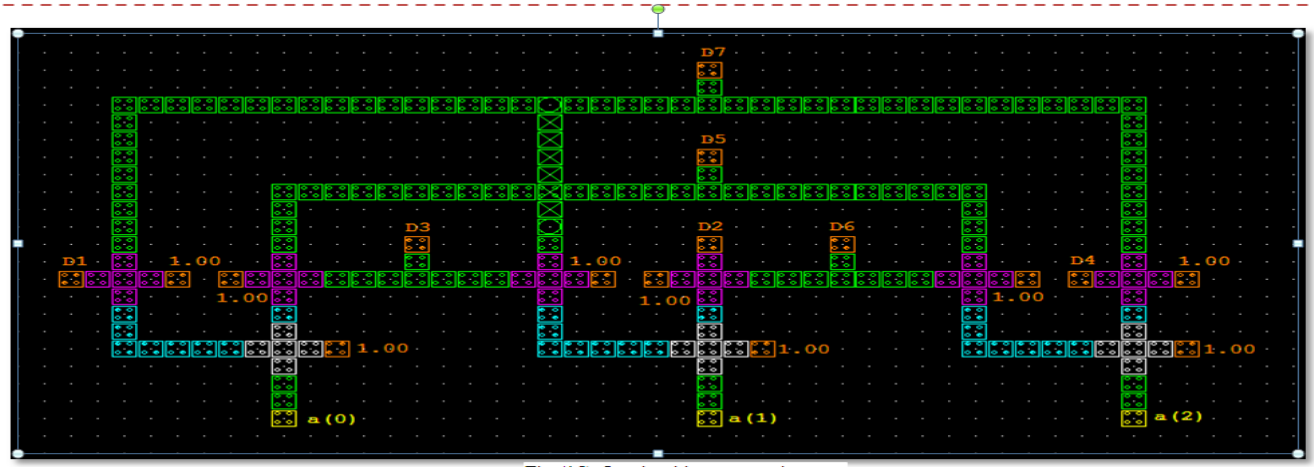


Fig (15) Octal to binary encoder

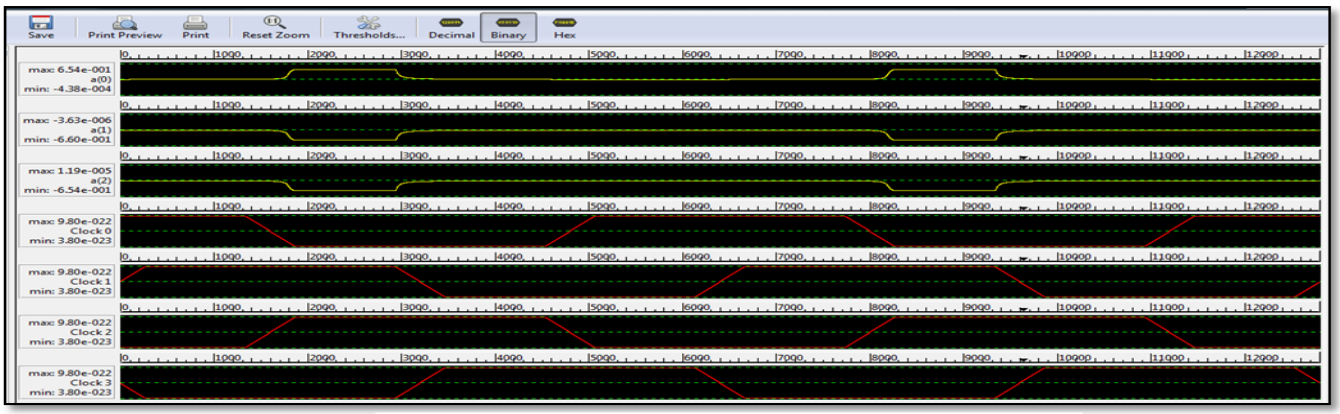


Fig (16) Simulation results for octal to binary encoder

From the output logic functions the input D_7 is common to all the three outputs. Similarly D_3 is common to A_0 and A_1, D_5 is common to A_0 and A_2, D_6 is common to A_1 and A_2 respectively. Remaining all the inputs are applied individual.

-

The design of octal to binary encoder in QCA designer tool is depicted in figure (15). In this proposed design only one crossover is constructed employing multilayer cross over consisting of 4 layers in total labelled as main cell layer, via 1, via 2 and top layer respectively so that no distortion occurs in the waveform simulations.

B. Simulation results

The simulations results obtained for the designed octal to binary encoder using QCA is depicted in figure(16).These results are related to the D_1 input which is fixed to +1 polarization yielded binary output as 001 in the simulation results which are labelled as , A_2, A_1 and A_0 respectively when the remaining inputs are fixed to -1 polarization

Similarly all the outputs are obtained in the same way by giving the all the possible combinations of octal digits as inputs to the proposed design with allotment of appropriate clocking zones, radius of effects in the QCA designer tool

IV. CONCLUSION

QCA is being emerged as an alternative to the CMOS technology achieving miniaturization, low power and speed switching speeds. QCA design can be build from the logic functions of the digital design i.e., boolean functions which are to be scaled to obtain the majority functions [12] used in QCA. This paper has a reveals all the fundamental concepts of QCA technology that includes majority gate (three input) along with the sketches related to the verification of AND, OR logics from the majority gate, basic QCA inverter and its reduced form which made

possible with the implementation of NAND, NOR gates with only six number of cells that can be achieved by addition of one translated cell to the majority gate and other fundamental structures etc., From the basic knowledge of QCA an octal to binary encoder is designed with minimum number of possible crossovers. These crossovers make the design to avoid latency by employing appropriate clocking to the design and simulated using QCA designer tool and results are obtained with minimum of distortion.

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