Design of Next Generation CPU Card for State of the Art Satellite Control Application

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***Abstract*— On-board Computers (OBC) and Attitude and Orbit Control Electronics (AOCE) developed by CEG, ISAC/ISRO is processor based subsystems of the spacecraft which perform a wide range of critical functions like telecommanding, telemetry and attitude and orbit control.**

After the usage of 16 bit Mil Std 1750 processors which had a performance of up to 1MIPS, the single core LEON3 FT processor is being considered for immediate future projects to gain performance advantages up to 10MIPS.

Dual-core technology combines two independent processors and their respective caches onto a single processor chip. This helps increase system performance so the processor can simultaneously handle multiple threads at a faster rate, helping to reduce lag time when running more than one application. A thread is a single stream of data through the processor. Each application generates its own or multiple threads. A dual-core processor boosts multitasking computing power and improves the throughput of multithreaded applications for our increasing demand. The dual core processor also includes some on chip peripherals devices like Mil-std-1553 BT/RT/MT, UART, CAN, Space wire, Ethernet, PCI, Memory controller, Debug support Unit, 192KiB SRAM, CCSDS Encoder & Decoder, presently which are using as discrete devices along with the processor for operation of the CPU card.

Using this on chip peripherals in the dual core processor we are reducing the space in the board as well as performance enhancement of the systems. To be able to handle the ever increasing requirements of the future as well as to target cycle times of less than 10ms, it is essential to adopt the dual core architecture to achieve performances of up to 50 MIPS or better.

In this paper we will present the design and development of next generation CPU card for advance state of the art Satellite control applications for ISRO's space program.

Keywords*— *LEON 3FT, GR712RC SPARC V8 Processor.

I. INTRODUCTION

It is evident that the developments in the field of processors and technology are enormous. To meet the growing needs of computing power, communication speed and performance requirements demanded by today's applications, processor clock speed has to be increased. However, increasing clock speed is not viable anymore due to heat dissipation and power consumption constraints. Hence instead of trying to increase the clock speed, multi-core processor architectures with the lower frequency can be used. A multi-core processor is a single integrated circuit in which two or more processors have been attached for enhanced performance, reduced power consumption and more efficient simultaneous processing of multiple tasks. A processing system is composed of two or more independent cores. An individual Processor is called as Core. The cores are integrated onto a single integrated circuit die or multiple dies in a single chip package. A multi-core system implements multiprocessing in a single physical package.

LEON is a 32-bit CPU microprocessor core, based on the SPARC-V8 RISC architecture and instruction set. It was originally designed by the European Space Research and Technology Centre, part of the European Space Agency, and after that by Gaisler Research. LEON has a dual license model: A LGPL/GPL FLOSS license that can be used without licensing fee, or a proprietary license that can be purchased for integration in a proprietary product. The core is configurable through VHDL generics, and is used in system-on-a-chip (SOC) designs both in research and commercial settings. The GR712RC device has been designed to provide high processing power by including two LEON3FT 32-bit SPARC V8 processors. GR712RC is based on LEON3FT and IP cores from the GRLIB IP library, implemented with the Ramon RadSafeTM 180 nm cell library on Tower Semiconductors 180nm CMOS process. The fault tolerant design of the processor in combination with the radiation tolerant technology provides total immunity to radiation effects. The power optimized GR712RC is fully software compatible with previous LEON processors, with a performance increase of up to 100 percent at the same clock frequency. Section II gives a brief overview of the processor being used presently in few of the spacecraft applications.

II. EXISTING PROCESSORS

The very first generation of microprocessors developed by ESA had been designed by MEDL in UK, named later GPS, today Dynex Semiconductor. The MA 31750 is a MIL-STD-1750 based processor (an open standard) which had a performance of up to 1MIPS. AT697F is a highly integrated, high-performance 32-bit RISC embedded processor based on the SPARC V8 architecture. Its implementation is based on the European Space Agency LEON2 fault tolerant model. By executing powerful instructions in a single clock cycle, this processor achieves throughputs approaching 1MIPS per MHz.

The Intel 80386 also known as i386 or just 386 is a 32-bit microprocessor. The successor to the Intel 80286 microprocessor. It was the first Intel processor with 32-bit data and address busses called IA-32. With a 33 MHz clock, it can operate at about 11.4 MIPS.

The RAD750 is a radiation-hardened single board computer manufactured by BAE Systems Electronics, Intelligence & Support. The successor of the RAD6000, the RAD750 is for use in high radiation environments experienced on board satellites and spacecraft. It has a core clock of 110 to 200 MHz and can process at 266 MIPS or more.

The single core LEON 3FT processor is being considered for immediate future projects to gain performance advantages up to 10MIPS. The GR-CPCI-UT699 development board has been designed to support development and fast prototyping of systems based on the Aeroflex UT699 32-bit Fault-Tolerant LEON3-FT SPARC V8 Processor which has a core frequencyup to 75MHZ.

III. HARDWARE IMPLEMENTATION

The LEON family of processors was originally designed by the European Space Research and Technology Centre (ESTEC), under the European Space Agency (ESA), in the year 1997, but was later handed out to Gaisler Research. The LEON, high-performance processors were specifically meant for implementation in the European space projects. Gaisler Research is otherwise called Aeroflex Gaisler and is responsible for the design and development of the LEON3 category, which is suitable for system-on-a-chip (SoC) designs. However, the fault tolerant version of LEON, the LEON 3FT aims at providing supports to work in harsh, highly variant space environments. The LEON 3FT is a monolithic, SPARC V8 processor which follows the RISC based Harvard architecture and projects a 7-stage instruction pipeline with a predominant fault-tolerant feature.

The GR712RC device has been designed to provide high processing power by including two LEON3FT 32-bit SPARC V8 processors, each with its own high performance IEEE-754 compliant floating-point-unit and SPARC reference memory management unit. This high processing power is combined with a large number of serial interfaces, ranging from high-speed links for data transfers to low-speed control buses for commanding and status acquisition. The GR712RC can be utilized in symmetric or asymmetric multiprocessing mode. The processors provide hardware support for cache coherency, processor enumeration and interrupt steering. A block diagram of GR712RC architecture is shown in Fig.1. The GR712RC processor has a dual-core SPARC V8 integer unit, each with 7-stage pipeline, 8 register windows, 4x4 KiB multi way instruction cache, 4x4 KiB multi-way data cache, branch prediction, hardware multiplier and divider, power-down mode, hardware watch points, single vector trapping, SPARC reference memory management unit, etc. It consists of EDAC protected (8-bit BCH and 16-bit Reed- Solomon) interface to multiple 8/32-bits PROM/SRAM/SDRAM memory banks, advanced on-chip debug support unit, 192 KiB EDAC protected on-chip memory, Multiple Space Wire links with RMAP target, Redundant 1553 BC/RT/MT interfaces, redundant CAN 2.0 interfaces, 10/100 Ethernet MAC with RMII interface, SPI, I2C, ASCS16 (STR), SLINK interfaces, CCSDS/ECSS Telemetry and telecommand, UARTs, Timers & Watchdog, GPIO ports, Interrupt controllers, status registers, JTAG, etc. and configurable I/O switch matrix. It incorporates a dual-core LEON3-FT SPARC V8 processor and is implemented using Ramon Chips' RadSafeTM library on Tower Semiconductors' standard 180 nm CMOS technology.

The variation in interfaces allows different systems to be implemented using the same device type, which simplifies parts qualification and procurement. It also brings cost reductions to software development since the core functionality can be reused from application to application, only changing the drivers for the interfaces. Due to the high amount of peripherals and a limited number of pins, there is an I/O switch matrix that controls which peripheral is connected to each pin.

The core block diagram of a LEON processor is shown in Fig.2. The GR712RC implements two LEON3FT processor cores in SMP configuration. LEON3FT is a 32-bit processor core conforming to the IEEE-1754 (SPARC V8) architecture. It is designed for embedded applications, combining high performance with low complexity and low power consumption. The LEON3FT core has the following main features: 7-stage pipeline with Harvard architecture, separate instruction and data caches, hardware multiplier and divider, on-chip debug support and multiprocessor extensions.

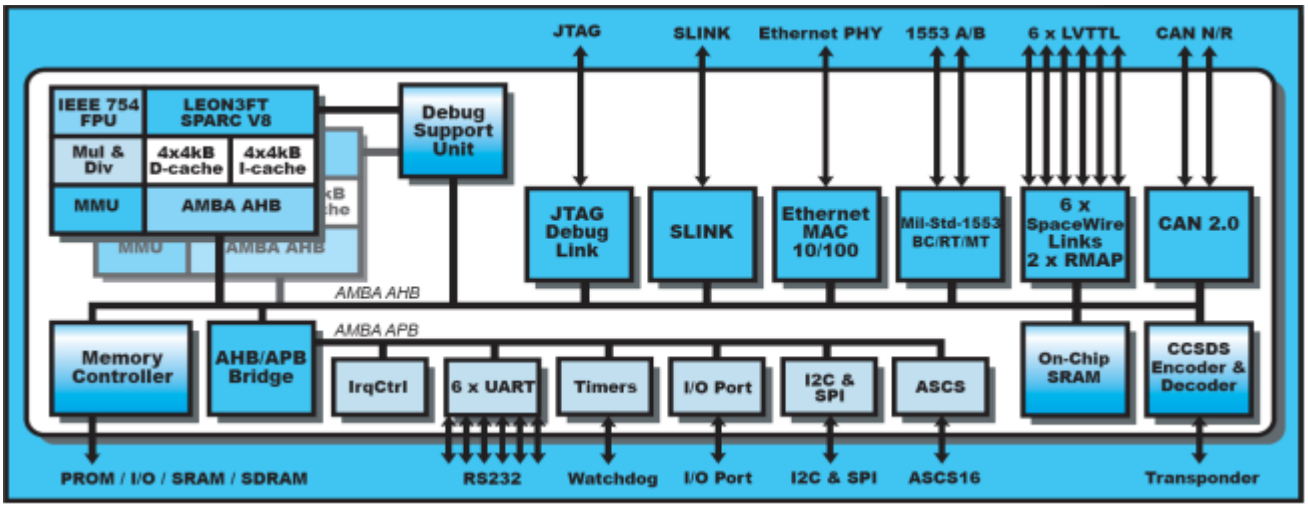

Fig.1, GR712RC block diagram

The Integer unit implements the full SPARC V8 standard including hardware multiply and divide instructions. The number of register windows is 8. The pipeline consists of 7 stages with a separate instruction and data cache interface (Harvard architecture). In the cache sub system each processor is configured with a 16 KiB instruction cache and a 16 KiB data cache. Each LEON3 processor is connected to a unique GRFPU floating-point unit. The GRFPU implements the IEEE-754 floating-point format and supports both single and double-precision operands.

A SPARC V8 Reference Memory Management Unit (SRMMU) is provided per processor. The SRMMU implements the full SPARC V8 MMU specification, and provides mapping between multiple 32-bit virtual address spaces and 32-bit physical memory. The LEON3 pipeline includes functionality to allow non-intrusive debugging on target hardware. Through the JTAG debug support interface, full access to all processor registers and caches is provided. The debug interfaces also allows single stepping, instruction tracing and hardware breakpoint/ watchpoint control.

The GR712RC contains an interrupt controller that support 31 system interrupts, mapped on the 15 processor interrupts. The cache system implements an AMBA AHB master to load and store data to/from the caches. The interface is compliant with the AMBA-2.0 standard. The LEON3 processor core implements a power-down mode, which halts the pipeline and caches until the next interrupt using clock gating. This is an efficient way to minimize power-consumption when the application is idle or when one of the processor cores is not used. LEON3 is designed to be use in multi-processor systems and the GR712RC contains two cores. Each processor has a unique index to allow processor enumeration. The write-through caches and snooping mechanism guarantees memory coherency in shared-memory systems. It contains logic to correct up to 4 bit errors per 32-bit cache word and associated tag. The processor registers are protected by a SEC/DED BCH EDAC.

The GR712RC is housed in a 240-pin ceramic quad-flat pack package (CQFP-240). To fit in this package, some of the on-chip peripheral functions have to share I/O pins. A programmable I/O switch matrix provides access to several I/O units. When an interface is not activated, its pins automatically become general purpose I/O. After reset, all I/O switch matrix pins are defined as I/O until programmed otherwise. The programmable I/O switch matrix consists of 67 pins. The combined 8/32-bit memory controller provides a bridge between external memory and the AHB bus. The memory controller can handle four types of devices: PROM, asynchronous static RAM (SRAM), synchronous dynamic RAM (SDRAM) and memory mapped I/O devices (IO). The PROM, SRAM and SDRAM areas can be EDAC-protected using a (39, 7) BCH code. The BCH code provides single-error correction and double-error detection for each 32-bit memory word. The GR712RC is provided with 192 KiB on-chip RAM, based on the FTAHBRAM core from GRLIB. The RAM is protected with an error detection and correction unit (EDAC), capable of correcting one error per word, and detecting two errors per word.

The on-chip memory is not cacheable. The CCSDS/ECSS/PSS Telemetry Encoder implements part of the Data Link Layer, covering the Protocol Sub-layer and the Frame Synchronization and Coding Sub-layer and part of the Physical Layer of the packet telemetry encoder protocol. The GR712RC contains six UART interfaces for asynchronous serial communications.

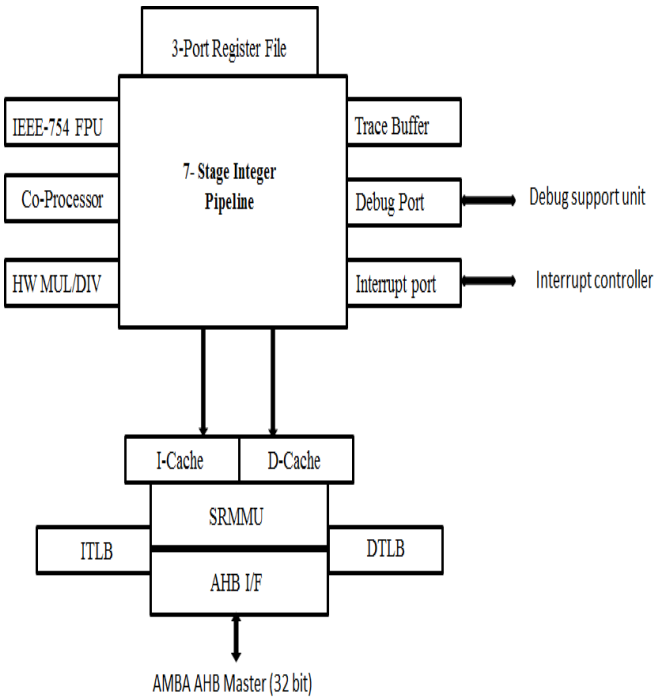

Fig.2, LEON3 processor core block diagram

The UARTs supports data frames with 8 data bits, one optional parity bit and one stop bit. To generate the bit-rate, each UART has a programmable 12-bit clock divider. Two 8-byte FIFOs are used for data transfer between the APB bus and UART. Both odd and even parity is supported. The General Purpose Timer Unit provides a common 16-bit prescaler and four 32-bit decrementing timers. Each timer can generate a unique interrupt on underflow. The I2C-master core is compatible with Philips I2C standard and supports 7- and 10-bit addressing. Standard-mode (100 kb/s) and Fast-mode (400 kb/s) operation are supported directly. External pull-up resistors must be supplied for both bus lines. The SPI controller provides a link between the AMBA APB bus and the Serial Peripheral Interface (SPI) bus. The SPI core is controlled through the APB address space, and can only work as master. The SPI bus parameters are highly configurable via registers, and the controller has configurable word length, bit ordering and clock gap insertion.

The B1553BRM core needs a 24, 20 or 16 MHz clock. The frequency used can be configured through a register in the core. This clock can either be supplied directly to the B1553BRM core through the 1553CK pin, the system clock, or it can be generated through a clock divider that divides the system clock and is programmable through the GPREG. The SDRAM clock (SDCLK) output is driven from the internal system clock. A programmable delay line allows tuning the SDCLK phase relative to the internal clock. The output is tuned to be in phase with the internal clock tree when the

delay line is set to zero. If the system clock is generated by 2x MFDLL, SDCLK is not active when the reset input (RESETN) is asserted. When the system clock is generated directly from INCLK (i.e. when DLLBPN = 0), then SDCLK is driven directly from INCLK. The CCSDS/ECSS/PSS Telemetry Encoder implements part of the Data Link Layer, covering the Protocol Sub-layer and the Frame Synchronization and Coding Sub-layer and part of the Physical Layer of the packet telemetry encoder protocol.

IV. GR712 Based CPU for OBC Card Block Diagram

The design of the CPU system for spacecraft applications is implemented on a protoboard, the major modules of the protoboard being the I/O & Power Supplies, Processor, and Memories. The GR712RC processor has a redundant 1553 communication protocol and the node is connected to the bus using transformer coupling.

The features of the then proposed design were as follows:

- Usage of high density EEPROMs for software storage and minimal PROM for Boot Code.
- Boot code can perform EEPROM update by telecommands in addition to BOOT functions.
- Program execution from SRAM for faster execution, EEPROM being slow and more susceptible to upsets.
- 16 bit level translators to interface to external +5V I/O bus – to achieve +3.3 V for I/O & +1.8 V for core.
- Software tool set that supports both Ada & C (cross-compilation).

The design implementation diagram is shown below in Fig 3 followed by a brief explanation:

A. Bus - The external memory address bus is 24-bit wide whereas the data bus is 32- bit wide with 8/16 check bits (6 CBs in MA 31750). The control bus comprises of dedicated chip select, read and write signals for various memory blocks.

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B. Memory – Memory Controller acts as the interface between memory (PROM, EEPROM and SRAM) and the AHB bus. Requirement is 32K × 32 of boot PROM, 512K × 32 of EEPROM & 1.5M × 32 of SRAM and all three can be EDAC protected using (39, 7) BCH code, nevertheless, PROM does not require EDAC implementation. PROM is 3.3V operated. It is slower than SRAM and has the boot program residing on it. We observe that even though the OBC PROM requirement is only 32K × 32, the configuration is 32K × 40, since EEPROM requires additional 8 bits (512K × 40) for implementing the EDAC logic and both EEPROM & PROM share the same memory bank with respect to the processor; we extend a common configuration of 40 for both PROM & EEPROM. EEPROM is slowest & more vulnerable to disturbances. Therefore, there arises a need to load the program from EEPROM to SRAM. The maximum SRAM capacity supported is 32 MiB + 25% for EDAC checksum over 2 banks. A SRAM read constitutes two data cycles and 0-3 wait states. The PROM is fabricated with QML-qualified radiation-hardened technology and is designed for use in systems operating in radiation environments. The radiation-hardened oxide-nitride-oxide antifuse technology features, 3.3V transistors in the data path, and high-voltage N and PFETs in the programming path circuitry. The PROM operates over the full military temperature range, requires a single 3.3 V ± 5% power supply, and is available with TTL-compatible I/O. Power consumption is typically 15mW/MHz in operation and is less than 10mW/MHz in the low power-enabled mode. The PROM operation is fully asynchronous, with an associated typical access time of less than 60 nanoseconds.

C. Level Translators – 5V to 3.3V translators are implemented using 54LVTH162244. On the other hand, 5V to 3.3V and vice versa translations are implemented using 54AC164245.

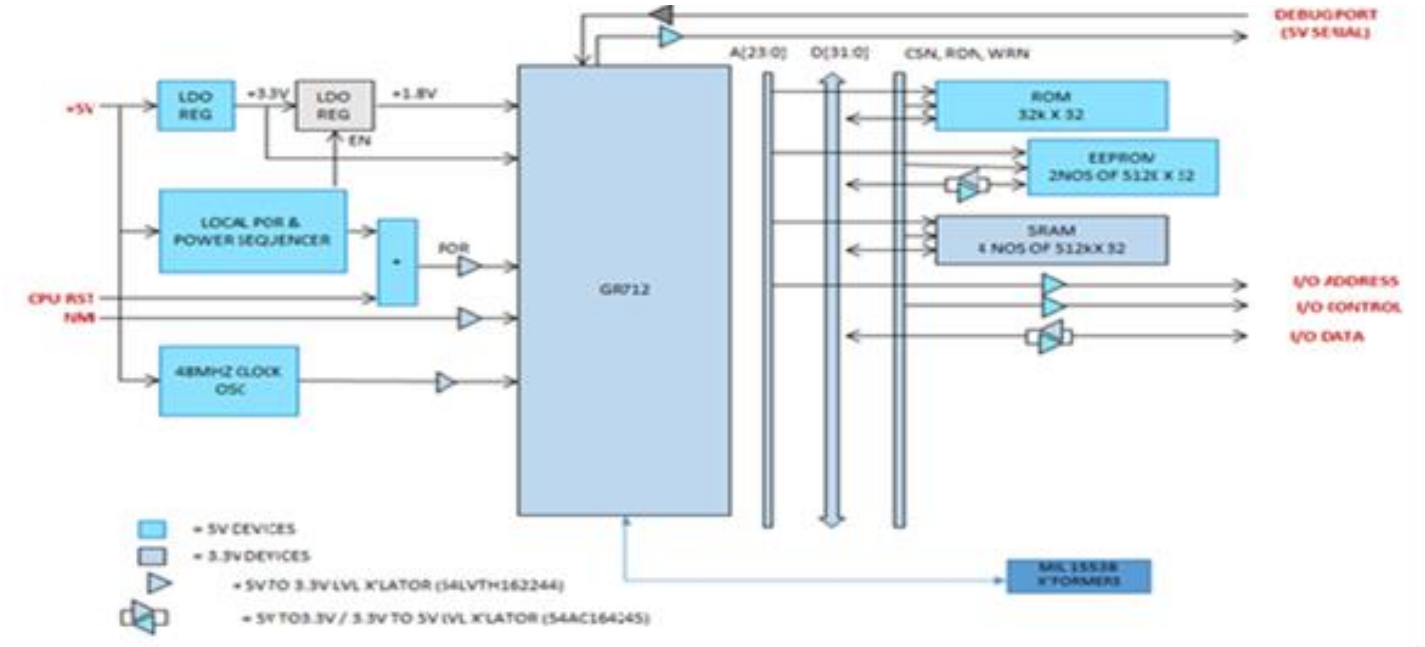

Fig.3, Design Implementation Diagram

D. Power on Reset Generation & Power Sequencing - The first start-up is the I/O (requiring 3.3V) and next is the Core (requiring 1.8V). Proper power sequencing of the processor is achieved by bringing up VDD to its recommended minimum operating voltage of 3.0V, and then delaying tVCD clock cycles before bringing up the VDDC supply. If power is applied to the VDDC supply pins while VDD is less than 3.0V, excessive current or damage to the device could occur. Power sequencing is needed when various types of electronic equipment must be powered up or down in groups, rather than all simultaneously. The design was proposed to implement suitable delays using RC based circuits. The delay values for I/O, core signals and the RESET signals in this design are 10ms, 15ms and 25ms.

E. Clock – The 16-bit processor competed with a frequency of 12 MHz, the current 32-bit processor promising a theoretical capability of nearly 90 MHz But, at higher frequencies, power consumption increases and also, board design is complex. So, a maximum frequency of operation of 48MHz is chosen.

F. Low Dropout Regulators - Low dropout regulators are used to provide regulated voltages to I/O and the core of the processor. LDOs improve transient response. The advantages of a low dropout voltage include a lower minimum operating voltage, higher efficiency operation and lower heat dissipation. LDO regulator is a DC linear voltage regulator which can operate with a very small input–output differential voltage and provides output voltages of 1.5V, 1.8V, 2.5V & 3.3V with 1.21V reference voltage. The only disadvantage of LDOs is their weight. Normal regulators cannot be used. LDOs work in the same way as all linear voltage regulators. The main difference between LDO and non-LDO regulators is their schematic topology. Instead of an emitter follower topology, low-dropout regulators utilize open collector or open drain topology. This enables transistor saturation, which allows the voltage drop from the unregulated voltage to the regulated voltage to be as low as the saturation voltage across the transistor. If a bipolar transistor is used, as opposed to a field-effect transistor or JFET, significant additional power may be lost to control it, whereas non-LDO regulators take that power from voltage drop itself.

CONCLUSION

In this paper, the design and implementation of CPU for spacecraft applications using a 32-bit dual core processor is presented. It is basically an enhancement over the existing design which implements a single core 32-bit processor for operation. The superseding processor indeed advertises an enhancement in terms of execution speed, operation in HiRel environments, fault tolerance, multiple options for external communication, power and timing constraints, size and hence weight and many more. The GR712RC device brings multi-processing to avionics and payload applications, increasing the processing performance compared to existing solutions, without consuming board real estate or demanding complex memory implementations. The GR712RC development board has been designed to support initially stand-alone operation, but also to fit into future architectures where inter-board communication is realized through active or passive SpaceWire backplanes.

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