

## Design of NCO by Using CORDIC Algorithm in ASIC-FPGA Technology

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**Abstract**—Coordinate Rotation Digital Computer (CORDIC) based digital signal processing has become an important tool in communications, biomedical and industrial products, providing designers with significant impetus for making algorithm into architecture. The algorithm has been realized in the ASIC -FPGA technology. There are numerous applications in the world of DSP that utilizes a NCO. As we are using ASIC-FPGA, we can change power, area, and speed as per our requirement, which can't be done in simple FPGA. As the output of NCO is a sinusoidal signal, we can use it in adiabatic circuits (i.e., energy recovery circuits) which are useful in designing in low power circuits.

**Keywords**- CORDIC, NCO, FPGA, ASIC-FPGA

### I. INTRODUCTION

The Coordinate Rotation Digital Computer (CORDIC) algorithm was developed by J. E. Volder in 1959, to replace the analog resolver in the B-58 bomber navigation computer at the aero electronics department at convair. In 1971, Walther has generalized this algorithm to implement rotation in circular, linear and hyperbolic co-ordinate systems. Since it is being used in applications such as digital signal processing, graphics, image processing, and kinematic processing. The advances in the VLSI technology have extended the application of CORDIC algorithm recently to the field of biomedical signal processing, neural networks and wireless communications .It is particularly suited for the handheld calculators for which cost is much more important than speed.

### II. CORDIC PRINCIPLE

The CORDIC algorithm approaches the target angle by several iterations.

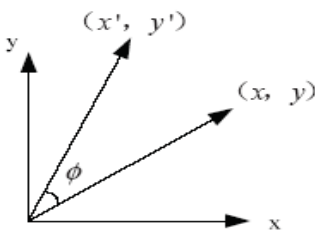


Figure 1:An illustration of the CORDIC algorithm

The basic idea of CORDIC is to rotate the vector over given angle. Each basic rotation is realized by using shift and add operations. A vector is rotated through fixed number of steps called as iterations. If a vector  $v$  having co-ordinates  $(x$  and  $y)$  is rotated through an angle  $\phi$  then obtaining a new vector with co-ordinates where  $x$  and  $y$  can be obtained using following method.

where  $X = r \cos \theta$ ,  $Y = r \sin \theta$

As showed in figure 1,the CORDIC algorithm transforming a vector  $x, y$  into a new vector  $x', y'$ . The basic iteration functions of CORDIC algorithm can be seen in the formula

$$\begin{aligned} x' &= x \cos \phi - y \sin \phi \\ y' &= y \cos \phi + x \sin \phi \end{aligned} \quad (1)$$

From formula(1) formula(2) can be derived

$$\begin{aligned} x' &= \cos \phi [x - y \tan \phi] \\ y' &= \cos \phi [y + x \tan \phi] \end{aligned} \quad (2)$$

If we made the  $\tan \phi = \pm 2^{-i}$

Where  $i$  is the current iterative times from 0 to  $N$

$$\begin{aligned} x_{i+1} &= K_i [x_i - y_i \cdot d_i \cdot 2^{-i}] \\ y_{i+1} &= K_i [y_i + x_i \cdot d_i \cdot 2^{-i}] \end{aligned} \quad (3)$$

where  $d_i = \pm 1$ ,  $K_i = \cos(\tan^{-1} 2^{-i}) = 1 / \sqrt{1 + 2^{-2i}}$   $K_i$

will be approximately equal to 0.6073 when sufficient iteration steps were computed. so the iteration eqn should multiply a gain which is computed by eqn(4)

$$A_n = \sum_{i=1}^N \sqrt{1 + 2^{-2i}} \quad (4)$$

The effective model of the rotation iterative which was used by the CORDIC algorithm is shown in equation (5).

$$\begin{aligned} x_{i+1} &= x_i - y_i \cdot d_i \cdot 2^{-i} \\ y_{i+1} &= y_i + x_i \cdot d_i \cdot 2^{-i} \\ z_{i+1} &= z_i - d_i \cdot \tan^{-1}(2^{-i}) \end{aligned} \quad (5)$$

For every step of the rotation is computed as a sign of the  $z_i$ :

$$d_i = \begin{cases} -1 & \text{if } z_i < 0 \\ 1 & \text{if } z_i > 0 \end{cases} \quad (6)$$

Then the result is

$$\begin{aligned} x_n &= A_n [x_0 \cos z_0 - y_0 \sin z_0] \\ y_n &= A_n [y_0 \cos z_0 + x_0 \sin z_0] \\ z_n &= 0 \\ A_n &= \sum_{i=1}^N \sqrt{1 + 2^{-2i}} \end{aligned} \quad (7)$$

The result is shown in the equation (8) when the initial vector  $y_0=0$ .

$$\begin{aligned} x_n &= A_n x_0 \cos z_0 \\ y_n &= A_n x_0 \sin z_0 \end{aligned} \quad (8)$$

If  $X_0$  is input data, the  $X_n$  and  $Y_n$  computed by the NCO are the results of the mixing. When we dose not use the multipliers, we can obtain the mixing data, which can reduce the hardware resources.

### III. NUMERICALLY CONTROLLED OSCILLATOR

A Numerically Controlled Oscillator produces a digital signal generator which is synchronous (i.e., clocked) usually sinusoidal. It offers some advantages in terms of accuracy, stability and reliability. It has many applications in communication systems, software defined radios, radar systems, and drivers in acoustic or optical transmissions.

Operation:

Generally a NCO consists of 2 parts

- A *phase accumulator* (PA), is generally a counter which determines the frequency of the output wave. It stores the current value of the sine's phase, and the amount it changes every cycle is normally refer to as phase.
- A *phase-to-amplitude converter* (PAC), is a look up table (LUT) containing waveform data (usually a sinusoid) for exactly one period. It uses the Pa output usually as an index into a LUT to provide a corresponding amplitude sample.

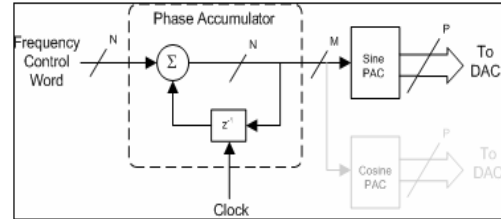


Figure 2: Block diagram of NCO

From the above fig 3, as it uses LUT's it requires more logic resources, hence more area and power .to reduce the area there by power, we are proposing a new block diagram can be seen below. The output frequency of the oscillator is given by

$$f_{out} = f_{clk} / 2^n \cdot \theta$$

### VI. PROPOSED NCO

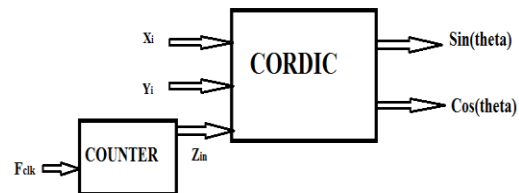


Figure 3:Block diagram of proposed NCO

It contains a simple counter / provide angles to the CORDIC algorithm, as we know CORDIC calculates the required operation accurately.

### V. IMPLEMENTATION

The verilog code is written for this paper. And it is simulated using Questasim simulator, synthesized using Precision synthesis tool. For the calculation of power, we go for cadence tools

Schematic of CORDIC algorithm

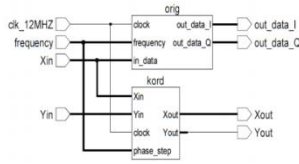
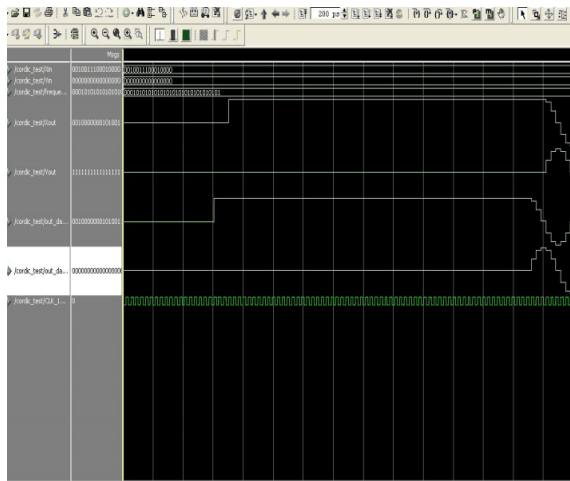
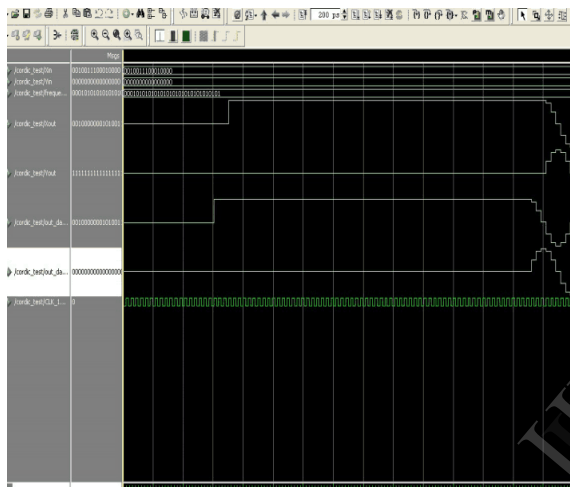


Figure 4:RTL view of CORDIC

VI.RESULTS



VII.CONCLUSION

We are using CORDIC algorithm for calculating trigonometric functions accurately and a NCO generate synchronous signal with accuracy. In ASIC-FPGA, as we can change the parameters like area , speed and power. If we are increasing the speed, can use it in high speed applications like CISC, XEON processors.

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