Design of Multi-Bit Adders for Multi-Operand Addition for with Optimised Area and Power

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***Abstract*--- In modern integrated circuits, power and area are being key factors to be considered while designing ASICs. So we have chosen customized designing of Multi-Bit Multi-Operand Adders for SHA-256 algorithm. Adder plays an important role in arithmetic operation such as addition, subtraction, multiplication, division etc. The optimization and characterization of such adder designs will aid in comparison and choice of adder modules in system design. In this paper multi-bit adders are designed using a 9-track operating with 0.8 v. and the polypitch maintained is 0.27nm. The library is implemented using 45nm in Cadence virtuoso v6.1.6. This article consists of an Adders design which has optimized area in Cadence Virtuoso v6.1.6.**

Keywords— ***VLSI-very large scale integration,ASIC-application specific integrated circuit,CMOS-complentary metal oxide semiconductor***.

I. INTRODUCTION

Integrated circuit technology has been through number of changes since some decades. **Moore's Law** is the observation made by Intel co-founder Gordon Moore that the number of transistors on a chip doubles every two years while the costs are halved. In 1965, Gordon Moore noticed that the number of transistors per square inch on integrated circuits had doubled every two years since their invention. This has paved the way for advanced VLSI (Very Large-Scale Integration) Adders are utilized to generate memory locations in different architectures and algorithms. Thus, improvement in the full adder would prove more beneficial for all the circuits where its application has a significant effect in the performance of the circuit. The most important parameters to be kept in consideration are compactness in designing ASICs which affects the performance and usefulness of any VLSI circuit. The paper here aims at analysis and improvement of structure size reduction of the 28T full adder at 45nm technology. Here 32bit Multi-Operand Adders are designed, characterized and verified using Cadence Virtuoso v6.1.6. Cadence Virtuoso is a tool used to design to help users to create manufacturing robust designs. . These adders are designed and implemented using carry ripple adder method in 45nm technology in cadence tool. The purpose of this project is to design and implement two different multi operand adders. designed is of only 1 bit which is implemented with different architectural methods that consumes more power and area.

II. PROPOSED DESIGN

A. *MULTI-OPERAND ADDERS*

The proposed design is of multi-bit adders which can be used for modulo addition and multiplication. The first adder is designed by using the method of carry ripple adder which is implemented by series of full adders in a linear method which has carry out of one full adder as an input to the n next full adder. The second adder is a carry save adder in a linear implementation that is similar to carry ripple adder where full adder does not need to wait for the previous carry out bit to be calculated before it does its own calculation. The final adder that was designed is a carry save adder which is of 32 bit that uses less area and power consumption. The technique used consists of N full adders in parallel where they can accept three N-bit input words $Xn\ldots1, Yn\ldots1, and\ Zn\ldots1$, and produces two N-bit output words $Sn\ldots1\ and\ Cn\ldots1$,satisfying X+Y+Z=S+2C as shown in figure 1.The results are sums and carries-out of each adder. This is called carry-save redundant format as carry outputs are preserved rather than propagated along the adder. Hence the full adders are called as carry-save form. The carry word C is shifted left by one position and added to the sum word S with an ordinary CPA,the results is X+Y+Z.

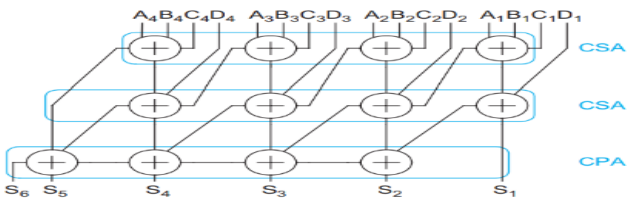

Figure 1: Multi operand Addition

B. *28-T TRANSISTOR ADDER DESIGN*

A single bit traditional CMOS Full-Adder cell is shown in fig.1. The single bit full adder cell has 28 transistors. Different logic design can be investigated from different points of view. Distinctly, they tend to favor one performance parameters at the expense of others [1]. In other words, it is different design specification constraints imposed by the application that each logic design has its place in the implementation of cell library

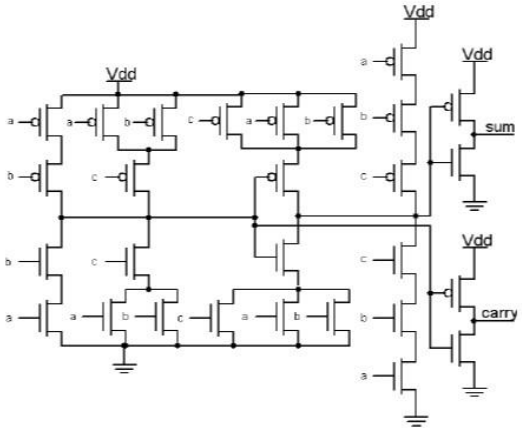

Fig 2: 28-Transistor Adder

The design is not always attained easily. The CMOS designs are not area efficient for complex gates which have large fanins. Thus, we must be careful while realizing a logic function using static logic style. Pseudo NMOS technique is simple, yet it binds noise margin and suffers from static power dissipation losses. Pass transistor logic design style is a popular method for implementing some specific circuits such as multiplexers and XOR-based circuits, like adders [6]. While, dynamic logic facilitates in realizing fast, small and complex gates. However, this advantage is gained at the outlay of parasitic effects such as load sharing, which leads to hazardous design process. Charge leakage requires frequent refreshing, operational frequency reduction of the circuit. In general, none of the above mentioned designs can compete with CMOS style in robustness and stability . The CMOS structure combines NMOS pull-down and PMOS pull-up networks to produce considerable outputs. In this style all transistors (either PMOS or NMOS) are arranged in completely separate branches, consisting of several subbranches. Mutually exclusiveness of pull-up and pull-down networks is of a great concern.

III. PROPOSED LAYOUT

This paper aims in reducing the overall area and power such that the design becomes better applicable for the various applications. Figure 3 shows the full custom layout of FULL ADDER. To continue with this the layout is created in full custom manner using 9 tracks over 12 tracks as in Cadence Virtuoso library which will help in reducing overall area. In the Figure 4 shows the full custom layout of FULL ADDER using 28T. The designs are implemented using Cadence Virtuoso tool.

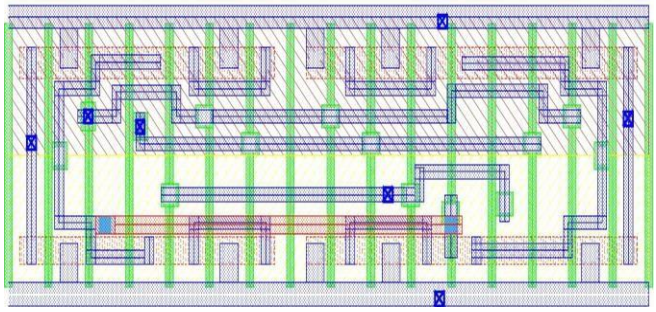

Fig 3: Full customized 28T Adder Layout

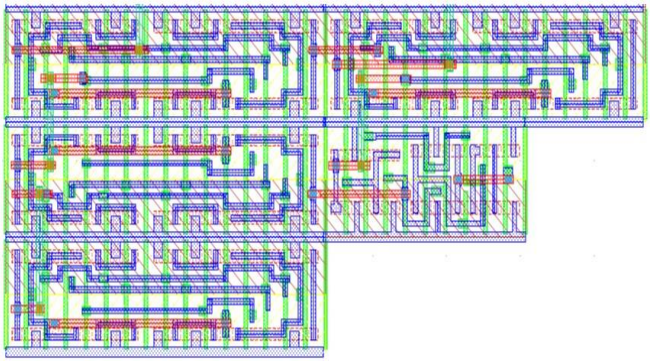

Fig 4: Full customized layout design of 3 operand Adder with the 3 unique stages

The above figure shows a 3-Operand Adder design layout where there are totally 3 stages which are unique and for the rest of the required bits 3rd stage is replicated upon each other. The adders initial stages consist of Carry Save Adders and the last stage is Carry Propagate Adders. Adders are implemented as Macros , they are block level designs which are optimized for power or area or timing. The below figure in the next

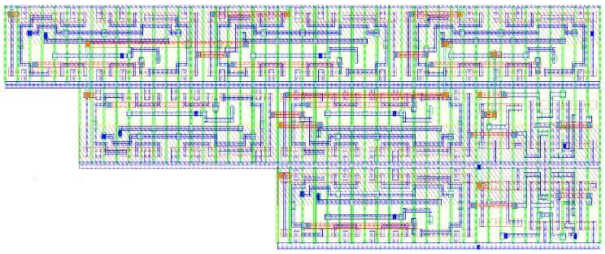

Fig 5: Full customized layout design of 4 operand adder with the 3 unique stages

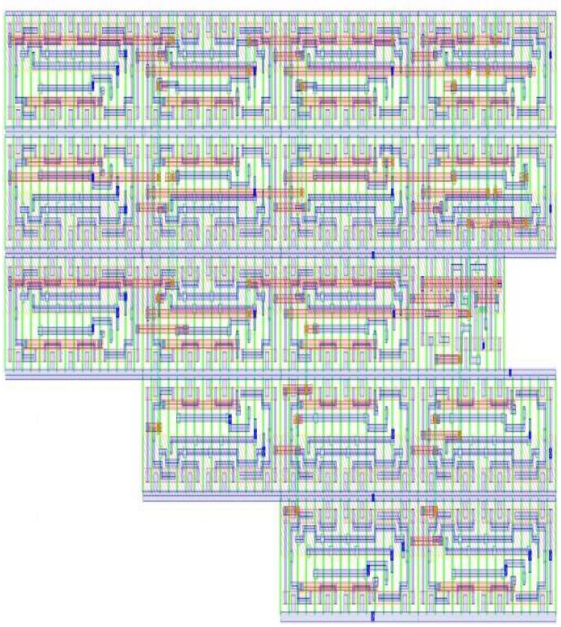

Fig 6: Full customized layout design of 5 operand Adder with the 5 unique stages

The above figure shows a 5-Operand Adder design layout where there are totally 4 stages which are unique and for the rest of the required bits 4th stage is replicated upon each other.

The 5-operand adder is constructed using the multibit adder topology design where the 3-operand adder is added with 2operand adder in order to get the 5-operand adder with optimized area and power.

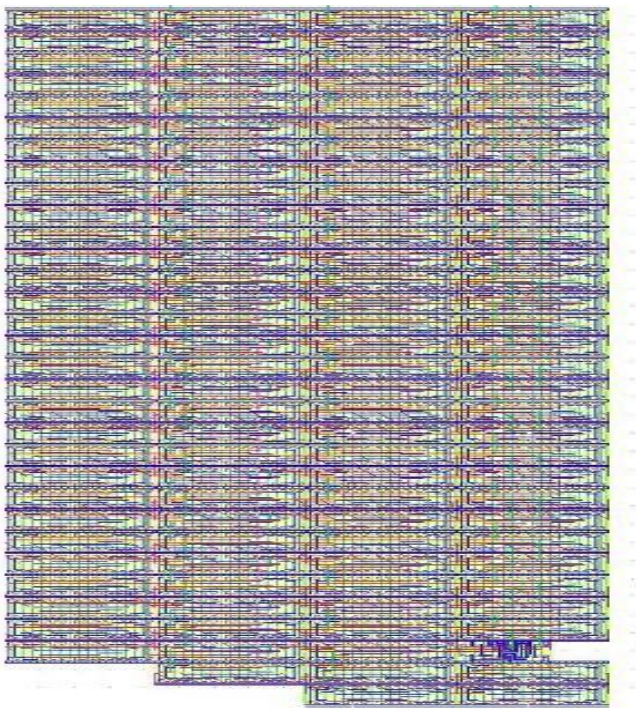

Fig7: Full customized layout design of 5 operand Adder (32-Bit)

The 32-bit adder is designed by creating the instance of one full bit 28-T adder. This adder is joined but calling the instances by 32 times hence we can conclude that the 5operand adder can be created in such manner.

IV. SIMILATION AND RESULTS

Figure 8 and Figure 9 shows the schematic and waveform of FULL ADDER. The functionality of the proposed design is verified and a comprehensive study of area, power reduction has done. The Full Adder used in the given design is also called as mirror type adder design because the N-MOS and P-MOS structure are in symmetric design [4].

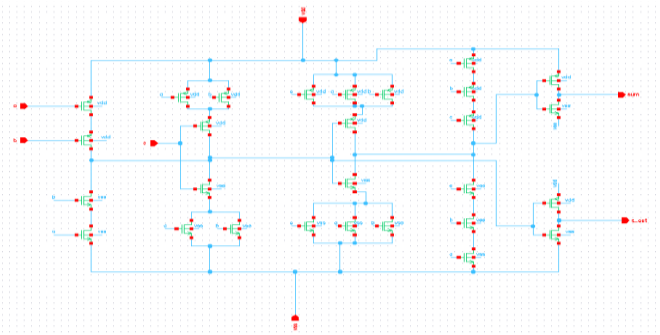

Fig 8: Full Adder Schematic

The schematic design of adder is shown above where it is designed in a rippler carry adder topology by using 28 transistors where the output obtained is sum and carry. The input are given to a inverter where the output which is obtained contains another inverter to get required output Design.

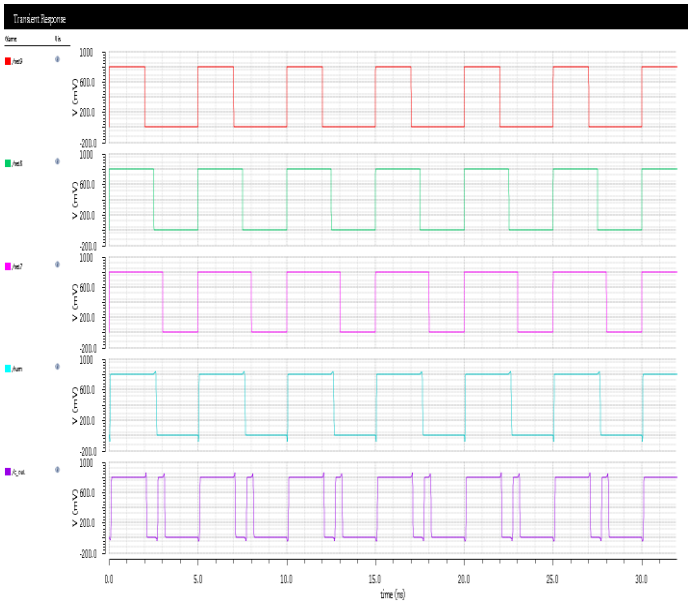

Fig 9: Waveform of Full Adder

The above figure explains about the waveform of the output obtained. The output are digital samples with either 1 if it is true else 0 if it is false or if the output is 0.The sum output is clear which gives the desired output with clear 1 and 0 but the carry output has some glitches where it may arise due to the width of PMOS and CMOS structures

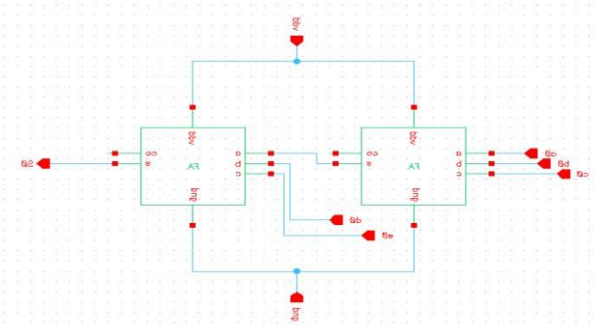

Fig 10**:** Five Operand Adder schematic

Figure 10 shows the schematic diagram of a 5-operand adder design and the connections are shown in the figure. This schematic is designed but combining one 3-operand full adder with that of 2-operand adder by connecting source and drain common. The output of 3-operand adder is given as input to that of 2-operand adder in order to create 5-operand.

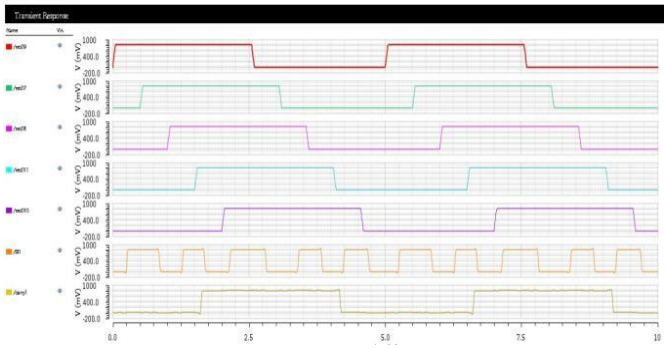

Fig 11**:** Waveform of Five Operand Adder Schematic

The above figure is the output of 5-operand adder where the output is clear which has a required output of sum and carry without any glitches in the waveform. Hence we can say that the output waveform can get correct clear sample of 1 and 0.

Table. 1**:** Comparison with existing cadence virtuoso library 45nm technology

Parameters	Proposed layout	Cadence library
Area	4.956um^2	6.019um^2
Cell height	1.24um	1.9um
Tracks	9	12
Operating voltage	0.8 V	1.1 V

From Table 1 shows the designs provided by Cadence Virtuoso library to proposed fully custom layout design**.**

V. CONCLUSION

This article has focused on designing Multi-bit Multi-operand Adder using Cadence Virtuoso v6.1.6 with reduced area and the power. These designs are also effective in ASIC design. Simulation results from the Table 1 concludes that this design can operate at 0.8 v as input voltage and with reduced power consumption and reduced area.

VI. ACKNOWLEDGEMENTS

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REFERENCES

[1] N. Zhuang, H. Ho, “A new design of the CMOS full adder,” IEEE. J. of Solid-State Circuits, Vol. 27, No. 5, pp. 840- 844, May 1992.

[2] R. Uma,Vidya Vijayan , Mohanapriya and Sharon Paul,“Area, Delay and Power Comparison of Adder Topologies ” International journal of VLSI Design and Communication Systems(VLSICS), Vol. 3, No. 1,Feb 2012

[3] Jasbir Kaur and Lalit Sood, “Comparison Between Various Types of Adder Topologies” IJCST Vol. 6, issue 1, Jan-March 2015

[4] Suryasnata Tripathy, L B OM Prakash , B. S. Patro and Sushanta K. Mandal, “A Comparative Analysis of Different 8-Bit Adder Topologies at 45nm Technology” International Journal of Engineering Research & Technology (IJERT) ISSN: 2278-0181 Vol .2 issue 10,October-2013

[5] M. Morris Mano, Digital Design second Edition, Prientice Hall,1991

[6] Niel H. E. Weste, David Harris, Ayan Benerjee, “CMOS VLSI Design”, Pearson Education, New Delhi, pp. 16, 2009.

[7] Sung-Mo Kang, Yusuf Leblebici, ―CMOS Digital Integrated Circuits, Tata McGraw-Hill publication New Delhi, pp. 343-347, 2010.

[8] A.M. Shams, M.A. Bayoumi, “A novel highperformance CMOS 1-bit full-adder cell,” IEEE Transactions on Circuits & Systems. II, Vol. 47, pp. 478– 481, May 2000.

[9] Abu-Shama, M.A. Bayoumi, “A new cell for low power adders,” Proc. lot. Midwest Symp. Circuits & Systems, pp. 1014-1017, 1995.

[10] R. J. Bakcer, H. W. Li and D. E. Boyce, “CMOS design, layout and simulation”, IEEE Press, 1998.

[11] Pallavi Saxena,Urvashi Purohit,Priyanka joshi, “Analysis of Low power, Area Efficient & High Speed Fast Adder” International journal of Advanced research on computer and communication engineering,2013 [12] D. Radhakrishnan, “Low-voltage low-power CMOS full adder,” Proc. Inst. Elect. Eng., Circuits Devices Systems, Vol. 148, No. 1, pp. 19–24, 2001..

[12] R. Jacob Baker et al., “CMOS – Circuit Design, Layout and Simulation”, Wiley-IEEE Press, 1997.