International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 4 Issue 01,January-2015

Design of Modified Decoder for Concurrent BIST and BISR Architecture

Mr. G. Pradheep, B. E, M.E,
Assistant Professor, Department of ECE,
Loyola institute of technology and science,
Loyola Nagar, Thovalai.

Ms. D. Beulet Mary, B.E, (M.E),
Student, Department of ECE,
Loyola institute of technology and science,
Loyola Nagar, Thovalai.

.

***Abstract*— Built in self test (BIST) brings forth an intended result and practical approach for VLSI circuit testing. The input vectors are the test patterns which can be supervised and the testing can be performed during the typical operation of the circuit without striking the circuit's normal operation. This is one of the online techniques estimated based on hardware overhead and concurrent test latency (CTL), the span taken to finish the entire test. In this paper we confer a novel idea of supervising the incoming input vectors of the circuit during the typical operation. The modified decoder with comparator and test generator are utilized to decode certain inputs it acquired. The static RAM like structured cells is employed to store the respective locations of the incoming circuit input vectors. The sense amplifier and two D flip flops with W stage counter is also involved in the respective logic module.**

The spare memory and controller is involved and permanent memory is introduced with compressed test vectors. The suggested scheme is manifested to accomplish crucially better than formerly proposed schemes with the benefit of less circuit complexity and the concurrent test latency is reduced.

***Index Terms*— Built in self test, concurrent test latency, response verifier, concurrent BIST unit**

I.INTRODUCTION

Built-in self test (BIST) techniques constitute a class of schemes that provide the capability of performing at-speed testing with high fault coverage. They constitute an attractive solution to the problem of testing VLSI devices. In off-line testing, a circuit is tested once and for all, with the hope that once the circuit is verified to be fault free it would not fail during its expected life-time. However, this assumption does not hold for modern day ICs, based on deep sub-micron technology, because they may develop failures even during operation within expected life time.

To enable replacement of faulty circuitry, the ICs are tested before each time they startup. If a fault is found, a part of the circuit is replaced with a corresponding redundant circuit part. Testing a circuit every time before they startup, is called Built-In-Self-Test (BIST). BIST is basically same as off-line testing using ATE where the test pattern generator and the test response analyzer are on-chip circuitry (instead of equipments). As equipments are replaced by circuitry, so it is obvious that compressed implementations of test pattern generator and response analyzer are to be designed. The BIST operation carried out in two modes as normal mode and the test mode. During this method the performance of the circuit is able to degrade. To overcome this input vector monitoring is introduced.

These architectures test the CUT concurrently with its normal operation by exploiting input vectors appearing to the inputs of the CUT; if the incoming vector belongs to a set called active test set, the RV is enabled to capture the CUT response. The block diagram of an input vector monitoring concurrent BIST architecture is shown in Fig. 1. The CUT has n inputs and m outputs and is tested exhaustively; hence, the test set size is N = 2n. The technique can operate in either normal or test mode, depending on the value of the signal labeled T/N.

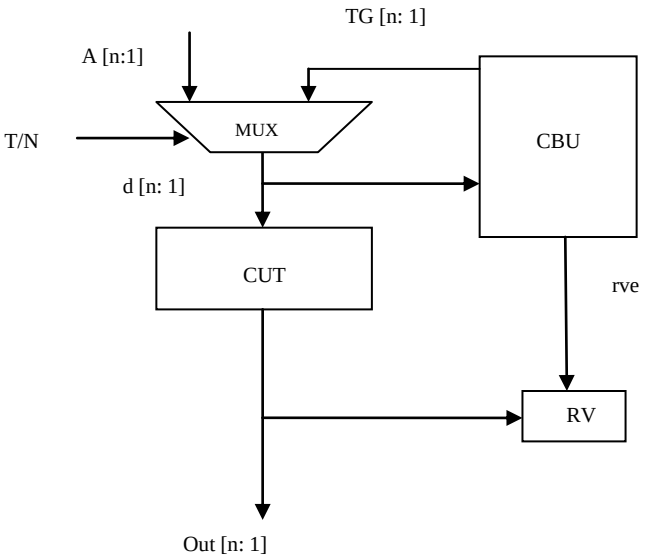

Fig1 Input vector monitoring concurrent BIST

During normal mode, the vector that drives the inputs of the CUT (denoted by d [n: 1] in Fig.1) is driven from the normal input vector (A [n: 1]). *A* is also driven to a concurrent BIST unit (CBU), where it is compared with the active test set. If it is found that A matches one of the vectors in the active test set, we say that a hit has occurred. In this case, *A* is removed from the active test set and the signal response verifier enable (rve) is issued, to enable the m-stage RV to capture the CUT response to the input vector. When all input vectors have performed hit, the contents of RV are examined.

During test mode, the inputs to the CUT are driven from the CBU outputs denoted TG [n: 1]. the concurrent test latency (CTL) of an input vector monitoring scheme is the mean time required to complete the test while the CUT operates in normal mode. An advantage of built-in self-test (BIST) is its low cost compared to external testing using automatic test equipment (ATE). In BIST, on-chip circuitry is included to provide test vectors and to analyze output responses. One possible approach for BIST is pseudo random testing using a linear feedback shift registers (LFSR). Among the advantages of BIST is its applicability while the circuit is in the system.

II EXISTING SYSTEMS

The input vector monitoring concurrent BIST techniques have been proposed which make use of input vectors arriving at the inputs of the CUT during normal operation. C-BIST, R-CBIST, MHSAT, OISAT, W-CBIST, SWIM are the previously employed techniques for the input vector supervising operation.

In C_BIST, the hardware related to this organization is modified and said to be comparative concurrent Built in self test. In this modified organization an equality comparator is added to compare the normal inputs to the CUT to the output of TG. The Active test set Generator and Comparator of C-BIST is a single Linear Feedback Shift Register and a comparator and thus the active test set consists of only one active test vector, which is the present value of the LFSR. During normal mode, the input vector is compared with the distinctive active test vector. If the two vectors match, the LFSR shift to the next state changing the active test vector and the Response Verifier is enabled. In C-BIST, the value of the concurrent test latency is very high since in every clock cycle the active test set consists of only one active test vector and it suffers from long test latency.

In MHSAT, the Active test set Generator and Comparator of MHSAT, consists of L *(L>1)* LFSRs and L comparators and thus the active test set consists of L active test vectors. Also, there is L order-dependent Response Verifiers each one corresponding to an LFSR. During normal mode, the input vector is compared to the L active test vectors. A hit occurs if the input vector matches any one of the active test vectors. In this case, the LFSR that performed the hit continues to the next state changing the specific active test vector, and the corresponding MISR is enabled. The test is complete when all the LFSRs have completed their cycles. In OISAT, instead of L order independent response verifier it employs only one order independent response verifier. The RV is enabled every time an LFSR performs a hit.

R-CBIST, which is more efficient than the other input vector monitoring concurrent BIST techniques projected so far in terms of Hardware Overhead and Concurrent Test Latency trade-off. It is based on a separate data bus RAM with 2k x (w+l)-bit memory locations where k+w=n. The pin out of the RAM consists of the address bus (A [k: l]) the input data bus the output data bus and two control signals: clock enable bar (ceb) and write enable bar (web). Every instant, the address bus point out the address of a memory word called enabled word. The address of the enabled word is the enabled address. The signal ceb is used to synchronize the read write access operation and web is used to differentiate between a read and a write access cycle. In R-CBIST, the Response Verifier is order-independent. The accumulator-based compaction of the responses is an order-independent Response Verification technique that requires only one D-type flip-flop and one full adder at each output of the CUT. This technique comprised with many hardware components when comparing to other monitoring systems taken down for the input vector monitoring and can be efficiently utilized.

The W-CBIST is another one method shown to be better than other input vector monitoring concurrent BIST schemes for low values of the hardware overhead. The test set size is Ts=2n. W-MCBIST is based on the partition of the test set into non-overlapping subsets (called windows) each one of size Ws =2w, where $0 < w < n$; and NW is the total number of windows. During normal operation, w-MCBIST utilizes the arrival of any test vector belonging to a specific window, called active window. The input vector is compared against a set of Ws vectors that comprise the active window as follows. The (n-w) bits of the n-bit input vector are compared with the outputs of the (n-w)-stage test generator and, if they match, comparator is enabled. The remaining w bits of the input vector are driven to the inputs of a w×Ws decoder whose enable input is driven by comparator. Therefore, if the input vector belongs to the active window, one of the signals is enabled. When all vectors of a window have performed a hit, the signal test generator enable signal triggers the test generator to the next state, in order to observe a new window. After the test generator has generated all its 2n-w states, we detect the signature captured in RV and decide whether the CUT is faulty.

Square Windows Monitoring (SWIM) concurrent BIST is based on monitoring input vectors using a square window. The basic idea of SWIM is to monitor a "square" window of vectors, whose size is W1xW2, with W1=2W1 and W2 = 2W2. The bits of the input vector are divided into three distinct sets comprising w1, w2 and k bits respectively, such that w1+w2+k=n. The k (high order) bits of the input vector specify whether the input vector belongs to the window under consideration. The w1+w2 remaining bits specify the relative location of the incoming vector in the current window. If the incoming vector belongs to the current window and has not been received during the assessment of the current window, we say that the vector has performed a hit and the response verifier is clocked in order to capture the CUT's response to the vector. When all vectors that belong to the current window have reached the CUT inputs, we continue to inspect the next window. The drawbacks of these techniques are overcome by our proposed methodology.

III PROPOSED METHODOLOGY

A.OVERVIEW

The circuit with n inputs and m outputs are taken under consideration. The window of vectors are monitored and the size of the window is denoted by W. The value of W is given by $W = 2^w$ where w is an integer number where w is less than n. The vectors which belong to the corresponding window are monitored every moment.

The input vectors are the normal possible test patterns which are applied to the circuit under test. The input vectors are classified into two distinct test sets consists of w and the k bits and so n=w+n. The k bits are the higher order bits and they show whether the input vector belongs to the corresponding window which is considered for the test. The w bits are the lower order bits and they exhibit comparable location of the vector. The window is involved with many input vectors which are considered for the test. The vector which belongs to the window and not been received during the examination of the window it is assumed that the hit is performed. The hit is nothing but the input vector is matched with one of the test vector in the active window. The active window is contained with many test vectors. This performance happened inside the concurrent BIST unit. After the hit is occurred the response verifier is clocked to capture the CUT'S response to the vector. When all the vectors belonging to the current window had completed the hit and reached the CUT inputs the next examination of next window is started.

The technique can operate in two modes such as normal mode and the test mode. During normal mode the T/N = 0, the normal input vectors are driven to the circuit under test. At the mean time the input vectors are also driven to the concurrent BIST unit as: the k bits which are the higher order bits are applied to the k – stage comparator and the other inputs of the comparator are gained from the outputs of the test generator. In addition to the comparator and the test generator the modified decoder and the logic module are used in this novel scheme. The Built in self repair (BISR) is a self repair scheme so that it will perform testing, analysis and repair on every power-up. It is a redundancy organization. If the test controller or else the memory under test are repair, they can be replaced by the spare controller and the spare cell.

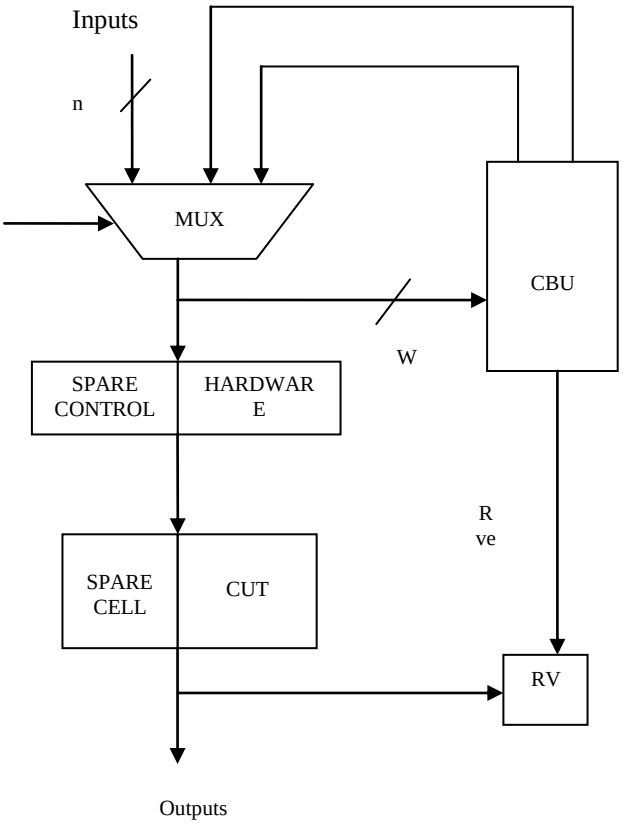

Fig 2 Block Diagram

The certain test vectors are permanently incorporated inside the memory by replacing the test pattern generator and the decoder in order to reduce the hardware overhead.

B.IMPLEMENTATION

The input vector monitoring concurrent BIST using the static RAM cells can be functioned by the following process. This test can be carried out during the normal operation of the circuit i.e. the concurrent test mode of the circuit. It can be classified into three modules as: The memory under test, the test pattern generation and the response verifier.

Memory under test: The circuit which is taken down for the test in this implementation is memory. The 10 x 10 memory is designed with ten rows and ten columns. The memory is nothing but the storage device which can store the data's which we send to store and then retrieve as our needs. In this memory read and write operation is checked. Initially we are giving zero as the input and tested for the response verifier output. If we receive the same input we can say that the memory under test is without any error and as fault free circuit.

Secondly, we shall give zero as input data to the memory under test. By changing the test input as one the memory output gives the different output and we can say that the circuit is with certain faults.

Test pattern generation: The TPG uses the characteristic information of the circuit to generate the test vectors internally. The characteristic information of the circuit is extracted using known spectral methods. The test pattern generator generates some selected test vectors to compare the incoming input vectors. The individual inputs are taken while comparing the inputs in the concurrent BIST unit. The test vectors are generated in the logic module by performing the hit of the vector to identify which vector is presented in the current window. This test signals are send to the memory under test only in the test mode. Because in normal mode sometimes the vectors will not check all the input vectors. The test vectors are automatically generated by the test generator and the response verifier is enabled corresponding to the output. In addition to this the w-stage counter is included to overflow the test generator signals because to reduce the size we are using this counter and to speed up the process.

Response Verifier: The response verifier is nothing but it will check and compare the outputs of the memory under test and the concurrent BIST units. The memory is designed with applying 00 input and retrieving the same output. So it will store 00 as the value to give as output. The inputs given to test the memory is 00 and 11. Initially 00 is given as the input to the memory under test by the test generator. The response verifier will receive the memory output and the CBU output. If the responses matched and the RV gives the output as 1we can say the memory is without any faults. Secondly 01, 10, 11……..are the corresponding inputs are given simultaneously and test the responses of the memory. The response verifier will check the simultaneous output and compare and found that the responses received are correct or incorrect for the above inputs. Finally it is found that the memory is fault free when the input is given as 00 because the stored memory data is 00.

The hardware overhead of the proposed scheme is calculated using the gate equivalents as a metric. One gate equivalent or gate is the hardware equivalent of a two input NAND gate. The accumulator-based compaction of the responses is an order independent response verification technique that has been shown to have aliasing properties similar to the best compactors based on cellular automata and multiple input signature registers.

C.BISR

The BIST circuit detects the faults in the main memory and spare memory. In test/repair mode the memory is accessed by the BIST module, while in normal mode the wrapper selects the data outputs either from the main memory or the spare memory. When we turn on the power, the BIST module starts to test the spare memory. Once a fault is detected, it informs the BIRA module to mark the defective spare row or column as faulty through the Error (ERR) and Fault Syndrome (FS) signals. After finishing the spare memory test, it tests the main memory. If a fault is detected, the test process pauses and the BIST module exports FS to the BIRA module, which then performs the RA procedure. When the procedure is completed and the memory testing is not yet finished, the BIRA module issues a Continue signal to resume the test process. As such the faulty memory and the faulty controller can be replaced by the spare memory and the spare controller.

IV. SIMULATION RESULTS

The simulation output for the above proposed methodology is given as follows:

The concurrent BIST unit is one of the significant units which are included with the modified decoder, comparator and the logic module. The input vectors are also compared using the comparator. The output of the concurrent BIST unit is applied to the circuit under test with the help of test generator. The response verifier is the one which verifies the ouput of the concurrent BIST unit and the ouput of the memory under test. The comparator will check and compare the normal input vectors and the test vectors. According to the test generator input the modified decoder is enabled.

If the test generator apply the input as 10, 01,11 etc the test generator output is shown as 1 because the data input given to store 00. Hence it is identified if anyother inputs is given as test vector to test the expected output does not acquired.The response verifier will compare the outputs efficiently. The test generator will apply the test vector as 00 which is same as the input normal input vector to the memory under test. The memory input is also sent to the comparator. In the mean time the test vector will also reached and the comparison taken down. The modified decoder will be enabled and the output is given to the logic module. The hit of the vector is carried out if the test vector in the active test set is got matched. In conclusion the output of response verifier is 00 and proved that the memory is fault free.

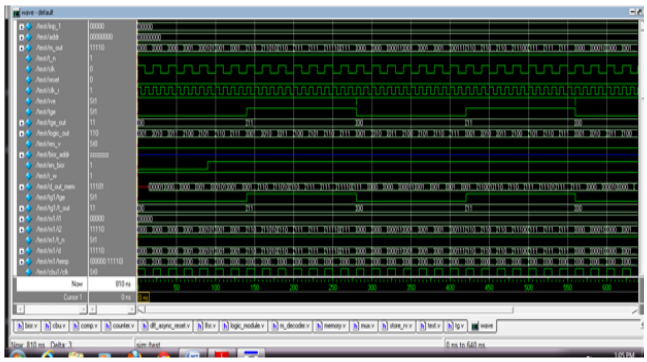

Fig.3 Simulation Outcome

V. CONCLUSION

In our proposed concept BIST is one of the imperious techniques to test the VLSI circuits. The testing is performed during the normal operation of the circuit without setting the circuit offline because the offline testing is more complicated and they contribute many problems. The input vector monitoring BIST scheme in addition to the use of static RAM cells are employed. This scheme is the online testing which is more reliable. The circuits are tested based on two important agendas. They are hardware overhead and the concurrent test latency i.e. the span taken to complete the circuit test. The modified decoder which extracts certain input vectors is used and the logic module which generates the test vectors to test the memory which is chosen as the circuit to test is involved. In this logic module the static RAM like cells are employed to store the corresponding locations of the vectors which belongs to the current window that is under examination during the typical operation. In addition to it the spare memory and the spare controller is implemented for the efficient operation of the circuit. By analyzing the hardware overhead and the concurrent test latency it is concluded that the proposed scheme is more efficient then the previously implemented testing techniques.

REFERENCES

1. I. Voyiatzis, A. Paschalis, D. Gizopoulos, N. Kranitis, and C. Halatsis, (2005), 'A low-cost concurrent BIST scheme for increased dependability', IEEE Trans. Dependable Secure Comput., vol. 2, no. 2, pp. 150–156
2. S. Almukhaizim, P. Drineas, and Y. Makris, (2006), 'Entropy-driven parity tree selection for low-cost concurrent error detection', IEEE Trans. Comput Aided Design Integr. Circuits Syst., vol. 25, no. 8, pp. 1547–1554
3. S. Almukhaizim and Y. Makris, (2007), 'Concurrent error detection methods for asynchronous burst mode machines,' IEEE Trans. Comput., vol. 56, no. 6, pp. 785–798
4. Ioannis Voyiatzi, Antonis Paschalis, Dimitris Gizopoulos, Constantin Halatsis, Frosso S. Makri, and Miltiadis Hatzimihail (2008), 'An Input Vector Monitoring Concurrent BIST Architecture Based on a Precomputed Test Set,' IEEE Trans. on computers, vol. 57, no. 8
5. I. Voyiatzis, T. Haniotakis, C. Efstathiou, and H. Antonopoulou, (2010), 'A concurrent BIST architecture based on monitoring square windows,' in Proc. 5th Int. Conf. DTIS, Mar. 2010, pp. 1–6
6. I. Voyiatzis and C. Halatsis, (2005), 'A low-cost concurrent BIST scheme for increased dependability,' IEEE Trans. Dependable Secure Comput., vol. 2, no. 2, pp. 150–156.
7. M. A. Kochte, C. Zoellin, and H.-J. Wunderlich,(2009), 'Concurrent self-test with partially specified patterns for low test latency and overhead,' in Proc. 14th Eur. Test Symp., pp. 53–58
8. I. Voyiatzis, (2008), 'On reducing aliasing in accumulator-based compaction,' in Proc. Int. Conf. DTIS, pp. 1–12
9. E. J. McCluskey, (1985), 'Built-in self-test techniques,' IEEE Design Test Comput., vol. 2, no. 2, pp. 21–28
10. K. K. Saluja, R. Sharma, and C. R. Kime,(1998), 'A concurrent testing technique for digital circuits,' IEEE Trans. Comput. Aided Design Integr. Circuits Syst., vol. 7, no. 12, pp. 1250–1260
11. R. Sharma and K. K. Saluja,(1993), 'Theory, analysis and implementation of an on-line BIST technique,' VLSI Design, vol. 1, no. 1, pp. 9–22
12. K. K. Saluja, R. Sharma, and C. R. Kime,(1986), 'Concurrent comparative built-in testing of digital circuits,' Dept. Electr. Comput. Eng., Univ. Wisconsin, Madison, WI, USA, Tech. Rep. ECE-8711
13. J. Rajski and J. Tyszer, (1993), 'Test responses compaction in accumulators with rotate carry adders,' IEEE Trans. Comput. Aided Design Integr. Circuits Syst., vol. 12, no. 4, pp. 531–539
14. L. R. Huang, J. Y. Jou, and S. Y. Kuo, 'Gauss-elimination based generation of multiple seed-polynomial pairs for LFSR' IEEE Trans. Comput. Aided Design Integr. Circuits Syst., vol. 16, no. 9, pp. 1015–1024.
15. E. J. Mc Cluskey, "Built-in self-test techniques," IEEE Design Test Comput., vol. 2, no. 2, pp. 21–28, Apr. 1985.