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Design of Miller Compensated Two-Stage Operational Amplifier for Data Converter Applications

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***Abstract*: This paper presents the detailed design of Miller compensated two stage operational amplifier for data converter applications such as Delta-sigma (Δ-Σ) analog-to-digital converters. The op-amp is designed to meet the requirement of high-speed high-resolution Delta-sigma (Δ-Σ) modulators at the cost of moderate power consumption. The circuit is implemented in a TSMC 0.18µm 3.3V CMOS technology. The design is carried out using LTSPICE tool.**

Keywords*: CMOS operational amplifier, Delta-sigma (Δ-Σ) analog to digital converter, loop filter, stable trans- conductance biasing.*

I. INTRODUCTION

CMOS Operational amplifier is a fundamental building block for numerous analog circuit designs. Operational amplifiers are one of the basic and important circuits which have a wide application in several analog circuits such as delta-sigma (Δ-Σ) analog to digital converters, switched capacitor filters and sample and hold amplifiers etc.The loop filter in delta-sigma (Δ-Σ) analog to digital converters is analog one and can be implemented either in a continuous time (Active-RC filter)or in a discrete-time(switched capacitor filter) active form and they can be implemented using two stage op amp or folded cascode operational amplifiers [1].CMOS two stage op amp best choice for implementation of summing amplifier or loop filter in delta sigma modulators since op amp provides high mid band DC gain, high band width, and high linearity [2].

The speed and settling accuracy of the delta sigma modulators are determined by the performance of the operational amplifier. The adequate speed of the Δ-Σ modulator is determined by the unity gain frequency and settling time while the settling accuracy is determined by the DC gain of the op amp. In Switched-capacitor circuits charge being transferred from one capacitor to another rapidly in each clock of operation therefore op amp slew-rate limit has to be taken into another design consideration. The Slew rate and bandwidth limitations produce harmonic distortion reducing the total SNDR of the sigma-delta modulators. In typical switched capacitors, the unity gain bandwidth of the operational a general rule of thumb is that the clock frequency should be 5 times than the unity gain frequency and the phase margin is at greater than 70 degrees to ensure stability. In other words the time constant of the filter should be kept smaller than the sampling period T, for the modulator to be stable. Further input-referred offset voltage of an op-amp in a CMOS technology typically around 5mV, which becomes more pronounced in low-voltage applications, where the inherent signal swing is reduced.

This paper describes the design of miller compensated two stage operational amplifier operating at 3.3V for the continuous time delta sigma modulator applications. The design mainly focussed to achieve sufficient electrical characteristics such as unity gain frequency, slew rate, Input common mode range, output swing and output offset all are taken into consideration as power consumption is secondary concern.

II. CIRCUIT DIAGRAM

A. Topology

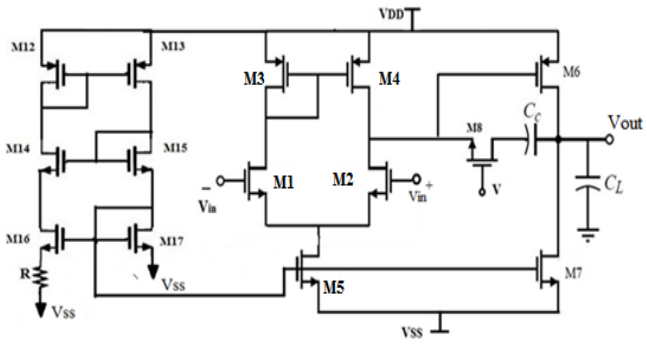

Fig.1 Miller compensated two stage operational amplifier.

The miller compensated two stage op amp with robust biasing circuit is shown in Fig. 1. It consists of stable trans-conductance biasing circuit and two stage op amp. The first stage usually consists of high gain, differential amplifier. The common source amplifier usually meets the specification of the second stage, having a moderate gain.

B. *Design Specifications*

TABLE I
SPECIFICATIONS

Name of the Parameter	Specification
Power supply	± 1.65 V
Technology	0.18 µm TSMC
Open loop gain (A_v)	> 70dB
Gain –Band width product (GB)	100MHz
Phase Margin (P.M)	≥ 60 degrees
Output offset voltage	< 5mV
Slew rate	≥ 50 V/ μs
Output Voltage Range	$\geq 2V_{p-p}$
Input common mode range (ICMR)	- 0.8 to 1.3V
Load Capacitance	10 pF
Total Power consumption	Minimum

III. DESIGN CALCULATIONS

This section presents a design procedure for a basic miller compensated two stage CMOS op amp with basic op amp equations.

Basic op amp Equations:

The following equations are the MOSFET, strong inversion, square law equations:

Drain current $I_D = \beta V_{OV}^2 = \frac{\mu_{n,p} C_{OX}}{2} * \left(\frac{W}{L}\right) * V_{OV}^2$ (3.1)

where $\beta = \frac{\mu_{n,p} C_{OX}}{2} * \left(\frac{W}{L}\right)$

Aspect ratio $\frac{W}{L} = \frac{2I_D}{\mu_{n,p} C_{OX} * V_{OV}^2}$ (3.2)

Transconductance, $g_m = \sqrt{2 * \mu_{n,p} C_{OX} * \left(\frac{W}{L}\right) * I_D}$ *(3.3)*

$g_m = \frac{2 * I_D}{V_{OV}}$ *(3.4)*

Where V_{OV} = (V_{GS} -V_{tn}) for NMOS and V_{OV} = (V_{SG} -$|V_{tp}|$) for PMOS, will be used throughout the paper. Strong inversion typically requires values of V_{OV} greater than approximately 200mV for bulk MOSFET's room temperature [3].

STEP 1: Design the compensation capacitor C_c in such a way that placing the pole P_2 , 2.2 times higher than the Gain bandwidth product (GB) permitted a 60^0 phase margin. This results in the following requirement for the minimum value for C_c .

$$C_c > \frac{2.2}{10} * C_L$$
$$C_c > \frac{2.2}{10} * 10 * 10^{-12}$$
$$C_c > 2.2 * 10^{-12}$$

Choose C_c=2.3pF

STEP 2: The next step of the design is the estimation of the bias current. From the slew rate specification, we have

Slew rate (SR) = $\frac{I_{SS}}{C_c} = \frac{I_5}{C_c}$

Where I_{SS} (=I_5) is the tail current.

$$I_5 = S.R * C_c = 50 * 10^6 * 2.3 * 10^{-12}$$
$$= 115\ \mu A$$

STEP 3: Assuming the GB established by the dominant node, we have

$$g_{m1} = GB * C_c = 2 * \prod * f * C_c$$
$$g_{m1} = 120 * 10^6 * 2.3 * 10^{-12}$$
$$= 0.0017 = 1.7\ m\ \Omega^{-1}$$
$$\left(\frac{W}{L}\right)_{1,2} = \frac{(g_{m,1})^2}{K_n * I_5}$$
$$= \frac{(1.7 * 10^{-3})^2}{343.2 * 10^{-6} * 115 * 10^{-6}}$$
$$= 73.22$$

STEP 4: Design for $\left(\frac{W}{L}\right)_{3,4}$ from the maximum input voltage specification.

$$\left(\frac{W}{L}\right)_{3,4} = \frac{I_5}{K_p * [V_{DD} - V_{in}(max) - |V_{tp,3}|(max) + V_{tn,1}(min)]^2}$$
$$\left(\frac{W}{L}\right)_{3,4} = \frac{115 * 10^{-6}}{70.4 * 10^{-6}[1.65 - 1.3 - 0.42 + 0.42)]^2}$$
$$= 14$$

STEP 5: Design for $\left(\frac{W}{L}\right)_5$ from the minimum input voltage. First we have to calculate $V_{DS5}(sat)$ then find S5.

$$V_{DS5} = V_{in}(min) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{tn,1}(max)$$
$$= -0.8 - (-1.65) - \sqrt{\frac{115 * 10^{-6}}{343.2 * 10^{-6} * \frac{73.22}{2}}} - 0.57$$
$$= 0.1867$$
$$\left(\frac{W}{L}\right)_5 = \frac{2I_5}{K_n C_{OX} * V_{DS5}^2} = \frac{2 * 115 * 10^{-6}}{343.2 * 10^{-6} * (0.1867)^2} = 19.22$$

STEP 6: Find g_{m6} , g_{m4} to design $\left(\frac{W}{L}\right)_6$

For required Phase margin

$$g_{m6} = 10 * g_{m1}$$
$$= 10 * 1.7 * 10^{-3}$$
$$= 17\ m\ \Omega^{-1}$$
$$g_{m3} = \sqrt{\frac{2 * K_p * \left(\frac{W}{L}\right)_3 * I_5}{2}}$$
$$= \sqrt{\frac{2 * 70.4 * 10^{-6} * 14 * 115 * 10^{-6}}{2}}$$
$$= 0.337\ m\ \Omega^{-1}$$

Let $V_{SG,4} = V_{SG,6}$

Therefore, $\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_4 * \frac{g_{m,6}}{g_{m,4}}$

$$= 14 * \frac{17 * 10^{-3}}{0.337 * 10^{-3}}$$

$$= 706.23$$

STEP 7: Calculate I_6 flowing through M6

$$I_6 = \frac{(g_{m,6})^2}{2 * K_p * \left(\frac{W}{L}\right)_6}$$

$$= \frac{(17 * 10^{-3})^2}{2 * 70.4 * 10^{-6} * 706.23}$$

$$= 2.9 \text{ mA}$$

STEP 8: Design $\left(\frac{W}{L}\right)_7$ to achieve the desired current ratios between I_6 and I_5

$$\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_5 * \frac{I_6}{I_5}$$

$$= 19.22 * \frac{2.9 * 10^{-3}}{115 * 10^{-6}}$$

$$= 484.67$$

STEP 9: Design $\left(\frac{W}{L}\right)_8$ by relationship relating to load, compensation capacitors, and $\left(\frac{W}{L}\right)_6$

$$\left(\frac{W}{L}\right)_8 = \frac{\left(\frac{W}{L}\right)_6}{1+\frac{C_L}{C_c}} = \frac{706.23}{1+\frac{10 * \mathbf{10^{-12}}}{\mathbf{2.3} * \mathbf{10^{-12}}}} = 132$$

IV. STABLE TRANSCONDUCTANCE BIASING

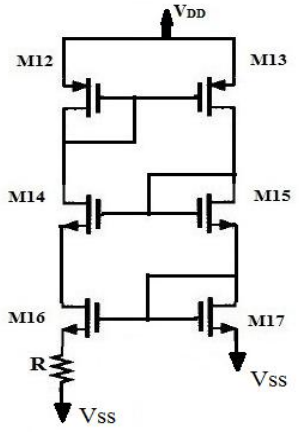

Fig. 2. Stable Trans-conductance biasing [4]

The bias circuit shown in Fig. 2 is used to stabilize the transistor trans-conductance of the op amp since it supplies constant bias current to the op amp. Biasing circuit is independent of power supply voltage variations.

Writing KVL to the loop as shown in Fig. 2

$$\mathbf{V_{GS,M17}} = \mathbf{V_{GS,M16}} + \mathbf{I_{D,M16}} * \mathbf{R}$$

$$\sqrt{\frac{\mathbf{2I_{D,M17}}}{\mathbf{K_n}*\left(\frac{\mathbf{W}}{\mathbf{L}}\right)_{\mathbf{M17}}}} + \mathbf{V_{TH,M17}} = \sqrt{\frac{\mathbf{2I_{D,M16}}}{\mathbf{K_n}*\left(\frac{\mathbf{W}}{\mathbf{L}}\right)_{\mathbf{M16}}}} + \mathbf{V_{TH,M16}} +$$

$\mathbf{I_{D,M16}} * R$

Since $\left(\frac{\mathbf{W}}{\mathbf{L}}\right)_{\mathbf{M12}} = \left(\frac{\mathbf{W}}{\mathbf{L}}\right)_{\mathbf{M13}}$,

There fore $\mathbf{I_{D,M16}} = \mathbf{I_{D,M17}}$.

Neglecting body effect,

we have $\sqrt{\frac{\mathbf{2I_{D,M16}}}{\mathbf{K_n}*\left(\frac{\mathbf{W}}{\mathbf{L}}\right)_{\mathbf{M17}}}} - \sqrt{\frac{\mathbf{2I_{D,M16}}}{\mathbf{K_n}*\left(\frac{\mathbf{W}}{\mathbf{L}}\right)_{\mathbf{M16}}}} = \mathbf{I_{D,M16}} * \mathbf{R}$

From the above equation it is observed that

$\left(\frac{\mathbf{W}}{\mathbf{L}}\right)_{\mathbf{M17}}$ & $\left(\frac{\mathbf{W}}{\mathbf{L}}\right)_{\mathbf{M16}}$ should not have same value.

For a special case,

$$\left(\frac{\mathbf{W}}{\mathbf{L}}\right)_{\mathbf{M16}} = 4 * \left(\frac{W}{L}\right)_{M17}$$

Re-arranging the above equation

$$\frac{2}{\sqrt{2 * I_{D,M16} * \mu_n C_{ox} * \left(\frac{W}{L}\right)_{M17}}} \left\{1 - \left(\sqrt{\frac{\left(\frac{W}{L}\right)_{M17}}{\left(\frac{W}{L}\right)_{M16}}}\right)\right\} = R$$

Recalling Trans-conductance,

$$g_{m,M17} = \sqrt{2 * K_n * \left(\frac{W}{L}\right)_{M17} * I_{D,M16}}$$

Therefore, $g_{m,M17} = \frac{2}{R}\left\{1 - \left(\sqrt{\frac{\left(\frac{W}{L}\right)_{M17}}{\left(\frac{W}{L}\right)_{M16}}}\right)\right\}$

$$g_{m,M17} = \frac{1}{R}$$

$g_{m,M17}$ Depends on 'R', Changing 'R' value gives required bias current.

Since the aspect ratios for the transistors in the biasing circuit shown in Fig. 3.5 are as follows.

$\left(\frac{W}{L}\right)_{M12} = \left(\frac{W}{L}\right)_{M13} = \left(\frac{W}{L}\right)_{M14} = \left(\frac{W}{L}\right)_{M15}$ and

$\left(\frac{W}{L}\right)_{M16} = 4 * \left(\frac{W}{L}\right)_{M17}$

V. SIMULATION RESULTS

This section presents various simulation results of electrical characteristics of two stage op amp such as unity gain frequency, slew rate, Input common mode range, output and input offset voltages, power supply rejection ratio(PSRR) and output swing plots.

A. Circuit schematic

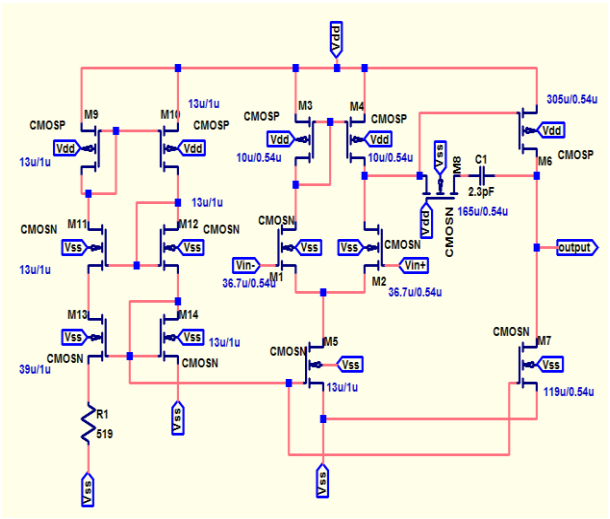

Fig. 3. Two stage miller compensated op-amp

TABLE III
ASPECT RATIOS

Device Name	(W/L) in µm through Design calculations	(W/L) in µm after optimization
M1,M2	39.53 / 0.54	36.7 /0.54
M3,M4	7.56 / 0.54	10 / 0.54
M5	19.22 / 1	13 / 1
M6	381.36 / 0.54	305 / 0.54
M7	261.72 / 0.54	119 / 0.54
M8	71.28 / 0.54	165 / 0.54
M12-M13	-	13/1
M14-M15	-	13/1
M16	-	39/1
M17	-	13/1

B. Frequency response

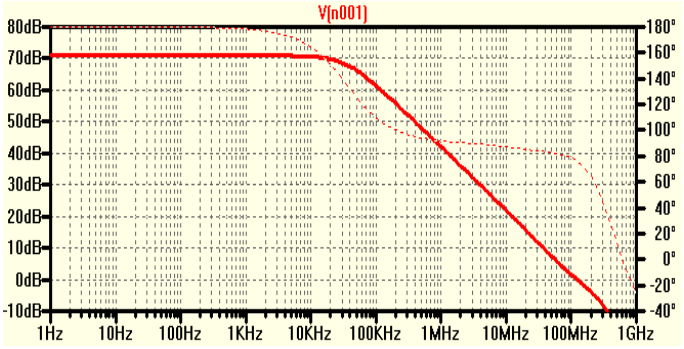

Fig.4. Frequency response of two stage op-amp

C. DC Transfer Characteristics

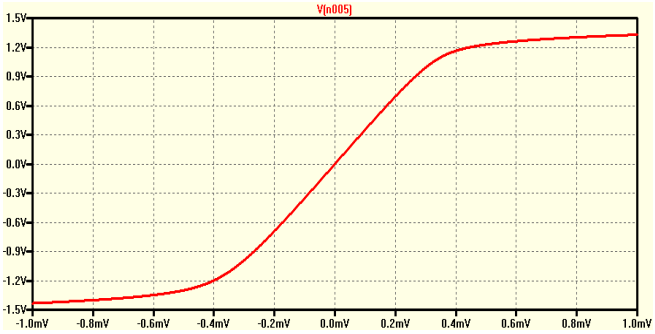

Fig. 5. DC Transfer Characteristics of two stage opamp

D. Output and input offset voltages

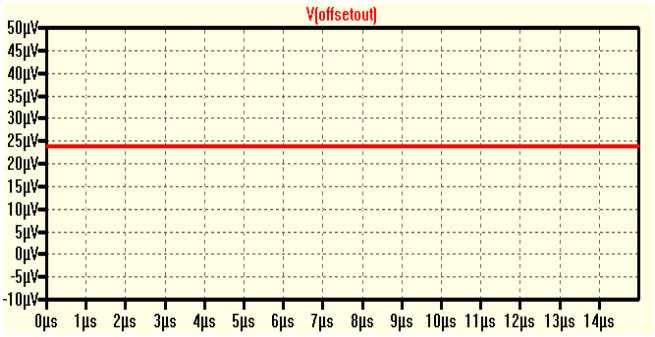

Fig . 6. Output offset voltage of two stage opamp

As seen from Fig. 6, the output offset of the amplifier is observed as 23.88 µV.

And the Input offset voltage of the op amp is given by

$$\text{Input offset voltage} = \frac{\text{output offset voltage}}{\text{Open loop DC gain}}$$

$$= \frac{23.88\ \mu V}{3536}$$

$$= 6.75nV$$

E. Input Common Mode Range (ICMR):

ICMR is measured as the range of voltages where the current through I_d(M5) begins to saturate until output voltage follows the input voltage.

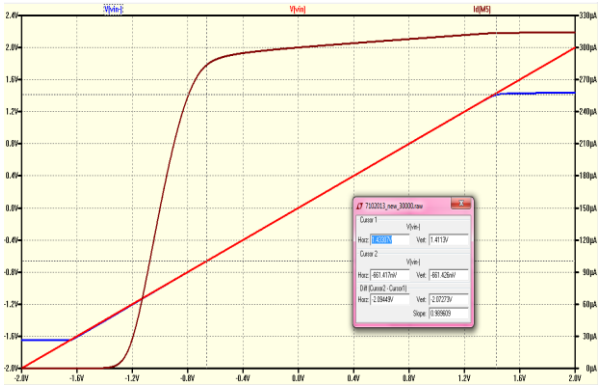

Fig . 7. ICMR of two stage opamp

F. Positive slew rate

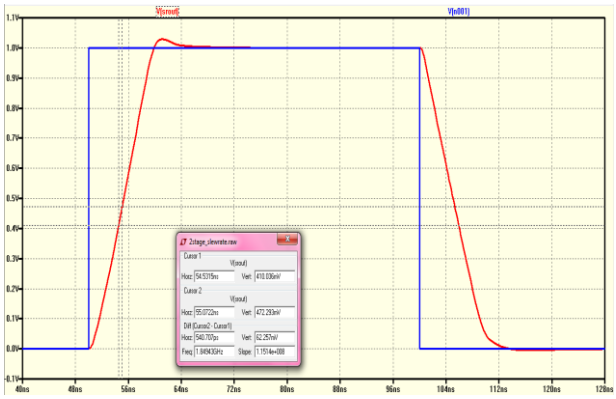

Fig . 8. Positive slew rate of two stage opamp

G. Negative slew rate

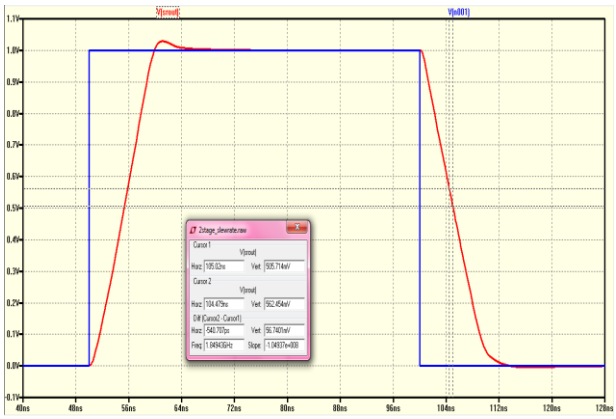

Fig . 9. Negative slew rate of two stage opamp

H. Settling time (t_s):

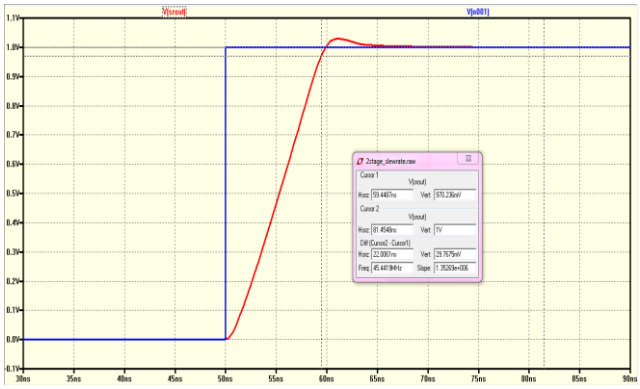

Fig . 10. Settling time (t_s) of two stage opamp

I. Positive Power supply rejection ratio(P-PSRR)

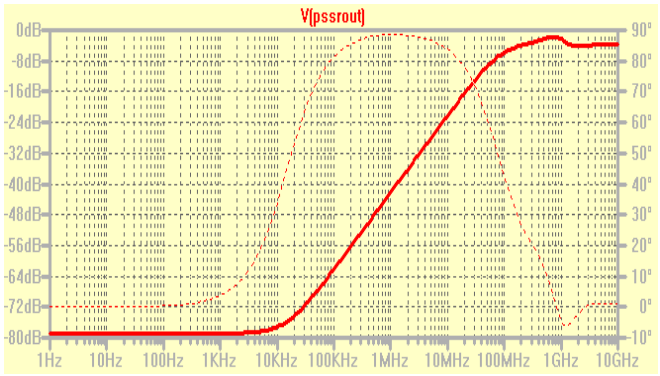

Fig . 11. (P-PSRR) of two stage opamp

J. Negative Power supply rejection ratio(N-PSRR)

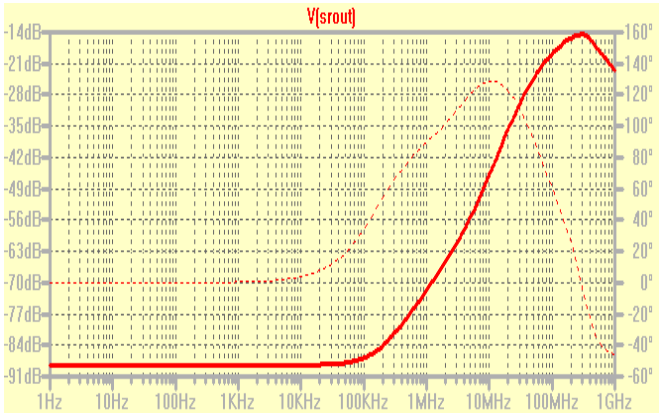

Fig . 12. (N-PSRR) of two stage op amp

K. Noise

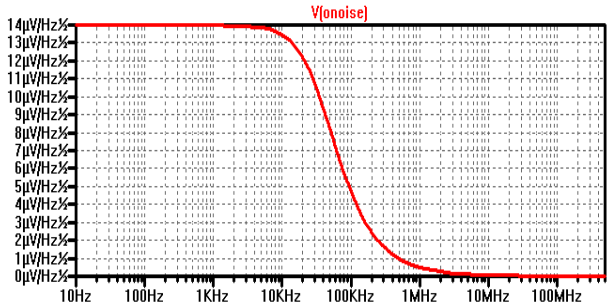

Fig. 12. Noise simulation *of* two stage op amp

TABLE IIII
PERFORMANCE SUMMARY

Name of the Parameter	Design Specification	Simualtion results
Bias current	150µA	300µA
Open loop gain (A)	> 70dB	70.97 dB
Gain –band width product (GB)	120MHz	120.078MHz
Phase margin (P.M)	≥ 60 degrees	76.5 degrees
Output offset voltage	< 5mV	23.88 µV
Input offset voltage	-	6.75nV
Positive slew rate	≥ 50 V/ µs	115.14 V/ µs
Negative slew rate	-	104.93 V/ µs
Output voltage range	$\geq 2V_{p-p}$	$2V_{p-p}$
Input common mode range (ICMR)	- 0.8 to 1.3V	-0.66 to 1.41V
Load capacitance	10 pF	5pF
Setlling time	-	22ns
Positive PSRR	-	78.8dB
Negative PSRR	-	88.5dB
Noise	-	$14\ \frac{\mu V}{\sqrt{Hz}}$
Total power consumption	Minimum	16.5mW

VI. CONCLUSIONS

In this paper the design of single ended miller compensated two stage operational amplifier presented with detailed design calculations. Simulation results shows that op amp have open loop DC gain of 70.97dB , unity gain frequency of 120MHz and output swing voltage of 2 volts peak-to-peak. An op amp provides appropriate DC gain and output offset voltage of 23.88 µV to match the signal to the input range of ADC.

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