Design of Low Power Universal Shift Register

[1] Saranya.M, [2]V.Vijayakumar, [3]T.Ravi, [4]V.Kannan
[1] *M.Tech-VLSI design, Sathyabama University, Jeppiaar Nagar, Rajiv Gandhi Salai, Chennai 119*
[2] *Assistant Professor, Sathyabama University, Jeppiaar Nagar, Rajiv Gandhi Salai, Chennai 119.*
[3] *Assistant Professor, Sathyabama University, Jeppiaar Nagar, Rajiv Gandhi Salai, Chennai 119.*
[4] *Principal, Jeppiaar Institute of Technology, Kunnam, Tamilnadu, India.*

Abstract

Universal shift registers, as all other types of registers, are used in computers as memory elements. Flip-flops are an inherent building block in Universal shift registers design. Furthermore flip-flops constitute most of the load on the clock distribution and power networks, which are the main power consuming block in Universal shift registers. In order to achieve Universal shift registers, that is both high performances while also being power efficient, careful attention must be paid to the design of flip flops. The paper presents a new design for implementing a static Master-Slave Flip-flop with reduced transistor count for low power and high performance applications. The proposed flip-flop is realized using only nine transistors (including an inverter to produce complementary clock signals locally) hence reducing the manufacturing cost. HSPICE simulation results of Universal Shift Register at a frequency of 250 MHz indicate improvement in power-delay product with respect to the conventional static Master-Slave flip flop configurations.

1. Introduction

A universal shift register is an integrated logic circuit that can transfer data in three different modes. Like a parallel register it can load and transmit data in parallel. Like shift registers it can load and transmit data in serial fashions, through left shifts or right shifts. In addition, the universal shift register can combine the capabilities of both parallel and shift registers to accomplish tasks that neither basic type of register can perform on its own. For instance, on a particular job a universal register can load data in series (e.g. through a sequence of left shifts) and then transmit/output data in parallel. Universal shift registers, as all other types of registers, are used in computers as memory elements. Although other types of memory devices are used for the efficient storage of very large volume of data, from a digital system perspective when we say computer memory we mean registers. In fact, all the operations in a digital system are performed on registers. Examples of such operations include multiplication, division, and data transfer.

Due to increasing demand of battery operated portable handheld electronic devices like laptops, palmtops and wireless communication systems (personal digital assistants and personal communicators) the focus of the VLSI industry has been shifted towards low power and high performance circuits. Flip-flops and latches are the basic sequential elements used for realizing digital systems like Universal shift Register. The flip-flops used in digital systems can be either dynamic or static based on their functionality when the clock is stopped/grounded, but the power is maintained.

From a low power perspective, flip-flops are clocked at the operating frequency of the system and consume about 30%-70% of the total power dissipation in the system which also includes the power dissipated in the clocking network of latches and flip-flops is prime The maximum speed at which synchronous systems can operate is determined by flip-flops since they are the starting and ending points of signal delay paths [13].

The remaining paper is organized as follows. Section II presents analysis about flip-flop power and performance metrics. Section III presents the design of TGMS D Flip Flop. Section IV outlines the Universal Shift register design. Using existing and proposed TGMS D flip Flop. Section V illustrates the simulation results. Finally, conclusions are summarized in Section VI.

2. Power And Performance Metrics

A. Power Characterization

The dynamic power consumption (P_D) in a circuit is estimated as

$$P_D = C V_{DD}^2 f$$

Where C is the load capacitance;
V_{DD} is power supply voltage;
f is operating frequency. [13]

Stojanovic & Oklobdzija proposed [2] that the total power dissipation is composed of the following three components:

I. **Local data power dissipation** represents the power dissipated in the inverter driving the data input of the flip flop.

II. **Clock power dissipation** represents the power consumption of the inverter driving the clock input of the flip flop.

III. **Internal power dissipation** includes the intrinsic power dissipated on switching of the internal nodes of the flip-flop excluding the load capacitance.

B. Performance Metrics

The basic performance metrics that are used to qualify a flip-flop and compare it to other designs are

• **Clock-to-Q delay**: Propagation delay forms the clock terminal to the output Q terminal. This is assuming that the data input D is set early enough with respect to the effective edge of the clock input signal.

• **Setup time**: The minimum time needed between the D input signal change and the triggering clock signal edge on the clock input. This metric guarantees that the output will follow the input in worst case conditions of process, voltage and temperature (PVT). This assumes that the clock triggering edge and pulse has enough time to capture the data input change.

• **Hold time**: The minimum time needed for the D input to stay stable after the occurrence of the triggering edge of the clock signal. This metric guarantees that the output Q stays stable after the triggering edge of the clock signal occurs, under worst PVT conditions. This metric assumes that the D input change happened at least after a minimum delay from the previous D input change, this minimum delay is the setup time of the flip-flop.Yet another parameter is D-Q delay or (Tset-up + Tcq) which determines the minimum clock time period for master–slave structures. **Stojanovic & Oklobdzija [2]** showed that D-Q delay is the real performance factor and not CLK-Q delay because D-Q delay also takes into account optimum set-up time which is positive for master–slave flip-flop structures.

C. Power-Delay Product

In VLSI, there is always a trade-off between power and performance. A flip-flop can be optimized for either high performance or low power but both the parameters are critical, so generally we want power–delay product to be minimum, which means that the flip-flop operates at optimum energy under a given frequency. Several metrics are available for comparative analysis of digital circuits. PDP (power-delay product) based metric is generally used for low power portable systems where battery life is the prime concern.

3. Design Of TGMS D Flip Flop

The design shown in Figure 1 is Transmission Gate Based Master Slave D Flip Flop [1]. The TGs T1 and T2 act as latches in the master and slave sections while inverted and non-inverted clock signals CLK and CLKB are generated locally by using an inverter INV3. To make the flip-flop static in nature a feedback is provided from the output node to a specific internal node in the master-stage as shown in Figure. 1. This feedback is employed keeping in mind that there are exactly two inversions in the forward path. The feedback strategy used in the design is entirely different with respect to the conventional static designs, which used two feedback loops one each in the master as well as the slave stage, which increased the total parasitic capacitance at the internal flip-flop nodes, leading to higher dynamic power dissipation and reduced performance. This also resulted in total chip area overhead due to increased transistor count. The whole idea was to reduce the transistor count and lower the power consumption, but some of the other important aspects like performance and low voltage operation of flip flops remained completely unexplored. But using TGs in the critical path leads to highest performance and symmetrical delays unlike (3-T) clocked inverter based designs which produce unsymmetrical H-L and L-H delays leading to glitches. This can further lead to unnecessary switching and enhanced power dissipation. Moreover, TG based flip flops display undeterred functionality even at much lower supply voltages due to higher driving capabilities.

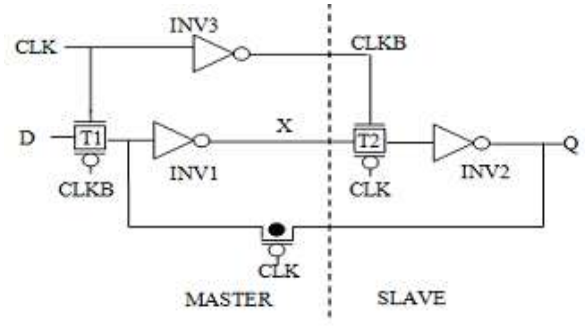

FIGURE 1. TGMS D FLIP FLOP

The proposed design is shown in Figure 2 . Its structure is based on master-slave configuration and the Master and the slave stages are clearly demarcated.

Operating Mode	S1	S0
Locked	0	0
Shift-Right	0	1
Shift-Left	1	0
Parallel Loading	1	1

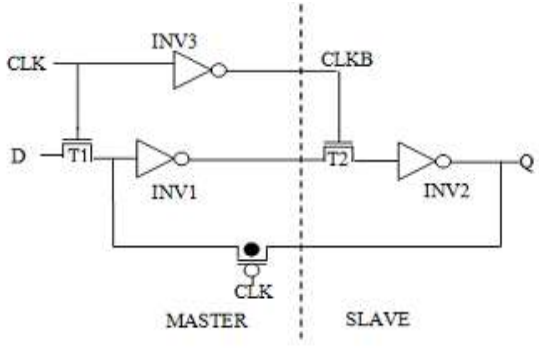

FIGURE 2. PROPOSED TGMS D FLIP FLOP

The proposed design D Flip Flop is static in nature by connecting the output to the input through a PMOS transistor operated by CLK. Even though the TGMS D flip flop have reduced number of transistor count, there is still possibility of increased power consumption due to clock load and its related power consumption.

The above proposed design is an attempt to reduce the clock load and its related power consumption.

4. DESIGN OF UNIVERSAL SHIFT REGISTER

With this existing and proposed design of TGMS flip flop, 4 bit Universal shift register is designed and the simulation results are shown in the next section. The proposed Universal shift register is aimed at reducing the transistor count and lower the power consumption.

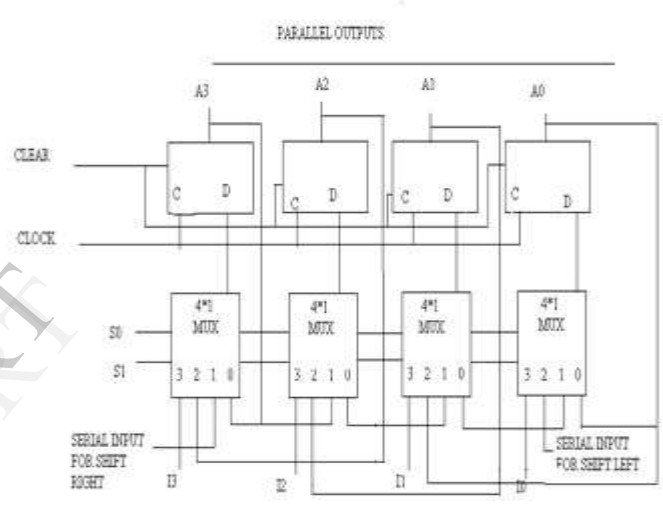

FIGURE 3. UNIVERSAL SHIFT REGISTER

In the locked mode (S1S0 = 00) the register is not admitting any data; so that the content of the register is not affected by whatever is happening at the inputs. In the shift-right mode (S1S0 = 01) serial inputs are admitted from Q3 to Q0. In the shift-left mode (S1S0 = 10) the register works in a similar fashion, except that the signals move from Q0 to Q3. Finally, in the parallel loading mode (S1S0 = 11) data is read from the lines I0, I1, I2, and I3 simultaneously.

Initially Universal shift register is designed with the conventional static master slave flip flop and its operation are analysed. Then the universal shift register with proposed D flip flop is designed. As the proposed flip flop is proved to be efficient in both power and speed, so as Universal shift register.

5. SIMULATION RESULTS

The designs were made with 130 nm CMOS technology in HSPICE software. All simulations are performed at nominal conditions: VDD =3.3V and at room temperature (25°C), which demonstrates the power and performance of the design at lower supply voltages. The clock frequency is kept at 250 MHz

The transient analysis of TGMS D Flip flop and the proposed design is given below.

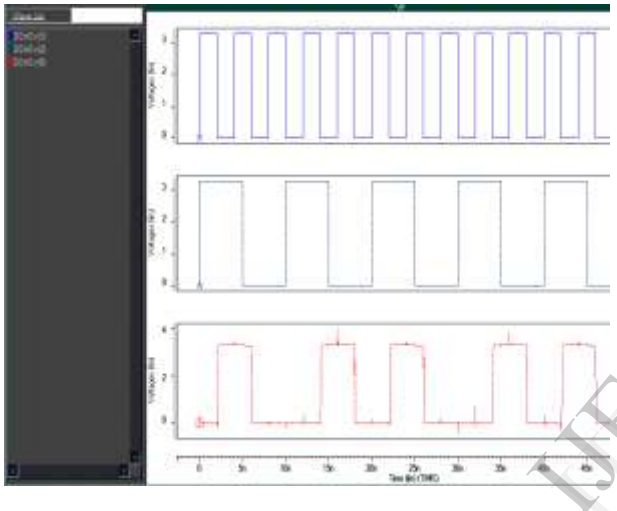

FIGURE 4. TGMS D FLIP FLOP

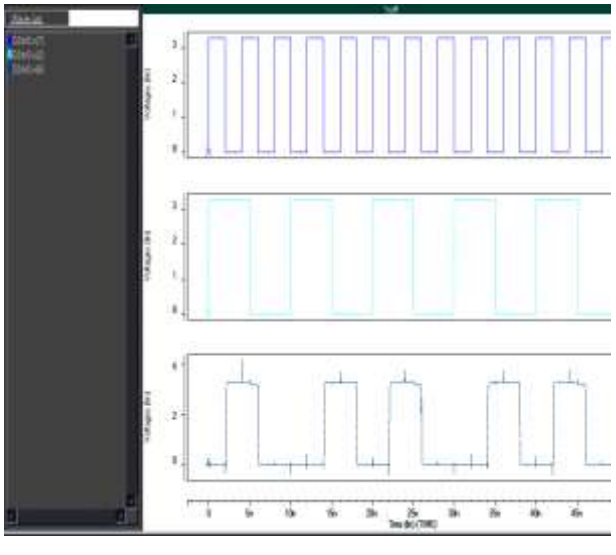

FIGURE 5. PROPOSED D FLIP FLOP

The transient analysis of Universal shift register using TGMS D Flip flop and the proposed design is given below.

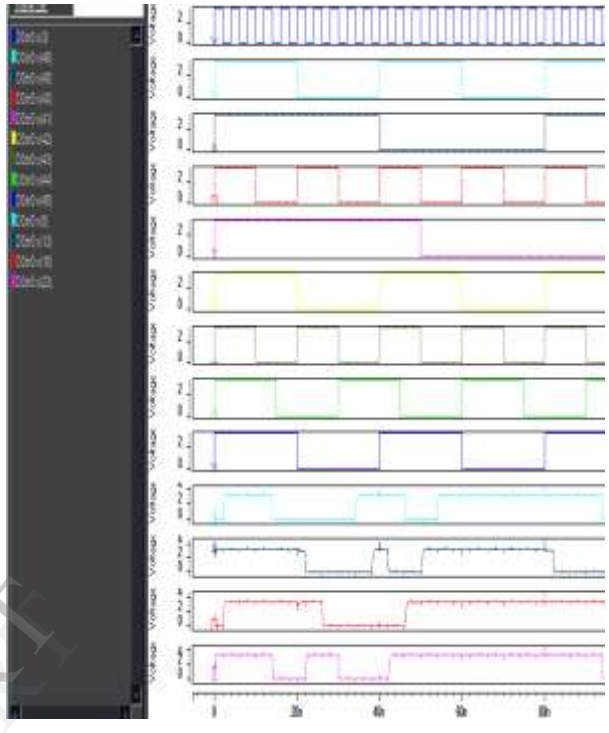

FIGURE 6. UNIVERSAL SHIFT REGISTER USING TGMS D FLIP FLOP

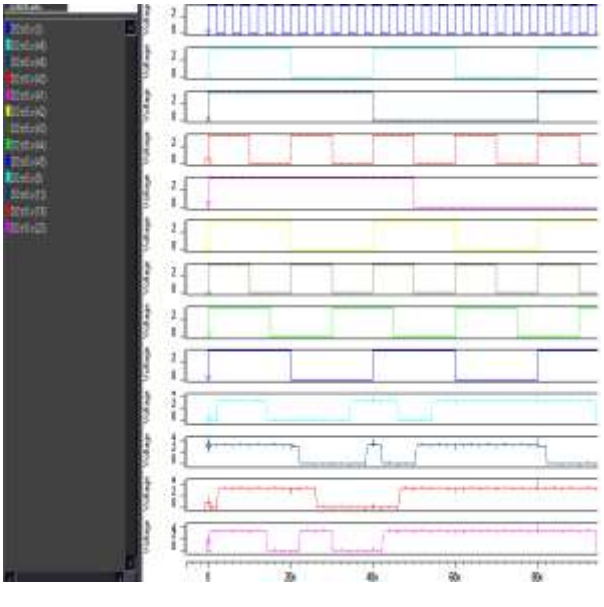

FIGURE 7. UNIVERSAL SHIFT REGISTER USING PROPOSED TGMS D FLIP FLOP

Comparison Table of Existing and Proposed Work

Design	Transistor Count (Including Clock inverter)	Average Power (uW)
TGMS D Flip Flop	**11**	**2.177**
Proposed Design D Flip Flop	**9**	**1.524**
Universal shift register using Existing Flip Flop	**106**	**33.223**
Proposed Universal shift register	**98**	**25.14**

6. CONCLUSION

Thus the new design of a static Master-Slave Flip-flop based Universal shift register with reduced transistor count renders better efficiency in terms of power and area reduction. The proposed Universal shift register is investigated using the standard parameters, optimization techniques and extensive simulation procedure and the results of the HSPICE simulation indicate that the proposed design is ideally suited for low power and high performance systems

10.References

[1]. Kunwar Singh, Satish Chandra tiwari and Maneesha Gupta, "A High Performance Flip Flop for Low Power Low Voltage System", *IEEE* 2011

[2] Vladimir Stojanovic and Vojin G.Oklobdzija, "Comparative Analysis of Master-Slave Latches and Flip-Flops for High –Performance and Low-Power System," IEEE J. Solid-State Circuits, vol.34, pp.536-548, April 1999.

[3] Yu Chien-Cheng "Design of Low-Power Double Edge-Triggered Flip-Flop Circuit" 2007 Second IEEE Conference on Industrial Electronics and Applications 23-25 May 2007 pp 2054-2057.

[4] M. Alioto, E. Consoli, and G. Palumbo, "Flip-flop energy/performance versus clock slope and impact on the clock network design," IEEE Trans. Circuits Syst. I, Vol 57, No 6, Jun 2010.

[5] M. Nogawa and Y. Ohtomo, "A data-transition look-ahead DFF circuit for statistical reduction in power consumption," in Symp. VLSI Circuits Dig. Tech. Papers, June 1997, pp. 101–102.

[6] A. Sayed and H. Al-Asaad, "A new low power high performance flip-flop", Proc. International Midwest Symposium on Circuits and Systems, 2006.

[7] Peiyi Zhao, Jason McNeely, Weidong Kuang, Nan Wang, and Zhongfeng Wang," Design of Sequential Elements for Low Power Clocking System"IEEE Trans on VLSI,vol 19, No 5 May 2011

[8] Gary K.Yeap, Practical Low power Digital VLSI Design, Kluwer Academic Publishers, 1998.

[9] Vladimir Stojanovic and Vojin G.Oklobdzija, Comparative, "Analysis of Master-Slave Latches and Flip-Flops for High –Performance and Low-Power System," IEEE J. Solid-State Circuits, vol.34, pp.536-548, April 1999.

[10] Gaetano Palumba and Melita pennisi, " Design Guidelines for High-speed Transmission Gate Latches: Analysis and Compaison.

[11]. J. Rabaey, A. Chandrakasan, B. Nikolic, Digital Integrated Circuits, 2nd edition, Prentice Hall, 2003.

[12]. V.G. Oklobdzija, V. Stojanovic, D.M.Markovic, N.M. Nedovic, Digital System Clocking. High Performance and Low Power Aspects, Wiley-Interscience, 2003.

Saranya.M was born in Vellore, Tamil Nadu, India. She received her Bachelor Degree in Electronics and Communication Engineering from Anna University in 2009. She is currently doing her Master Degree in VLSI DESIGN from Sathyabama University. Her interested areas are Microwave Engineering, VLSI Design. She has Research publications in National / International Journals / Conferences.

V.Vijayakumar was born in Tiruvarur, Tamilnadu,India in 1983. He received his Bachelor Degree in Physics from Bharathidasan University in the year 2003, Master Degree in Physics from Bharathidasan University in the year 2006. Master Degree in VLSI DESIGN from Sathyabama University in the year 2008. Currently he is doing Ph.D in Sathyabama University. He is working as Assistant Professor in Department of ECE in Sathyabama University. His interested areas of research are Nano Electronics, VLSI Design, He has Research publications in National / International Journals / Conferences.

T.Ravi was born in Namakkal, Tamilnadu, India in 1978. He received his Bachelor Degree in Electrical and Electronics Engineering from Madurai Kamaraj University in the year 2001, Master Degree in Applied Electronics from Sathyabama Deemed University in the year 2004. Currently he is doing Ph.D in Sathyabama University. He is working as Assistant Professor in Department of ECE in Sathyabama University. His interested areas of research are Nano Electronics, VLSI Design, Low Power VLSI Design and Mixed Signal circuits. He has Research publications in National / International Journals / Conferences. He is a member of VLSI Society of India.

Dr.V.Kannan was born in Ariyalore, Tamilnadu, India in 1970. He received his Bachelor Degree in Electronics and Communication Engineering from Madurai Kamaraj University in the year 1991, Master Degree in Electronics and control from BITS, Pilani in the year 1996 and Ph.D., from Sathyabama University, Chennai, in the year 2006. His interested areas of research are Optoelectronic Devices ,VLSI Design, Nano Electronics, Digital Signal Processing and Image Processing. He has 150 Research publications in National / International Journals / Conferences to his credit. He has 21 years of experience in teaching and presently working as Principal, Jeppiaar Institute of Technology, Kunnam, Tamilnadu, India. He is a life member of ISTE.