

Design of Low-Power Hybrid Full Adders using Full-Swing XOR–XNOR Gates

Dasari Yugandhar¹, Agatamudi Harsha Vardhini²

Electronics and Communication Engineering / Aditya Institute of Technology and Management/ Tekkali, India

Corresponding author: MIG-199, APHB Colony, Opposite ZP Office, Srikakulam, Andhra Pradesh-532001

Abstract: This paper presents a family of hybrid 1-bit full-adder circuits based on full-swing XOR/XNOR and simultaneous XOR–XNOR logic. The proposed architecture combines the XOR–XNOR block with transmission-gate-based 2:1 multiplexers to generate the Sum and Carry outputs. Six hybrid full-adder variants are described: HFA-20T, HFA-17T, HFA-B-26T, HFA-NB-26T, HFA-22T, and HFA-19T. The designs target low power dissipation, reduced propagation delay, low output capacitance, full-swing operation, and improved driving capability. The manuscript also considers the use of the proposed full-adder cells in ripple-carry structures. The study reports circuit-level simulation and investigates the effects of supply voltage, output capacitance, threshold voltage, input noise, and transistor sizing. The proposed structures are intended for low-power VLSI applications such as arithmetic units, digital signal processing, and microprocessors. Quantitative power, delay, and power-delay-product results should be inserted after final verification of the simulation setup.

Keywords: full adder; XOR; XNOR; XOR–XNOR; hybrid logic; transmission gate; low-power VLSI; power-delay product; ripple-carry adder

I. INTRODUCTION

Arithmetic circuits are fundamental components of digital systems, and adders form an important building block for arithmetic and data-processing operations. Full adders are used in arithmetic logic units, multipliers, address-generation circuits, digital signal processors, and related VLSI systems. As integration density increases and portable electronics demand lower energy consumption, full-adder implementations must balance power, propagation delay, area, output swing, and driving capability.

The proposed study identifies XOR/XNOR logic as a major contributor to the power and delay of a full-adder cell. Conventional implementations based on CMOS, complementary pass-transistor logic, transmission-gate logic, and hybrid approaches provide different trade-offs. In particular, non-full-swing internal nodes, excessive output capacitance, and NOT gates on critical paths can degrade the overall performance of a hybrid adder.

The objective of this work is to develop and organize a family of hybrid full-adders around a full-swing XOR/XNOR or simultaneous XOR–XNOR circuit and a transmission-gate 2:1 multiplexer. The resulting designs are intended to reduce power and delay while retaining full-swing outputs and practical driving capability.

II. MATERIALS AND METHODS

A 1-bit full adder has three inputs, A, B, and Cin, and two outputs, Sum (S) and Carry-out (Cout). The Boolean equations used in the source manuscript are:

$$S = A \oplus B \oplus C_{in}$$

$$C_{out} = (A \cdot B) + (C_{in} \cdot (A \oplus B))$$

The functional truth table of the 1-bit full adder is presented as Table 1

Table 1: Truth table of the 1-bit full adder.

A	B	Cin	Cout	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

The proposed family uses a hybrid logic structure in which a full-swing XOR/XNOR or simultaneous XOR–XNOR circuit supplies the data inputs of transmission-gate 2:1 multiplexers. The carry input is used as a selection signal. This organization follows the functional relationships identified in the source manuscript: when Cin = 0, the Sum output follows $A \oplus B$ and the Carry output follows $A \cdot B$; when Cin = 1, the corresponding data functions are $A \text{ XNOR } B$ and $A + B$.

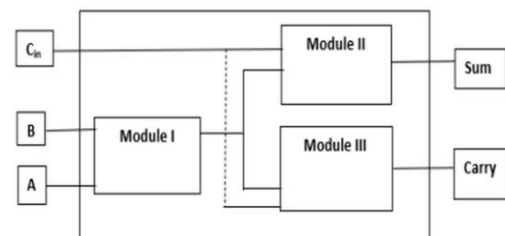


Fig. 1 Block diagram of hybrid logic FA circuit [3]

Fig 1: Block diagram of the hybrid full-adder architecture based on XOR/XNOR logic and transmission-gate multiplexers.

The XOR–XNOR block described in the manuscript uses six transistors, consisting of three PMOS and three NMOS devices. The design generates complementary XOR and XNOR outputs with full voltage swing. The proposed full-adder variants then modify buffering, critical-path inversion, and the use of the carry signal to control internal capacitance and output drive.

A. PROPOSED FULL-ADDER VARIANTS

HFA-20T: The HFA-20T uses the six-transistor XOR–XNOR block and two 2:1 transmission-gate multiplexers. The design contains 20 transistors and provides full-swing outputs. The HFA-20T has reduced output driving capability in chain applications as a limitation when no output buffering is used.

HFA-17T: The HFA-17T reduces the transistor count to 17 by generating one of the complementary signals through an inverter.

This reduces the number of transistors but places an inverter on the critical path, which can increase latency and short-circuit power.

HFA-B-26T: The HFA-B-26T introduces output buffers at the Sum and Carry outputs. The buffers improve the ability of the cell to drive practical loads, although the reported design analysis indicates an associated increase in delay and power relative to the smaller unbuffered cells.

HFA-NB-26T: The HFA-NB-26T places buffers at the data inputs of the 2:1 multiplexers. According to the manuscript, this arrangement can stabilize the multiplexer data nodes before the XOR/XNOR signals are generated. Its critical path contains the XOR–XNOR block and a 2:1 multiplexer, while its output driving capability is influenced by the multiplexer resistance.

HFA-22T and HFA-19T: These variants add the carry signal to the Sum-generation structure so that the XOR and XNOR nodes do not directly drive the Sum output. The study states that the resulting reduction in XOR/XNOR-node capacitance is expected to improve delay and power relative to the corresponding HFA-20T and HFA-17T structures, while the additional transistors can improve driving capability.

Table 2: Structural summary of the proposed full-adder cells.

Cell	T	Main structural feature
HFA-20T	20	XOR–XNOR + two TG 2:1 MUXs
HFA-17T	17	XOR/XNOR with inverter-generated complement
HFA-B-26T	26	Output buffers at Sum and Cout
HFA-NB-26T	26	Buffers at MUX data inputs
HFA-22T	22	HFA-20T with carry-assisted Sum path
HFA-19T	19	HFA-17T with carry-assisted Sum path

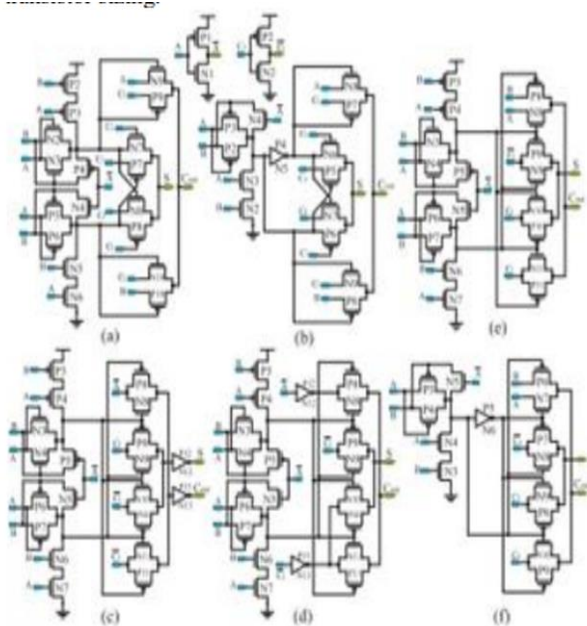


Fig.2. Proposed six new hybrid FA circuits. (a) HFA-20T. (b) HFA-17T. (c) HFA-B-26T. (d) HFA-NB-26T. (e) HFA-22T. (f) HFA-19T.

Fig 2: Six proposed hybrid full-adder circuits: HFA-20T, HFA-17T, HFA-B-26T, HFA-NB-26T, HFA-22T, and HFA-19T.

B. SIMULATION AND EVALUATION METHODOLOGY

The study describes transistor-level evaluation of the proposed circuits and discusses power consumption, propagation delay, power-delay product (PDP), output capacitance, supply voltage, threshold voltage, input noise immunity, and transistor sizing. A journal submission should report the exact simulator version, CMOS model, technology node, supply-voltage range, transistor dimensions, input

transition time, output load capacitance, simulation duration, and measurement definitions.

The study reports Tanner simulation with a 45-nm CMOS technology model in its abstract and earlier sections. The conclusion additionally reports Microwind simulations using 90-nm and 180-nm CMOS technology. Because these statements are not internally consistent, the final manuscript must identify one verified simulation flow or clearly separate multiple experimental setups before publication.

The principal metrics should be defined as follows: average power consumption, worst-case propagation delay, and power-delay product. For a consistent comparison, all competing cells should be simulated under identical supply voltage, technology, input activity, load capacitance, and transistor-sizing assumptions.

$$PDP = P_{avg} \times t_{pd}$$

The manuscript also discusses sensitivity to supply voltage, threshold voltage, output capacitance, input noise, and transistor sizing. These analyses should be reported using clearly specified parameter ranges and a consistent baseline configuration.

The final experimental description should state the simulator, CMOS technology node, supply voltage, load capacitance, input conditions, transistor dimensions, and measurement procedure consistently.

III. RESULTS

The truth table in Table 1 verifies the intended full-adder functionality. The proposed architecture derives the Sum and Carry outputs from complementary data functions selected by C_{in} , consistent with the full-adder equations given in Section 3.

The study also considers a ripple-carry implementation in which the carry output of one full-adder stage drives the carry input of the next stage. This structure is useful for assessing the driving capability and cumulative delay of the proposed cell.

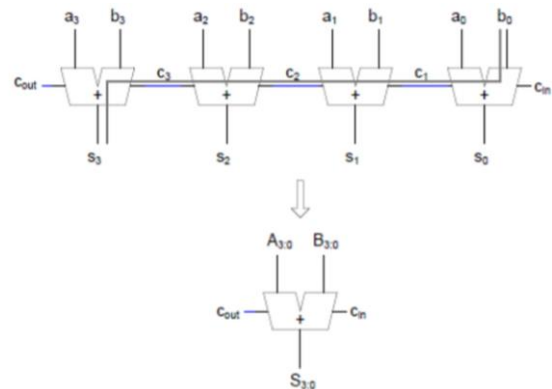


Fig 3: Four-bit ripple-carry adder structure using the proposed full-adder cell.

The supplied manuscript does not contain a complete extractable numerical table for power, delay, PDP, area, and technology node. These values should be inserted from the verified simulation outputs before submission.

IV. DISCUSSION

The architectural discussion indicates several design trade-offs. Reducing transistor count can reduce circuit complexity, but adding an inverter to the critical path can increase delay and short-circuit power. Output buffering can improve load-driving capability but introduces additional capacitance and switching activity. Conversely, reducing the capacitance of internal XOR/XNOR nodes can improve the delay and power characteristics of the overall full-adder cell. These trade-offs should be demonstrated quantitatively using a

common simulation environment rather than only qualitative statements.

For journal publication, the comparison should include representative conventional and hybrid full-adders from the cited literature. The comparison must use equivalent technology and test conditions, or the differences in technology and loading must be explicitly stated.

The proposed full-adder structures are intended for arithmetic and data-processing blocks in low-power VLSI systems. Potential application areas identified in the source manuscript include arithmetic logic units, digital signal processing, microprocessors, multipliers, address-generation circuits, comparators, parity circuits, and related arithmetic structures.

V. CONCLUSION

A family of six hybrid full-adder cells based on full-swing XOR/XNOR and simultaneous XOR–XNOR logic has been organized and described. The proposed architecture combines a compact XOR–XNOR block with transmission-gate multiplexers and optional buffering or carry-assisted signal routing. The six variants provide different trade-offs among transistor count, critical-path complexity, output driving capability, internal capacitance, power, and delay. The study indicates that these structures are intended for low-power and high-speed VLSI applications.

ACKNOWLEDGMENT

The authors may acknowledge institutional support, funding agencies, laboratory facilities, and technical assistance, where applicable.

CONFLICT OF INTEREST

The authors should declare any financial or personal relationships that could have influenced the work. If none, state: “The authors declare that they have no conflict of interest.”

REFERENCES

- [1] R. Rajaei and A. Amirany, “Nonvolatile Low-Cost Approximate Spintronic Full-Adders for Computing in Memory Architectures,” *IEEE Transactions on Magnetism*, vol. 56, no. 4, pp. 1–8, Apr. 2020.
- [2] E. Pakniyat, S. R. Talebiyan, and M. J. A. Morad, “Design of high performance and low power 16T full adder cell for sub-threshold technology,” in *Proc. IEEE International Congress on Technology, Communication and Knowledge (ICTCK)*, Mashhad, Iran, 2015, pp. 79–85.
- [3] D. Radhakrishnan, “Low voltage CMOS full adder cells,” *Electronics Letters*, vol. 35, no. 21, pp. 1792–1794, Oct. 1999.
- [4] J. Kandpal, A. Tomar, M. Agarwal, and K. K. Sharma, “High-Speed Hybrid-Logic Full Adder Using High-Performance 10-T XOR-XNOR Cell,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 6, pp. 1413–1422, Jun. 2020.
- [5] H. Naseri and S. Timarchi, “Low-power and fast full adder by exploring new XOR and XNOR gates,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 8, pp. 1481–1493, Aug. 2018.
- [6] H.-R. Basireddy, K. Challa, and T. Nikoubin, “Hybrid Logical Effort for Hybrid Logic Style Full Adders in Multistage Structures,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 5, pp. 1138–1147, May 2019.
- [7] M. Hasan, M. J. Hossein, M. Hossain, H. U. Zaman, and S. Islam, “Design of a Scalable Low-Power 1-bit Hybrid Full Adder for Fast Computation,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 8, pp. 1464–1468, Aug. 2020.
- [8] C. P. Kadu and M. Sharma, “Area-Improved High-Speed Hybrid 1-bit Full Adder Circuit Using 3T-XNOR Gate,” in *Proc. International Conference on Computing, Communication, Control and Automation (ICCUBE)*, 2017, pp. 1–5.
- [9] K. Sanapala and R. Sakthivel, “Ultra-low-voltage GDI-based hybrid full adder design for area and energy-efficient computing systems,” *IET Circuits, Devices & Systems*, vol. 13, no. 4, pp. 465–470, May 2019.
- [10] D. Abedi and G. Jaberipur, “Decimal Full Adders Specially Designed for Quantum-Dot Cellular Automata,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 1, pp. 106–110, Jan. 2018.
- [11] V. Kolla, T. Nagateja, and R. Vaddi, “Robust and energy efficient non-volatile reconfigurable logic circuits with hybrid CMOS-MTJs,” in *Proc. 3rd International Conference on Emerging Electronics (ICEE)*, 2016, pp. 1–5.
- [12] R. Rajaei and S. Bakhtavari Mamaghani, “Ultra-Low Power, Highly Reliable, and Non-volatile Hybrid MTJ/CMOS Based Full-Adder for Future VLSI Design,” *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 1, pp. 213–220, Mar. 2017.
- [13] M. Keerthana and T. Ravichandran, “Implementation of Low Power 1-bit Hybrid Full Adder using 22 nm CMOS Technology,” in *Proc. IEEE 6th International Conference on Advanced Computing and Communication Systems (ICACCS)*, Coimbatore, India, 2020, pp. 1215–1217.
- [14] P. Bhattacharyya, B. Kundu, S. Ghosh, V. Kumar, and A. Dandapat, “Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 10, pp. 2001–2008, Oct. 2015.
- [15] H. Thapliyal, F. Sharifi, and S. D. Kumar, “Energy-Efficient Design of Hybrid MTJ/CMOS and MTJ/Nanoelectronics Circuits,” *IEEE Transactions on Magnetism*, vol. 54, no. 7, pp. 1–8, Jul. 2018.