International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 4 Issue 04, April-2015

Design of Low Power CNTFET Based D Flip Flop using Sleep Transistor Technique

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***Abstract*— Digital designs in this era require small size and low power components. Scaling of CMOS technology results into various short and narrow geometry effects. One of those effects is subthreshold current (leakage current) which results into unnecessary power dissipation. CNTFET (Carbon Nanotube FET) is a novel approach to solve the problem of scaling. Leakage current power dissipation is reduced by sleep transistor configuration. Flip Flops are an essential part of digital designs. Reduction of power consumption in a Flip Flop is highly desirable. This paper is intended to accomplish a systematic analysis of low power consumption positive edge triggered D Flip Flop made using CNTFETs and in sleep transistor configuration. The proposed circuit has less power dissipation and can be used efficiently with low power circuitry. This proposed work is then compared with the performance analysis of conventional Complementary Metal Oxide Semiconductor and Carbon Nanotube FET circuit designs. The overall simulation and computation is performed using HSPICE.**

Keywords*— *D Flip Flop (DFF), Carbon Nanotube FET (CNTFET), Complementary Metal Oxide (CMOS), Subthreshold leakage current, Sleep Transistor, HSPICE.

I. INTRODUCTION

The current technological advancements require small low power devices that can be used in embedded systems. We use portable devices having compact structure. These compact structures need unit elements (MOS) to be of very small size. Small size can be made by implementing Scaling techniques on a Metal Oxide Semiconductor transistor, but due to numerous small scale and narrow scale geometry effects the scaling technique becomes unfeasible for further diminishment of CMOS transistor. For even smaller size we can use Carbon Nanotubes as a channel material. Carbon Nanotubes are specially designed tubes made up of graphene. These tubes have high conductivity and readily substitute the conventional channel material-Silicon in FETs. Now with CNTs as the channel material we can further scale down the Field Effect Transistor. CNTs also have superior mechanical and thermal properties. CNTFETs are very similar to CMOS and even the functionality of both the methodologies is similar. We can design almost all CMOS designs on CNTFET. The leakage current is one of the limiting factors for scaling of transistors [1]. The subthreshold leakage current evoked by the small scale geometries can be tackled by using sleep transistor configuration. Sleep transistor technique has various versions and usage designs [2]. Usage of sleep transistor increases the number of transistor but considerably reduces the power dissipation due to the leakage current.

D Flip Flop or the Delay flip flop is one of the sequential circuits that has been widely used for transistor based logic designs. Overall analysis presented in this paper is performed on a 16T D Flip Flop. The D Flip Flop is made using CNTFET and leakage current has been reduced using sleep transistor technique (stacking [3]).

This paper is organised in sections as : Section II discusses the latest technology of CNTFET. Section III elaborates the low power technique used in the proposed circuit. Section IV covers the various D Flip Flop designs. Section V examines the simulation results and performance analysis. Section VI consummates the paper with the conclusion.

II. CNTFET

Sumio Iijima of NEC in TAIWAN was the first person who observed carbon nanotubes in 1991 while he was studying electrically discharged soot. Graphene sheet when rolled into a tubular shape forms a Carbon Nanotube [4]. CNTs have a diameter of a few nanometers only. The diameter of single walled CNT ranges from 0.7nm to 0.3nm[5]. It has numerous electrical, mechanical and thermal properties that are noticeable and can be used in various fields of science. As a matter of fact CNTs have entered into transistor technology [6]. Carbon Nanotubes are characterized by the way in which the grapheme sheet is rolled and can be denoted by chiral vectors (n,m). CNTs with there chiral vectors as m-n=3i (i.e. Z) are metals otherwise they are semiconductors [7]. The diameter of the CNT is directly related to the carbon-carbon distance (a_0) and the chiral vectors (n,m).

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm}$$

In CNTFET a carbon nanotube is placed in between two electrodes that is in between drain and source of the transistor, Fig. 2. This model is based on Stanford CNTFET model [8]. It is very much similar to a MOSFET as it has 3 terminals – Source, Drain, Gate. Here the channel carrier conduction is offered by carbon nanotubes. Usually an array of carbon nanotubes are used. The tubes used here are single walled carbon nanotubes (SWCNT) which are formed by rolling a single sheet of graphene. CNTFETs deliver a very high

performance transistor action. Various conduction parameters depends on the number of tubes used.

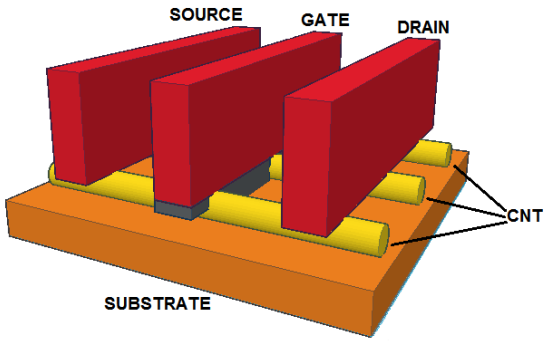

Fig 2

The threshold voltage of CNTFET is inversely proportional to the carbon nanotube diameter and is given by,

$$V_{th} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{cnt}}$$

III. LOW POWER TECHNIQUE : SLEEP TRANSISTOR

Scaling at a large extent usually causes rise in leakage currents. Leakage currents are not favourable for transistor action and performance. It becomes a source of unnecessary power dissipation. As the number of transistors is increasing yearly (Moore's Law) [9], leakage is also increasing. Leakage current prevents the transistor in going to complete off state. In the active state the CMOS circuit power dissipation is due to dynamic and static components but in the standby mode it is due to this leakage current.

In sleep transistor technique we use NMOS and PMOS transistors in the pull up and pull down paths of a CMOS logic design. These pull up/down transistors are gated with a sleep signal which controls the data retention of the logic design. When the circuit is in active mode the sleep signal is kept at high voltage-Logic 1 and when the circuit is in standby mode sleep signal is kept at low voltage-Logic 0. The pull down sleep transistor acts as a virtual ground point and the pull up sleep transistor acts as a virtual power point. Two versions of sleep transistor technology are discussed in this paper.

Fig. 3.1 is the Pull Down Sleep Transistor version. It has a transistor T1 positioned at the pull down path. When the circuit is in standby mode SLP=0 and T1 goes into cut off stage and thus preventing excess leakage current flow. As it has only one sleep transistor it requires less area but it has higher total average power dissipation.

Fig. 3.2 is the Pull Up and Pull Down Sleep Transistor version. It has two transistors T1 and T2 positioned at the pull down and pull up path. When the circuit is in active mode SLP = 1 and $\overline{SLP}$ = 0 hence both T1 and T2 are active. Now when the circuit goes in standby mode with SLP=0 and $\overline{SLP}$ = 1 these T1 and T2 go into cut off stage and thus preventing excess leakage current flow.

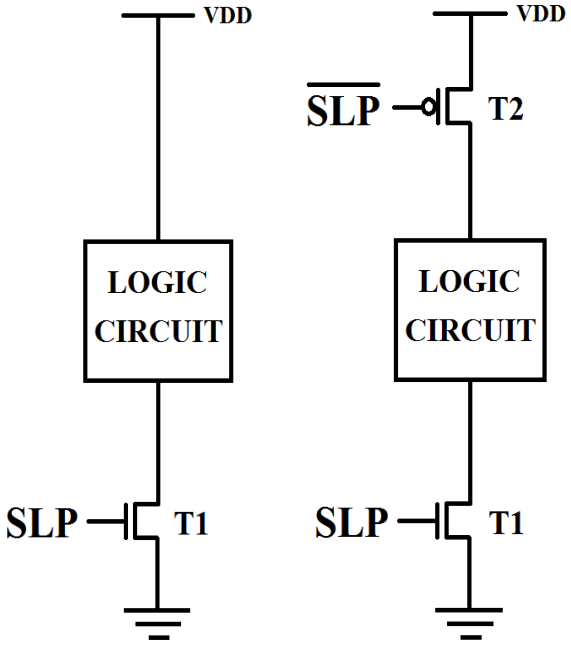

Fig. 3.1 Fig. 3.2

IV. D FLIP FLOP DESIGNS

A. *TGDFF (TRANSMISSION GATE D FLIP FLOP)*

The conventional D flip flop design has 16 transistors. Fig 4.1 depicts the transmission gates and inverters are connected in series. This configuration produces a very strong regenerative feedback. The clock signal is fed to 8 transistors. This flip flop is positive edge triggered and changes its output only at the clock signal's rising edge. The first analysis in this paper is performed on this circuit and average power is calculated.

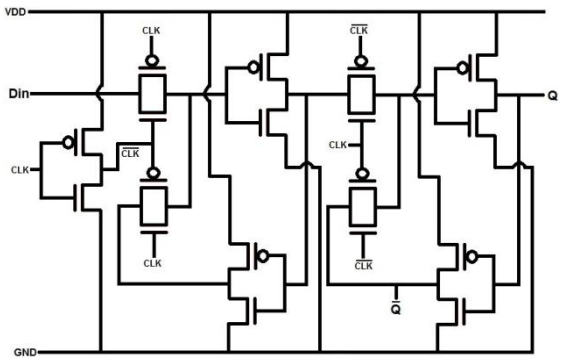

Fig 4.1

B. *TGDFF USING CNTFET*

Second analysis is performed on TGDFF's CNTFET version. Here the previous circuit's (Fig. 4.1) design is implemented over Stanford's CNTFET spice model. As CNTFETs have very low power dissipation, there is a noticeable difference between the average power of CNTFET and the conventional circuit. The feedback of this design is similar to the previous discussed model. The carbon nanotube based transmission gates behave in a very interesting manner. Further discussion can be seen in Section V.

C. *CN-ST-TGDFF (CNTFET BASED TGDFF WITH SLEEP TRANSISTORS – PULL UP AND PULL DOWN)*

Now in sleep transistor technique one CNTFET is attached at the pull up path and one at the pull down path, see Fig 4.2. This addition of two transistors controls the leakage current in the standby mode as discussed earlier but state retention property is not impeccable. Average power is then calculated using HSPICE and CNTFET's Stanford model.

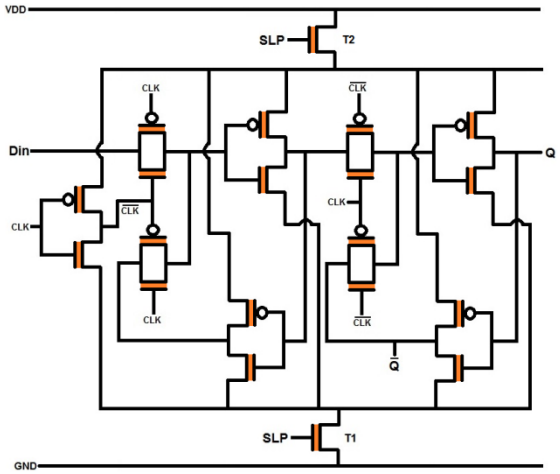

Fig 4.2

V. SIMULATION RESULTS AND PERFORMANCES

All the related performances and results are tabulated in this section.

TABLE 5.1

DESIGN	POWER CONSUMPTION (nW)		
	TEMPERATURE		
	25˚	*30˚*	*35˚*
CMOS DFF	641.9	655.3	662.9
CNTFET DFF	20.4	21.5	25.3
CNTFET DFF WITH SLEEPER	9.7	15.4	20.3

TABLE 5.2

TEMP ˚C	PERCENTAGE POWER REDUCTIONS		
	CMOS TO CNTFET DFF	CNTFET TO CNTFET SLEEPER DFF	CMOS TO CNTFET SLEEPER DFF
25	96.8	52.4	98.4
30	96.7	28.3	97.6
35	96.1	19.7	96.9

This 16T D Flip Flop based on CNTFET is designed in 32nm technology model (STANFORD MODEL) [10]. All the simulations related to this is done on HSPICE. Fig. 5.1 shows the power consumption of CMOS DFF, CNTFET DFF and CNTFET DFF with Sleeper Transistors. As we can observe from the power consumptions of all the three circuits discussed here, it is clear that CNTFET based models consumes way less power when compared to the conventional CMOS logic designed circuit. The new nano tube based circuits consume approximately 30 times less power than the former circuit.

CMOS designed circuit consumes 641.9 nW of power at 25˚C, the CNTFET based circuit consumes 20.4 nW of power. This shows that the same circuit consumes less power in case we use carbon nanotubes as the channel medium. Now by just adding the sleeper transistor at the pull up and pull down position we can see that the power consumption further decreases to 9.7nW.

Similarly is the case of percentage power reductions. At 25˚C, we get large values of percentage power reductions in all the three comparisons. But as we increase the temperature to 30˚C we see slight decrease in the percentage power reductions. At 35˚C the reductions further decrease down.

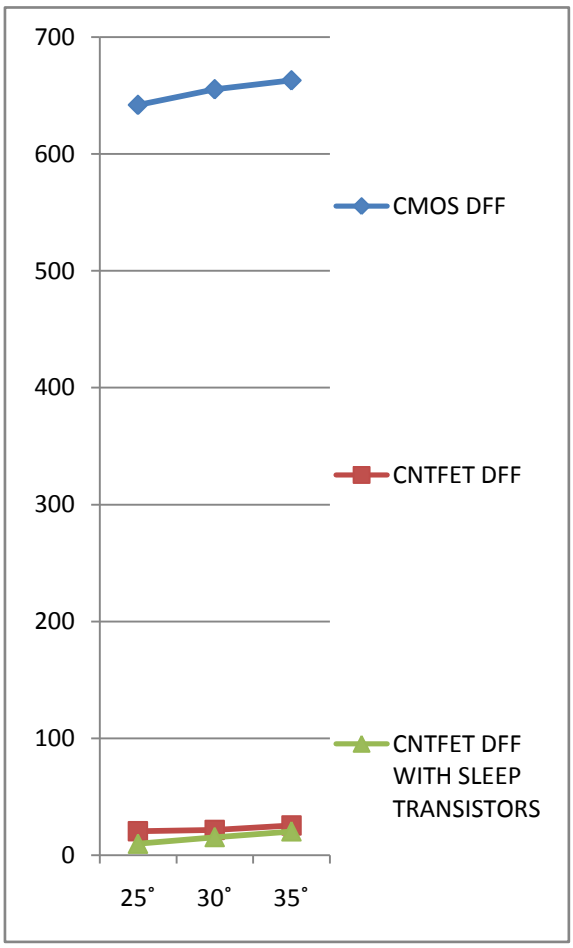

FIG 5.1

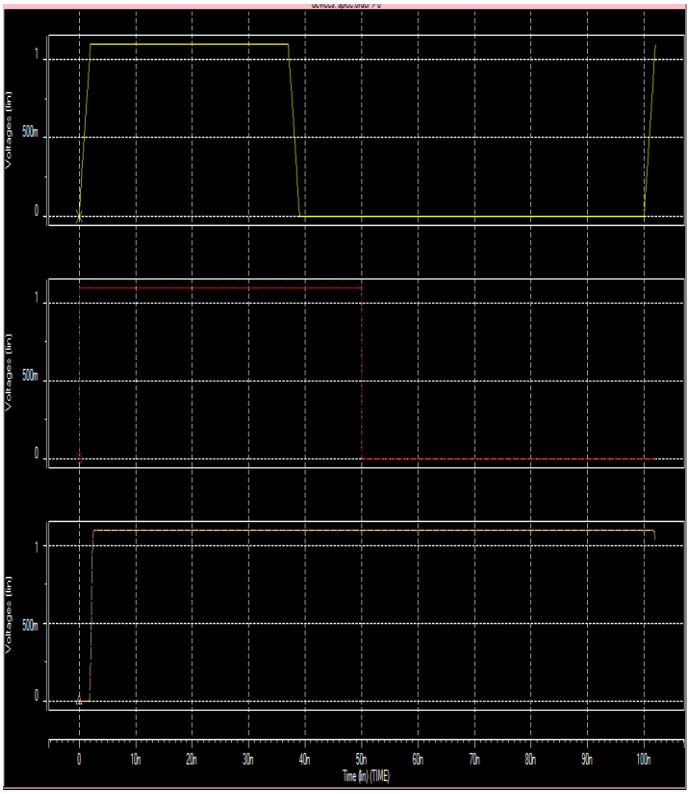

Fig 5.2 (CMOS DFF)

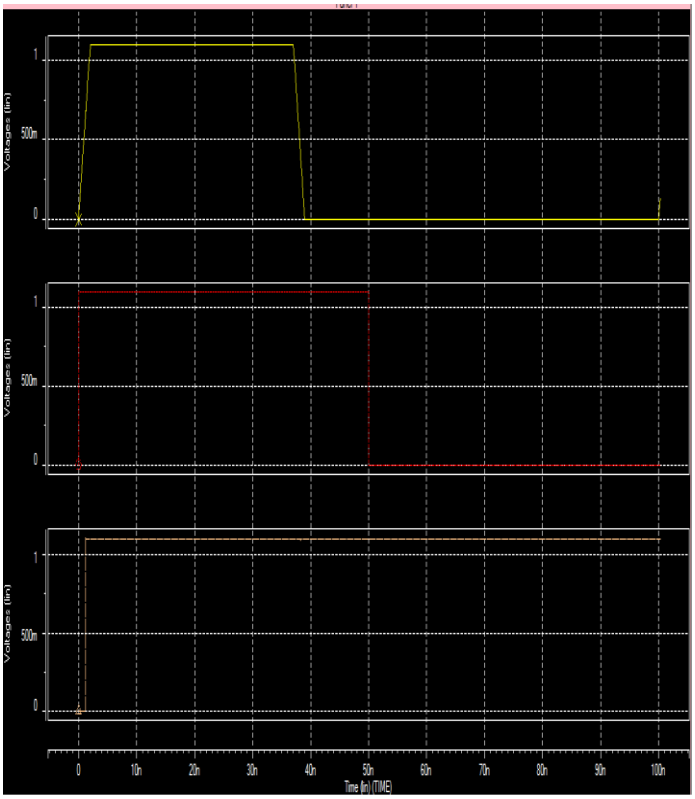

Fig 5.3 (CNTFET DFF)

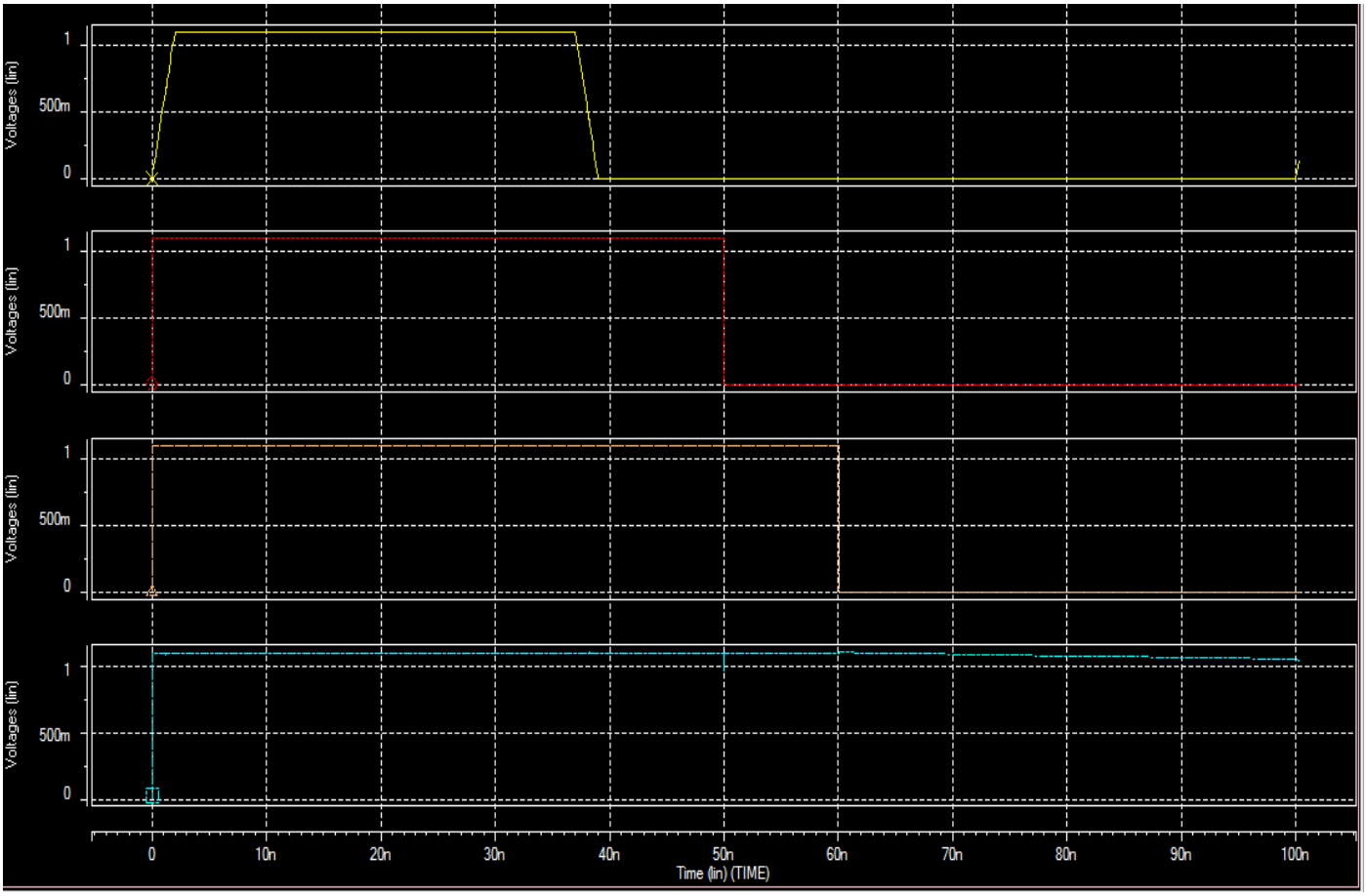

Fig 5.4 (CNTFET SLEEPER DFF)

Fig. 5.2 depicts the basic DFF (CMOS) edge triggered action. Due to this performance ability, DFFs are widely used in modern day circuits. On every rising edge of the clock the flip flop changes its state. This switching takes place frequently enough to consume a large amount of power (~650nW) which can be inferred from the above results. This power is the dynamic power.

Fig. 5.3 shows the performance ability of CNTFET based DFF. This is very much similar to the previous case of CMOS DFF. Here the switching action is the same but in the contrary this design has very less power consumption (~21nW).

Fig. 5.4 shows the performance ability of CNTFET based DFF model having sleep transistors. This model also has the same switching action as the previous models have but with very less power consumption (~15nW).

VI. CONCLUSIONS

This paper clearly elaborates the usage of carbon nano tubes as channel medium and the concept of sleeper transistors. Flip Flops consume large amount of dynamic power because of the switching action. This dissipation can be reduced by making the channel dimensions smaller and by the use carbon nano tubes. At small channel geometries the dynamic power nearly equals the static power. From the above analysis it is perspicuous that there is a huge power reduction from CMOS DFF to CNTFET SLEEPER DFF i.e. ~97%.

This type of flip flops can be used in the devices of near future as they would deliver exact performance like the conventional circuits and they would also consume less power. Hence low power handheld devices can feature this type of circuit methodology.

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