Design of Low Power, Area-Efficient Carry Select Adder

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Abstract

Design of low power and area-efficient logic systems forms an integral part and largest areas of research in the field of VLSI Design. Addition is the most fundamental arithmetic operation. In this paper, a low power, area-efficient carry select adder is proposed. CSA is one of the fastest adders used in data-processing systems to perform fast arithmetic operation. Secondly, structure of carry select adder is such that there is scope of reducing the area and power consumption. Thirdly, there is scope to reduce the area by using some add-one scheme. So, a Modified Carry Select Adder(MCSA) is designed by using single Ripple Carry Adder(RCA) and Binary to Excess-1 Converter (BEC) instead of dual RCAs in order to reduce the area and power consumption with small speed penalty. CSA and MCSA structures are designed for 8-bit, 16-bit, 32-bit and 64-bit. Result analysis shows that MCSA is better than CSA.

1. Introduction

Addition forms a very integral part of computer arithmetic. It is extensively used among a set of real time digital signal processing benchmarks from application specific CSP to general purpose processors [1]. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. Some of the complex adders are Ripple Carry Adder (RCA), Carry Look- Ahead Adder (CLA), Carry Select Adder (CSA) etc.

Ripple Carry Adder is composed of many cascaded single-bit full adders. The circuit is simple and area-efficient but computation speed is slow [2]. Carry Look-Ahead Adder derives faster results but there is increase in area. In carry select adder, N bit adder is divided into M parts. Each part of adder is composed of two ripple carry adders with C_{in}=0 and C_{in}=1 respectively. According to the logic state of input carry, we can select the output result by using a multiplexer. Thus, CSA can compute faster because current adder stage does not need to wait for the previous stage's carry-out signal. In CSA, carry propagation delay can be reduced as compared with RCA. Therefore, Carry select adder is used because it is faster than other adders and also there is further scope to reduce the area and power consumption.

In this paper, Modified Carry select Adder is proposed using single RCA and BEC instead of dual RCA in order to reduce the area and power consumption.

This paper is organised as follows: In section 2, Delay and Area calculation for basic adder block is shown. Section 3 explains Conventional CSA and in section 4 Binary to Excess-1 converter (BEC) is described. Section 5 explains the Modified Carry Select Adder. Results are evaluated in section 6 and section 7 concludes.

2. Delay and Area Calculation for Basic Adder Blocks

AND, OR and INVERTER (AOI) implementation of XOR gate is shown in Figure 1. The operations of gates between the dotted lines are performing operations in parallel. Delays contributed by the gates are indicated by the numeric representation. The area and delay methodology considers that all gates are made of AND, OR and INVERTER, each having area equals to 1 unit and delay equals to 1 unit.

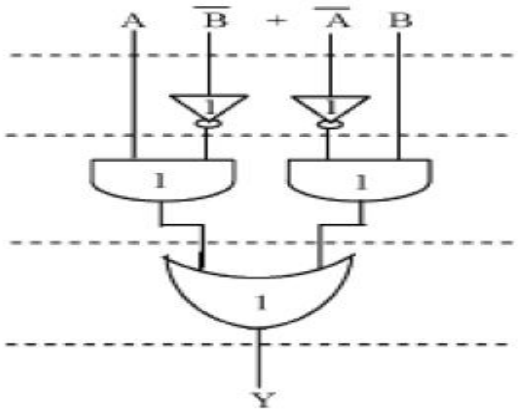

Figure 1. Delay and area evaluation of XOR gate

Number of gates in the longest path of a logic block that contributes to the maximum delay is then added up. The area evaluation is done by counting the total number of AOI gates required for each logic block. Using this approach CSA blocks of 2:1 MUX, Half adder (HA) and Full Adder (FA) are evaluated and listed in Table 1.

Table 1. Delay and area count of the basic blocks of CSA

Adder Blocks	Delay	Area
XOR	3	5
2:1 MUX	3	4
Half Adder	3	6
Full Adder	6	13

3. Conventional Carry Select Adder

The CSA is one of the fastest adders used in many data-processing processors for performing arithmetic operations. It is also used in computational systems to alleviate the problem of carry propagation delay by generating multiple carries and then selecting a carry to generate the sum [3].

CSA consists of number of blocks in which RCA chains run in parallel. The principle on which CSA works is: Two additions are performed in parallel; blocks evaluated conditionally with carry values 0 and 1. For the addition purpose RCAs are used. Therefore, CSA uses dual RCAs structures. When the carry-in values are assigned to the blocks, then the final value is used to select the sum bits from one of the two blocks. At this point of time, carry-out values can be evaluated, which in turns selects the sum bits and carry out of the next block.

In RCA, every full adder has to wait for the incoming carry before the outgoing carry is generated. But CSA found a way to get around this linear dependency by anticipating both the possible values of carry i.e. 0 and 1 and evaluates the result in advance. Once the real value of carry is known, result can be easily selected using the multiplexer stage. Figure 2 shows the 64-bit conventional CSA which consists of two RCAs in each block, one for C_{in}=0 and other for C_{in}=1. But the conventional CSA is still area consuming due to the dual RCA structure.

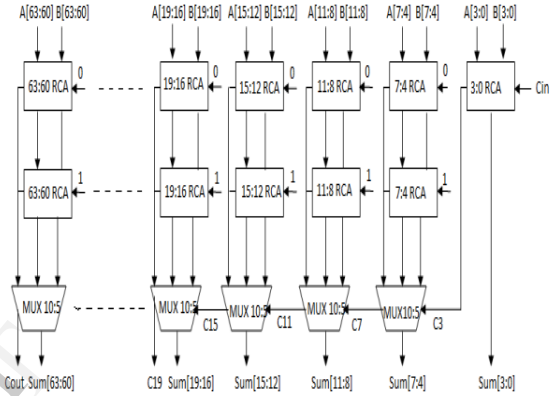

Figure 3. 64-bit Conventional carry select adder

4. Binary to Excess-1 Converter

In order to reduce the area and power consumption of conventional CSA, binary to Excess-1 Converter (BEC) is used in place of RCA with C_{in}=1. To replace the N-bit RCA, N+1 bit BEC is used. The main advantage of BEC comes from the fact it uses lesser number of logic gates than the N-bit full adder structure. The structure and function table of 4-bit BEC is shown in Figure 3 and Table 2 respectively.

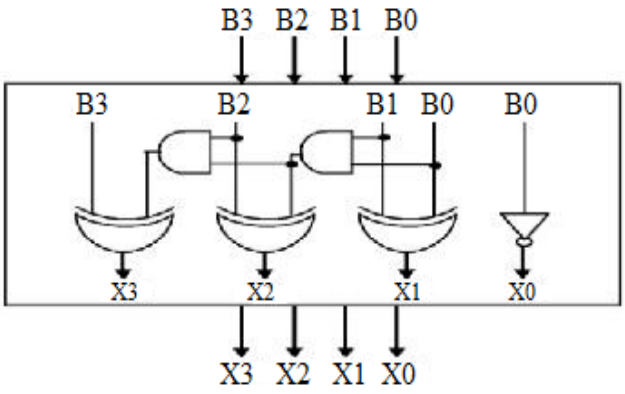

Figure 3. 4-bit Binary to excess-1 converter

BEC [4] is a circuit used to add 1 to the input numbers. Addition can be performed using BEC together with a multiplexer as shown in Figure 4, one input of 8:4 MUX gets as its input (B3, B2, B1 and B0) and another input of MUX is BEC output. Therefore, BEC can be used in order to reduce the area and power consumption of conventional CSA. When MCSA is designed for a large number of bits using BEC logic then there is large silicon area reduction [5].

Table 2. Truth table of 4-bit binary to excess-1 converter

Binary Logic $B_0\ B_1\ B_2\ B_3$	Excess-1 Logic $X_0\ X_1\ X_2\ X_3$
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

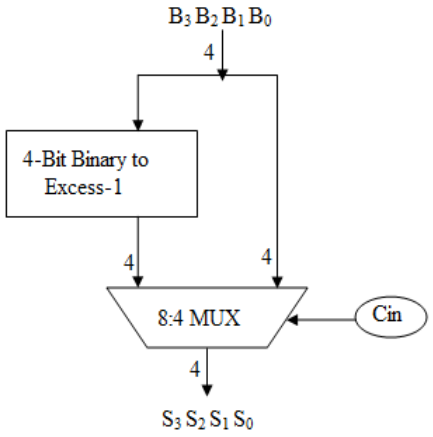

Figure 4. 4-bit Binary to Excess-1 logic with 8:4 multiplexer

5. Modified Carry Select Adder

The proposed structure of Modified carry select adder uses single RCA and BEC instead of dual RCA in order to reduce the area and power consumption with small aped penalty. The reason for the area reduction is that BEC uses less number of logic gates than the RCA. Therefore, there is large silicon area reduction for which MCSA is designed for large number of bits. The MCSA architecture for 64-bit is shown in Figure 5.

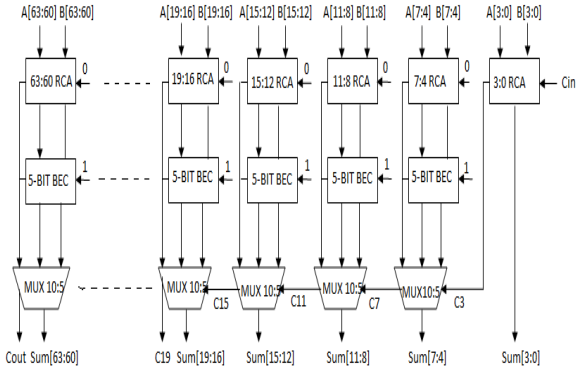

Figure 5. 64-bit Modified carry select adder

To replace N-bit RCA, N+1 bit BEC is used. Thus, MCSA is designed using 4-bit RCA for each block and thus BEC used is of 5-bit. In this way, the area and power consumption of MCSA is reduced. Thus, dual RCAs in conventional CSA are replaced by single RCA with C_{in}=0 and BEC with C_{in}=1. MCSA architectures are designed for 8-bit, 16-bit, 32-bit and 64-bit. The results are then compared for area, delay and power with the results of conventional CSA.

6. Results

The design has been synthesized at 90nm process technology using Xilinx Spartan-3 device. The performance of proposed MCSA is analyzed and compared with conventional CSA. Power consumption is measured in terms of the total power and dynamic power. Number of gates indicates the area of design and speed of adder is estimated by calculating the delay involved in design. Table 3 shows the comparison of area, delay and power consumption of CSA and MCSA for 8-bit, 16-bit, 32-bit and 64-bit. The result shows that the area and power consumption of MCSA is reduced with small speed penalty. Thus, MCSA is better than conventional Carry select adder in terms of area and power consumption. The graphical representation of area and power consumption for CSA

and MCSA are shown in Figure 6 and Figure 7 respectively.

Table 3. Comparison of frequency, area, power and delay of CSA and MCSA

	Adder	Maximum Attainable Frequency (MHz)	Area/ Gates (AOI)	Power (mW)	Delay (ns)
8-bit	CSA	69.14	200	94.48	14.46
	MCSA	60.12	167	86.92	16.63
16-bit	CSA	50.47	480	94.63	19.81
	MCSA	46.30	381	81.38	21.59
32-bit	CSA	32.76	1040	95.01	30.51
	MCSA	30.52	809	81.79	32.65
64-bit	CSA	19.25	2160	95.49	51.92
	MCSA	18.51	1665	79.25	54.01

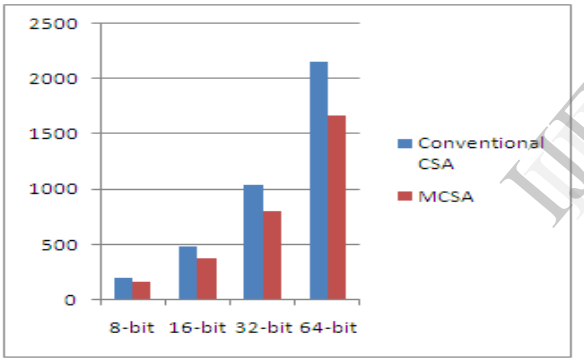

Figure 6. Comparison of adders for area/gates

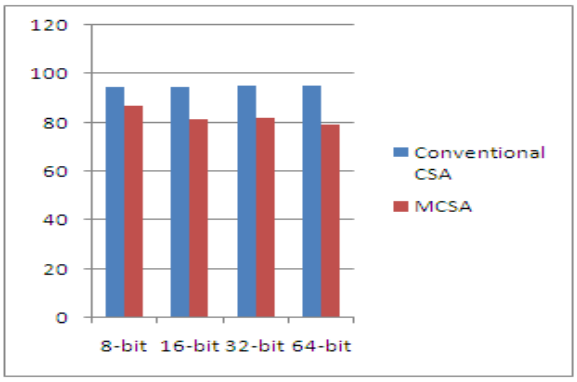

Figure 7. Comparison of adders for power consumption

The area utilization summary of 8-bit, 16-bit, 32-bit and 64-bit CSA and MCSA are shown in Table 4. The report shows that MCSA has less area than conventional CSA. The graphical representation of area utilization is shown in Figure 8. Number of slices and 4 I/P LUTs are less in MCSA than in conventional CSA. The comparison results shows that MCSA is better than CSA in terms of area and power but with small speed penalty.

Table 4. Area utilization summary of adders

	Adder	No. of slices	No. of 4 I/P LUTs	No. of bonded IOBs	No. of GCLKs
8-bit	CSA	12	21	28	1
	MCSA	10	18	28	1
16-bit	CSA	27	47	52	1
	MCSA	21	39	52	1
32-bit	CSA	57	99	100	1
	MCSA	44	81	100	1
64-bit	CSA	117	203	196	1
	MCSA	88	163	196	1

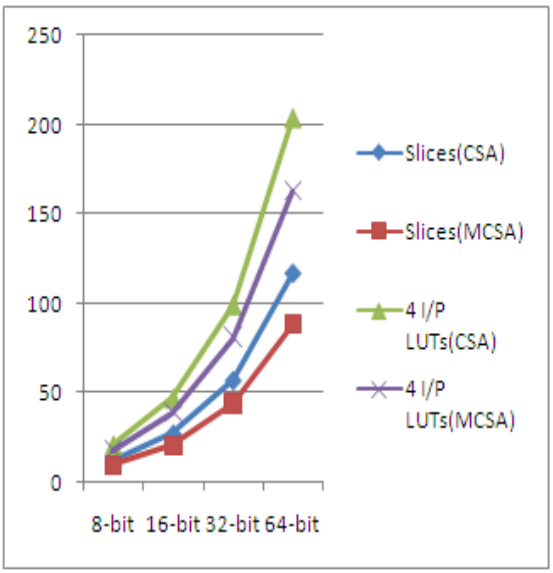

Figure 8. Area utilization summary of adder

7. Conclusion

An efficient modified carry select adder for 8-bit, 16-bit, 32-bit and 64-bit has been proposed using single RCA with C_{in}=0 and BEC with C_{in}=1 with less area and power consumption. The delay of MCSA is slightly increased but a design with less area and power consumption is obtained. The frequency of conventional CSA is better than MCSA. This paper proposes a scheme that reduces the area and power consumption of conventional CSA. Hence, the proposed MCSA is better than conventional CSA and is used in various applications like data paths in microprocessors, in processing units such as Arithmetic Logic Units, in digital signal processing and in various other applications.

8. References

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