Design Of Low Power And Reduced Area Carry-Select Adder

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Abstract

This paper presents a low power and reduced area carry select adder. By using new technique called combine-1 we have generated 4 bit carry select adder (CSA) and compared it with conventional carry select adder. This work use simple and efficient gate level modification of conventional carry select adder, resultingin reduction in transistor count and power by voltagescaling. This work has been implemented in tannertools, version 13 using 0.13µm technology. Here area has been shown in terms of transistor count.

1. Introduction

Area and Power consumption are relevant figures of merit to be considered especially when the design targets VLSI realization.In VLSI design we always give stress on three aspects area, power and speed. As a designer, while dealing with these constraints, we have to tradeoff as per the requirements amongthese aspects[4]. This can shown by following equation

$$P_{avg} = C_{load.}V_{dd}^{2}.f$$

Above equation tells us two facts, first tells that when we reduce the power consumption, speed of operation decreases so we need to tradeoff between power and speed. Second- power reduces squarely with supply voltage scaling.Another way to limit the power dissipation of a circuit is to reduce the amount of switched capacitance at the output. Area can be made directly proportional to transistors count in the circuit, as we decrease the count area automatically decreases significantly. In this work comparison is made between conventional and proposed models of CSA with respect to area in terms of transistors count.

2. Adder

The binary addition has been a subject of extensive study for many years. Adders are the essential component in general purpose micro-processors, digital signal processors and so forth. It also finds application in many other functions such as subtraction, multiplication and division, so it is very important to choose the adder design that would give the desired performance. The choice of adder architecture to use is of utmost importance, since the performance of adders may determine the whole system performance. Adders are the basic building blocks of Arithmetic and Logic unit and decide the performance of CPU[1].Every aspect of the adder design is directly related to area optimization. If we eliminate the transistors corresponding to redundant points we can easily save the area.

3. Carry Select Adder

The CSA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carry and then select a carry to generate the sum[2]. The basic block diagram is shown in fig1,which is the basic building block of a carry-select adder, where the block size is 4 [3]. Two 4-bit ripple carry adders are multiplexed together, where the resulting carry and sum bits are selected by the carry-in.Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, selecting which adder had the correct assumption via the actual carry-in yields the desired result.

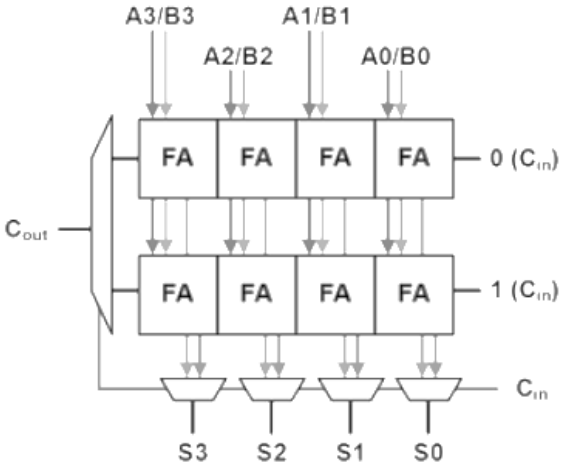
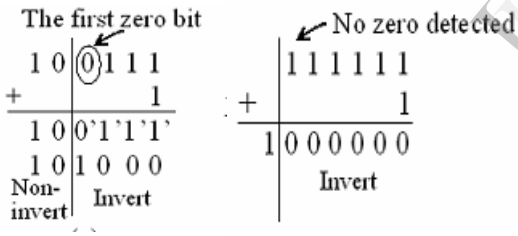


Figure 1: Block diagram of CSA

4. Proposed CSA

The proposed innovation for doing addition is that instead of using two separate adders in CSA, one for the case CS1=1 and the other for the case CS1=0 (CS1is the carry propagated from the first partition to the second one), one adder will be used to reduce the area and power dissipation. Here zero detection logic is used



In zero detection logic once the first zero is detected logic is remain unchanged otherwise it is complemented.The combine-1 circuit proposed mitigates the resource overhead of CSA by replacing one copy of RCA by

$$S_1 = S_0+1$$

Let kdenote the position that the first bit of "0" is detected in $S_0(i)$, starting from the least significant bit (LSB). Then, from

$$\prod_{i=0}^{k} S_0(i) = 0 \qquad k \in [0, n-1]$$

We have,

$$S_1(t) = S_0'(t) \qquad t \in [0, k]$$

$$S_1(t) = S_0(t) \qquad t \in [k+1, n-1]$$

single quotation mark on the superscript implies Boolean complement. From the above derivation, the combine-1 circuit is in essence, based on a "first" zero detection logic. It generates s_1 by inverting each bit in s_0 starting from the LSB until the first zero is encountered. In other way we can say that if sum output from CSA is 1 carry out will be one otherwise zero. As all sums equal one, the zero detection logic generates one at final. As in conventional CSA we use two RCAs block but in proposedcombine-1 design style one RCA block has used zero detection logic with selective complement circuit and multiplexer circuit with minimized transistor count is used as shown in fig2,

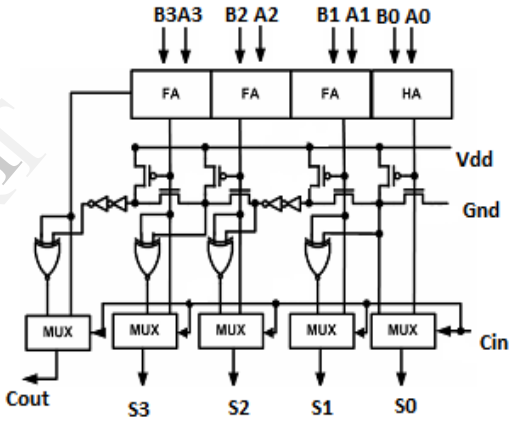


Figure 2: Schematic diagram of CSA

Multiplexer circuit has been implemented using 2T mux cell[1]the implementation of MUX to select correct carry output based on carry-in available as carry out from the previous block. It is implemented in pass transistor logic. pass transistor passes good '0', but a bad '1'.

5. Simulation Result

The circuit design in this paper has been developed using Tanner version 13 in 0.13µm technology. In tables 1 and 2, the spice simulation results of both theconventional and proposed 4 bit CSA structures in terms ofpower and area are produced. The total power dissipated is the sum of dynamic power, internal power, net power and leakage power. This shows that the design can be very well incorporated

into complex VLSI Designs and DSP applications in order to have low power and minimized area of the circuits. Decrease in the number of transistors significantly reduces the power consumption.

Table1.Comparison of power dissipation in conventional and proposed designs at different voltages.

Voltage	Power (conventional)	Power(Proposed design)
3v	15.5mw	11mw
2v	4.3mw	2.5mw
1.5v	1.4mw	0.9mw

Table2.Comparison of transistor count in conventional and proposed designs.

Design	Area (in terms transistors count)
Conventional	390
Proposed	280

6. Conclusion

The proposed structure proves to be a easier solution for less power consumption of carry select adder as we scale down the voltage. The conventional CSA suffers from the disadvantage of decreasing the speed of operation as voltages are reducing. The proposed unit is also found to have less transistors count which also imparting in lowering down the power consumption [5].

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