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Design of Low Power ADC Using 0.18µm CMOS Technology

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Abstract

The dual slope integrating analog to digital converter (ADC) is an efficient one for wireless transmission of ECG signals. Normally the dual slope ADCs are used for high resolution applications and the accuracy is very high. The main advantage of the ADC design is its high speed with low power. The dual slope ADC consists of integrator, comparator and a ten bit binary counter. To design integrator by using low power op-amp; comparator by using CMOS transistor and a binary counter by using JK flip-flop which are consume less power. These components have to be incorporated in a system with a single control switch that produces the control signals and dual ramp at the input side. Finally the digital output is occur at the terminal of binary counter. This work was done using CADENCE Virtuoso environment with 180nm technology.

Keywords: ECG, ADC, CMOS, binary counter

1. INTRODUCTION

Analog to digital converters are the interface between the analog input signal and digital signal processing block. Most of the real world signals are analog in nature, they are continuous-time, and continuous-valued signals etc., Compared to analog signals, digital signals have the following advantages:

a) It is immune to electrical noise
b) It can be manipulated easily
c) It is easy to store
d) It is easy to copy and transfer

The type of ADC used is an indirect method of A/D conversion, where the analog voltage is converted to a time period measured by a counter. An electronic switch selects the circuit's input as an unknown analog voltage or a reference voltage. At the initial condition, the counter is reset and then switch selects the unknown analog voltage to the integrator. The counter is enabled when the output of the comparator is zero (V_o =0), it counts for a fixed time interval until it flows. For a constant analog input, the slope of integrator's ramp output is proportional to the unknown input; hence the output voltage of the integrator at the end of the fixed time interval (T) is proportional to the analog output [1]. If the analog input (V_i) varies during the fixed time interval, the integrator's output at the end of this time interval is proportional to the average value of the input

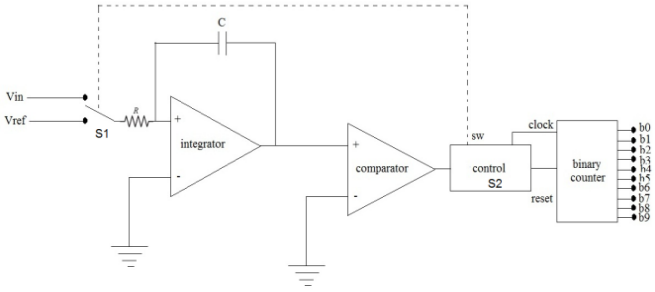

Fig. 1. Block diagram of Dual Slope ADC.

$$V_o(T) = -\frac{1}{RC}\int_0^T V_i\,dt \qquad (1)$$

where R is resistance in Ω and C is capacitance in F. At the end of clock period T, the input of the integrator is switched from the analog input to the reference voltage, making the integrator ramp output with a fixed positive slope [2]. The counter counts the integrator's output to reach the comparator's threshold where the counter is stopped at required time period. Normally during the conversion period the input voltage varies between 0 to $v_{in.}$

2. DUAL SLOPE ADC

The block-diagram of the dual-slope integrating A/D converter is shown in Fig. 1. This converter is based on the same principle as the single-slope converter. It converts the analog input to time, and the measure the time by counting fixed-frequency pulses [3], [4]. The improvement over the single-slope converter comes from using the same integrator to integrate first the input voltage V_i and then the reference V_{ref}. As a result, the conversion function of the dual-slope converter does not depend on exact values of the time-constant RC or the clock period T, the integrator is built using RC around an op-amp. Switches S1, S2 are used to bring either the input V_i or the reference $-V_{ref}$ to the input of the integrator. Zero crossing of the integrator output V_{int} is detected using the voltage comparator. An (n+1)bit binary counter with reset R and

clock CLK inputs is used to count the number of fixed-frequency pulses CLK generated by an external clock during the conversion period. The most significant $(n+1)^{th}$ bit of the counter is used as the signal Q to control the switches S1 and S2. All inputs to the counter and the latch are assumed to be rising-edge triggered. At the beginning of a conversion period, the (n+1) bit binary counter and the integrator are reset by the signal R. When R goes low, the switch S1 is turned off and the fixed-frequency clock pulses CLK are passed to the clock input of the binary counter. The switch S1 is on and the switch S2 is off, so that the integrator output, assuming constant V_i is

$$V_{\text{int}}(t) = -\frac{v_i}{RC}t \tag{2}$$

At the end of the first interval t1, the counter counts up through 2n pulses, and goes from 011…….1 to 100……0. The $(n + 1)^{th}$ bit Q goes high, the switch S1 is turned off and the switch S2 is turned on. Therefore the length of the interval t1 is given as

$$t_1 = 2^n t \tag{3}$$

so that the integrator output at the end of this interval is

$$V_{\text{int}}(t1) = -\frac{v_i}{RC}2^n T \tag{4}$$

in the second interval $-V_{ref}$ is integrated using the same integrator, so that

$$V_{\text{int}}(t) = V_1 + \frac{v_{ref}}{RC}t - t_1 \tag{5}$$

the conversion ends at the time when the integrator output crosses zero. The length of the second interval t2 is

$$t_2 = -\frac{v_1}{v_{ref}}RC \tag{6}$$

during the second interval, the counter counts up N pulses, the final count N is given by

$$N = 2^n \frac{v_1}{v_{ref}} \tag{7}$$

This is the ideal conversion function [13]. The most important point to note here is that both RC and T cancel out from the final expression for N, so that accuracy of the converter is not affected by the exact values of T, R or C. The choice of R, C and T is still important in practical issues because the clock rate and voltage variation is within the limit of the design, and the voltage variations are also within the component and supply limits. For n-bit conversion, the conversion time goes up to $2^{n+1}T$, where T is the period of the external clock used to measure the times t1 and t2. This limits the achievable sampling rate of the dual-slope A/D converter.

PRINCIPLE OF OPERATION

The basic integrating ADC circuit consists of a switch, an integrator, a timer that determines how long to integrate the unknown and measures the duration of the reference integration, a controller, and a comparator. The switch is installed between the voltage to be measured and the reference voltage (negative value). Depending on the operation, a switch connected in parallel with the integrator capacitor for resetting the integrator in two consecutive rounds (by discharging the integrator capacitor) [12]. The switches are controlled by dedicated controller. The conversion takes place in two phases; one is the run-up phase, and the other is the run-down phase. In the first stage, the voltage which is supplied to the integrator is to be measured. During first part i.e. the run-up phase, the switch selects the measured voltage as the input provided to the integrator. Then the integrator is allowed to ramp for a fixed interval of time for the charging of the capacitor. During the second part i.e. run-down phase, where the input to the integrator is a reference voltage (negative), the switch selects the reference voltage as the input voltage of integrator. The time taken for the integrator's output to return to zero value is measured during this phase.

DESIGN OF INTEGRATOR USING OPAMP

The mathematical operation of integration can be simulated by replacing the feedback resistor in an inverting OP AMP circuit and inserting a capacitor. Figure 2 shows the ideal op-amp integrator

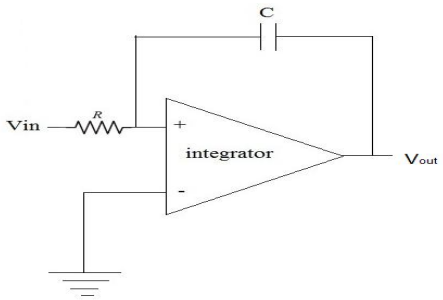

Fig.2. Op-amp Integrator

The Integrator is a circuit using op-amp that performs the mathematical operation of Integration. The integrator acts like a storage element that produces a voltage output which is proportional to the integral of its input voltage with respect to time [14]. In other words the magnitude of the output signal is determined by the length of time a voltage is present at its input as the current through the feedback loop charges or discharges the capacitor as the required negative feedback occurs through the capacitor. If an ideal op amp circuit operation is assumed, no current will flow into the inverting terminal of the amplifier due to the infinite input impedance [5]. Also, the voltage between the inverting and non-inverting terminal is equal due to the effects of the negative feedback. This means that the voltage at the inverting terminal is at ground potential. So, If= - IC and $I_{in} = V_i/R_{in.}$

$$V_o = -\frac{1}{C}\int i_c(t)dt \tag{8}$$

the op-amp for an integrator is designed using the CMOS transistors and the ratio of the CMOS are designed

according to the input and output requirements of the amplifier [1]. It gives the design of a two stage op-amp and the structure of the two stage op-amp is shown in the fig.3.

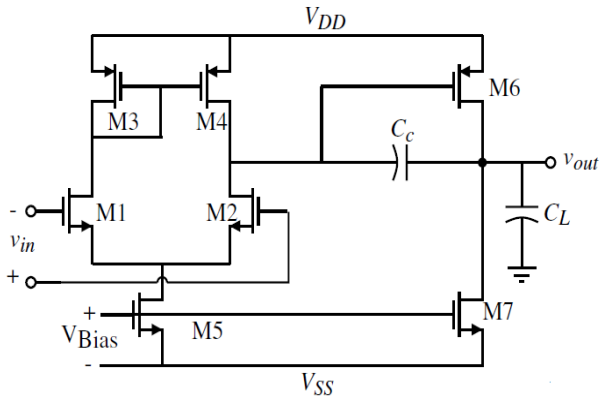

Fig.3. CMOS op-amp

DESIGN OF COMPARATOR

The comparator is a circuit that compares one analog signal with another analog signal or a reference voltage and outputs a binary signal based on the comparison. The comparator is basically a 1-bit analog-to-digital converter [7]. The symbol of comparator is shown in the fig.5.

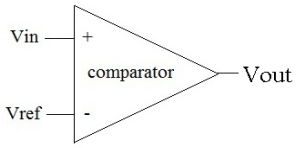

Fig.5. Schematic symbol of Comparator

The comparator is an analog circuit used to compare the sampled input signal and the reference signal. In this paper a low power two stage comparator is used which works in the positive feedback mode. Fig.6 shows the schematic diagram of the 2 stage comparator. The main advantage of using this kind of comparator is no power has been wasted from the supply when the comparator is not working stage [8]. The biasing circuit gives the biasing current to the comparator. The biasing current is given as

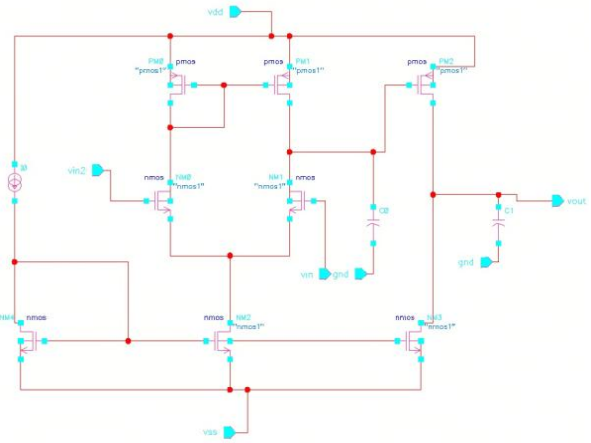

Fig.6. Comparator Schematic

$$I_{ds} = \frac{k}{2}\frac{w}{l}(V_{gs} - V_{th})^2(1 + \lambda V_{ds}) \quad (9)$$

The W/L ratios are calculated according to the biasing currents of the transistor. The differential pair transistors Q3 and Q4 compare the two input signals and the error signal is amplified at the output stage. All the other transistors act as for switching operation [9]. The comparator consumes 13.8µW when the supply voltage is 1.8V.

3. RESULTS AND DISCUSSION

OUTPUT OF AN OP-AMP

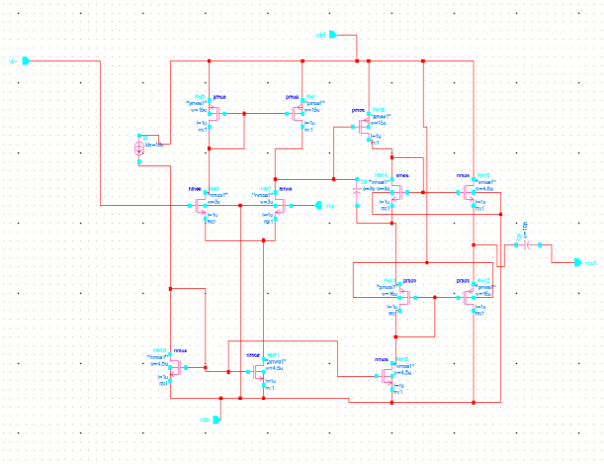

Fig.8. Schematic Diagram of Op-amp

In this work, 10 bit binary counter is used to convert analog signal to digital signal, where it consists of JK flip flops, which has been driven by the synchronous clock pulse.

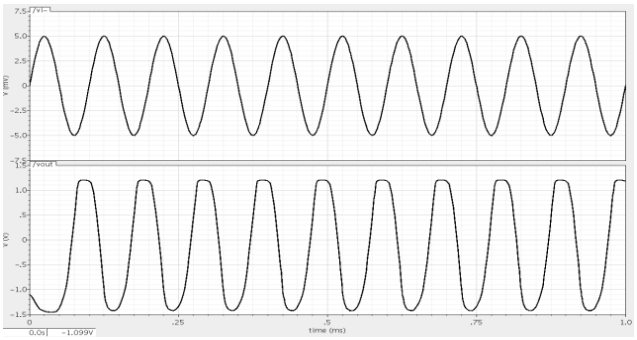

Fig.9. Output of Op-amp

The schematic diagram of the designed op-amp and its output response shown in the fig.8 & 9 which is in the inverted amplified form. The designed op-amp is producing the output power of 0.25mW.

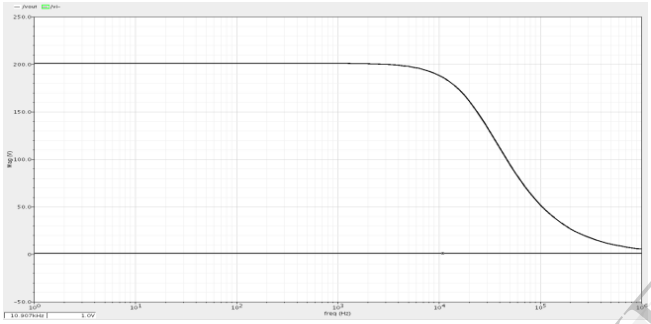

Fig.10. AC Response of Op-amp

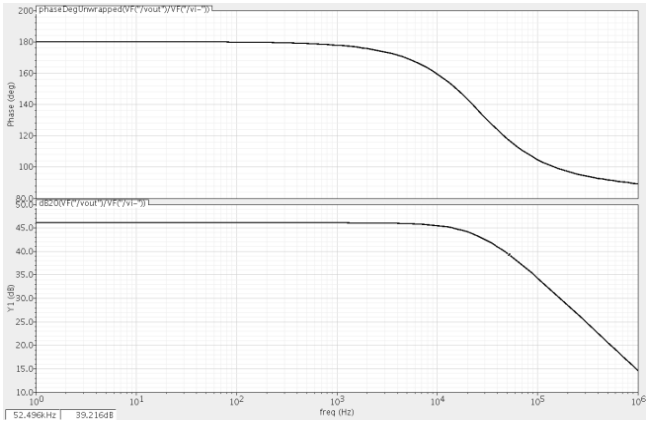

Fig.11. Gain of Op-amp

The figure 10 and 11 shows the output AC response and the output gain of the designed op-amp. The gain value of the op-amp is 47db and the phase value is 180 degrees.

OUTPUT OF OP-AMP INTEGRATOR

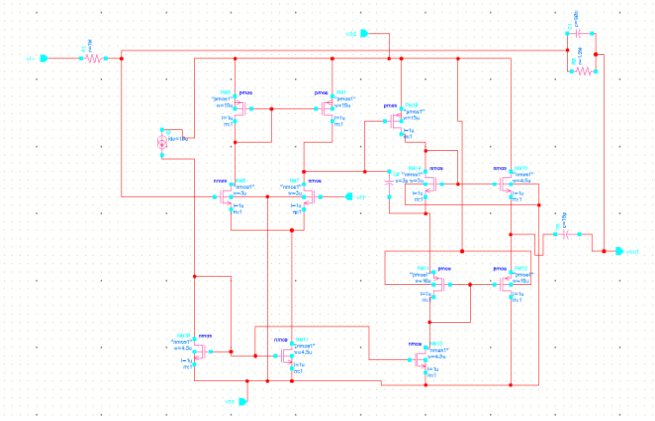

Fig.12. Schematic Diagram of Op-amp Integrator

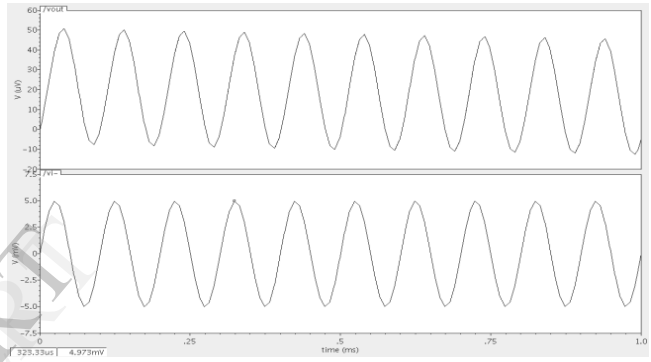

Fig.13. Output of Op-amp Integrator with sine wave

The schematic diagram of the designed integrator using cadence tool is shown in the figure 12. The value of the feedback capacitor is 90nf and finally the obtained waveform is shown in the figure 13. The integrator will produces the cosine waveform when the input is sine wave and it produces triangular wave when the input is square pulses as shown in fig.14.

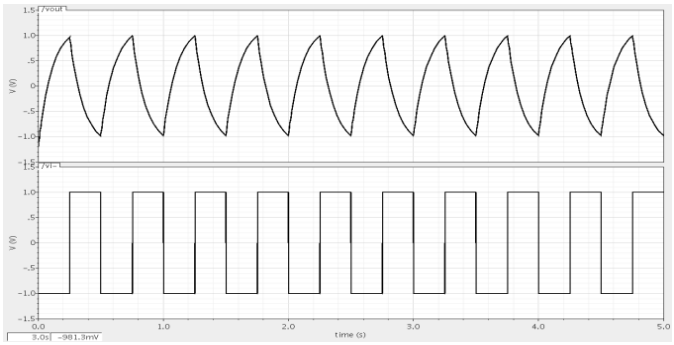

Fig.14. Output of Op-amp Integrator with pulses

OUTPUT OF COMPARATOR

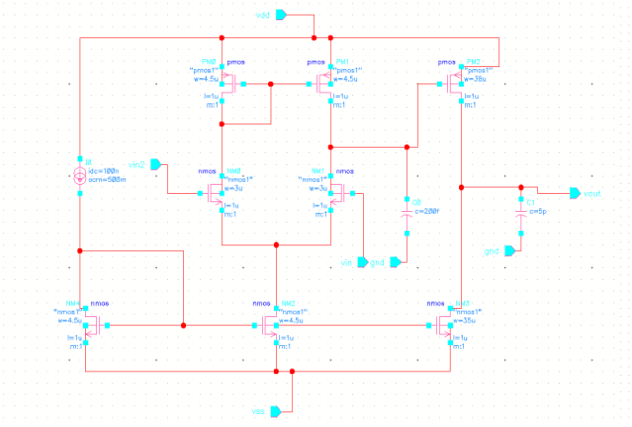

Fig.15. Schematic Diagram of comparator

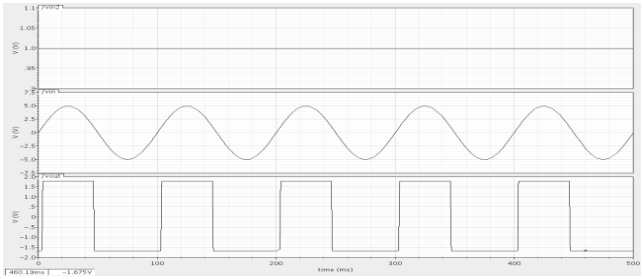

Fig.16. Output response of comparator

The schematic diagram of the designed two stage comparator is shown in the figure 15 and the corresponding output of the comparator is shown in the figure 16 which shows the compared output of sine wave and a reference signal.

OUTPUT OF DUAL SLOPE ADC

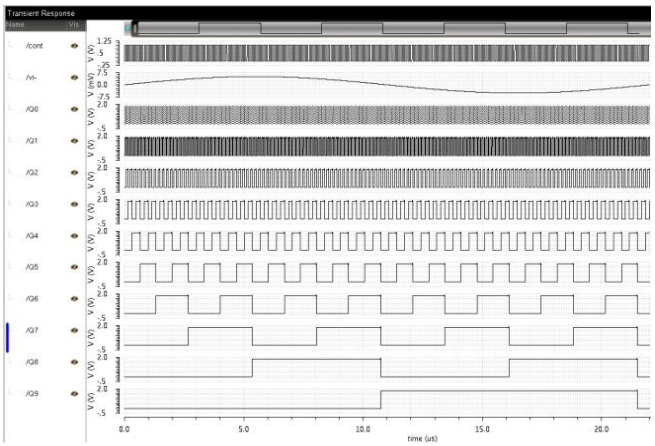

Fig.17. Output of ADC showing digital bits

Finally the output of the dual slope ADC is obtained using the designed blocks and the input analog signal and the corresponding output bits are shown in the figure 17.

OUTPUT POWER OF DUAL SLOPE ADC

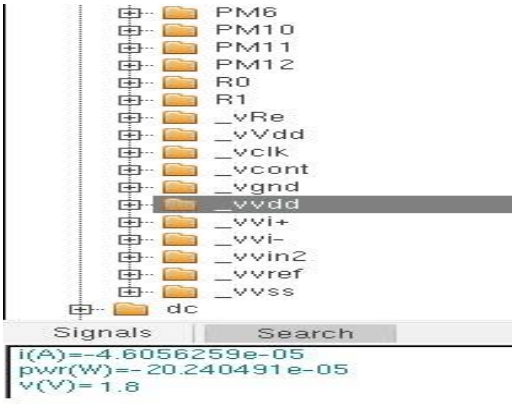

Figure. 5.18. power of Dual slope ADC

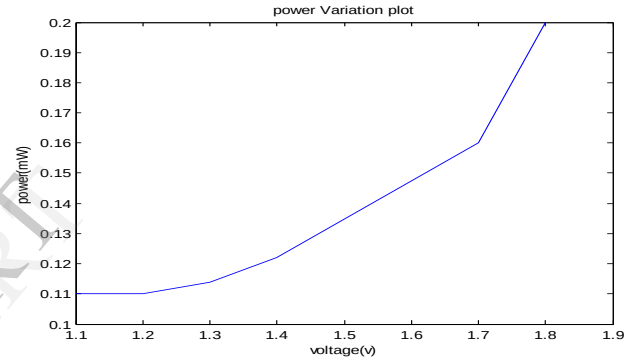

Figure. 5.19. power variation plot of SAR-ADC

The fig.5.18 shows the power consumption of Dual slope ADC when the operating voltage is 1.8V. The variation of plots from 1.1V to 1.8V is shown in the fig.5.19.

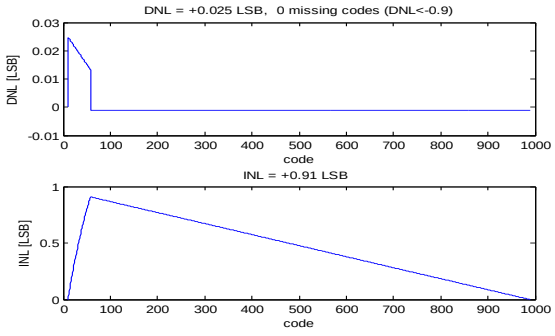

Figure. 5.20. INL and DNL for ADC using matlab

The INL and DNL for an analog to digital converter is calculated using the histogram principle and linearised histogram principle in matlab. The input vector given to the calculation is the ECG data observed from the body. Since the obtained ECG signal is noise less the INL and DNL values will be less as shown in the fig.5.24.

PARAMETERS OF DUAL SLOPE ADC

PARAMETERS	VALUES
Resolution	10 bits
Technology	180nm
Supply	1.1V to 1.8V
Input range	10mV
power	110.4µW to 202.4 µW
ENOB	4.69 bits
SNR	29.9 db
INL	0.91 LSB
DNL	0.025 LSB
I_{supply}	46µA
FOM	18.28µJ

4. CONCLUSION

In this work, dual-slope ADC is operated at 1.1v with high data rate which consumes power of 110.4µW. In contradict, a system operated at 1.8v which consumes power of 202.4 µW. This shows that applied voltage is proportional to the power consumption of the system. This system has been designed in CADENCE Virtuoso Analog Design environment with 180nm technology. . In future work, to implement dual-slope ADC for the wireless applications of ECG system.

5. REFERENCES

1 Andriana Voulkidou, Lambros Mountrichas, Stylianos Siskos An Adaptable 14-Bit Dual Slope ADC with Wide Input Range Procedia Engineering 47 (2012) 997 – 1000.

2 Alberto Rodríguez-Pérez, Manuel Delgado-Restituto and Fernando, MedeiroInstitute of Microelectronics of Seville, Power Efficient ADCs for Biomedical Signal Acquisition 2009.

3. Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U,A 10- bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS
4. Daniel Schinkel, Eisse Mensink, Eric Klumperink, Ed van Tuijl, Bram Nauta, A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time
5. Ehsan Rahiminejad and Reza Lotfi, A Low-Power Architecture for Integrating Analog-to-Digital Converters 2010.
6. Fan Hua, Wei Qi, Kobenge Sekedi Bomeh, Yin Xiumei,and Yang Huazhong, (Division of Circuits and Systems, Department of Electronic Engineering, Tsinghua University, Beijing 2008, China) An 8-bit 180-kS/s differential SAR ADC with a time-domain comparator and 7.97-ENOB.
7. Hamed Mazhab-jafari, 16 channel CMOS Impedance Spectroscopy DNA analyzer with Dual-slope multiplying ADC IEEE trans on biomedical circuits and systems oct 2012.
8. Hasan Krad, A Dual-Slope Integration Based Analog-to-Digital Convertor, American J. of Engineering and Applied Sciences 2 (4): 743-749, 2009.
9. James L. McCreary, student member, IEEE, and Paul r. Gray, member, IEEE, all-mos charge redistribution analog-to-digital conversion techniques—part-1.
10. Jens Sauerbrey, Doris Schmitt-Landsiedel, Roland Thewes, "A 0.5V, 1µW Successive Approximation ADC", IEEE Journal of Solid State Circuit, IEEE 2002.
11. Jie Yuan, Ho Yeung An activity-trigerred 95.3 dbDR-75.6 db THD CMOS Imaging sensor with digital calibration, IEEE journak of SSC oct 2009.
12. MAXIM Application note 1080 Understanding SAR ADCs Mar 01, 2001.
13. Phillip DAllen.,Douglas R Holberg., CMOS Analog circuit design second edition Oxford university press.
14. Pratibhadevi Tapashetti, Ankur Gupta, Design and Simulation of Op Amp Integrator and Its Applications, International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-1, Issue-3, February 2012