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Design Of Low Power 64-Bit SRAM Using 13T Cell

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Abstract

A new 13T SRAM cell has been designed at 180nm for low power and high performance. It employs single line read/write architecture. The output of the cell features a full rail-to-rail swing. The static power dissipation of 13T SRAM cell is 283.14µW, which constitutes solely 35% of 6T SRAM cell and comprises of higher SNM. The 64-bit SRAM memory was designed using the 13T cell and has a total power dissipation of 4.5mW.

1. Introduction

Reducing the static power dissipation is a major issue in the current low power design trend. Different design styles have been introduced to reduce static power dissipation. In high density circuit such as memory, reducing static power will bring down a major portion of power consumption [4,6]. This paper discusses a new SRAM cell design for low power purpose at 180nm level.

2. Working of 6T SRAM

The conventional 6T SRAM is shown in Fig 1. It has six transistors which form the two access transistors and two inverters connected which are connected back to back. The widths of these transistors are chosen carefully so that the cell has better read-write stability [1-2, 5]. The widths of the pull-down, pull-up and access transistors should be as follows.

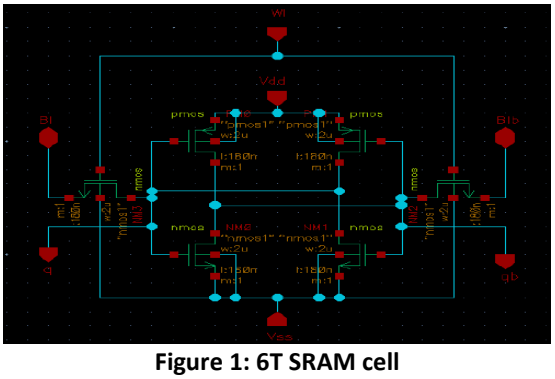

Figure 1: 6T SRAM cell

2.1. Reading

For read operation first both bl and blb are precharged to and then the WL is enabled. Based on the data stored in the cell, one of the bit line discharges. The bit lines are connected to a sense amplifier, which amplifies the signal and produces a rail-rail-swing in the right direction.

2.2. Writing

For writing, the data and ~data are connected to the bl and blb and then the WL is enabled. Now, the data is forced into the inverters and hence the data is written into the cell.

3. Working of 13T SRAM

In the new design, we has used forced stack technique and introduced a pass transistor between the back-to-back connections of the two inverters. The design features dedicated single line read/write architecture. The dedicated read & write port improves the noise margin of the SRAM. A 13T cell is shown in Fig 2.

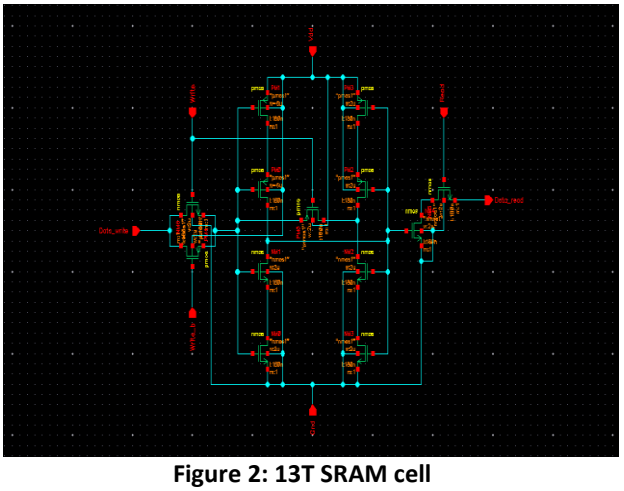

Figure 2: 13T SRAM cell

3.1. Writing

The data_write line is precharged to the required state (i.e. logic '0' or logic '1') and then WL is enabled. After enabling WL, the data is written into the cell. The pass-transistor cuts the feedback from the second inverter and is immune to any noise caused by the second inverter.

3.2. Reading

The data_read line is precharged to V_{dd} prior to the application of RL signal. Once RL is enabled, based on the data stored in the cell data_read line retains or discharges its charge.

4. 64-bit SRAM design

The 13T cell is replicated to form an 8x8 SRAM array. Lyon-Schediwy decoder is used to decode the address. A sense amplifier based on is used. The entire module is **designed at** 180nm technology.

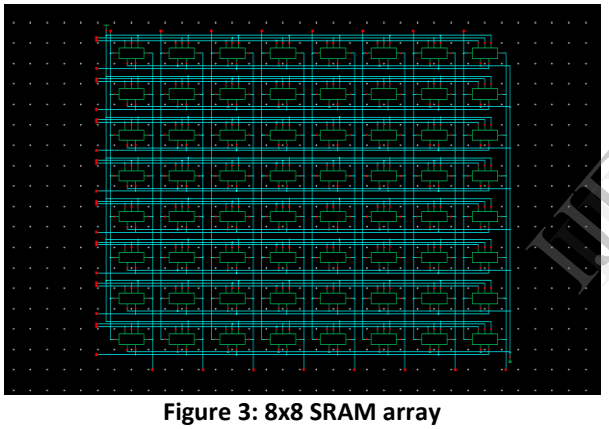

Figure 3: 8x8 SRAM array

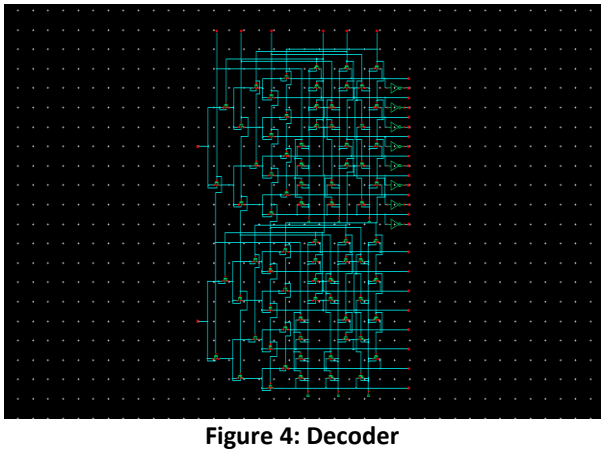

Figure 4: Decoder

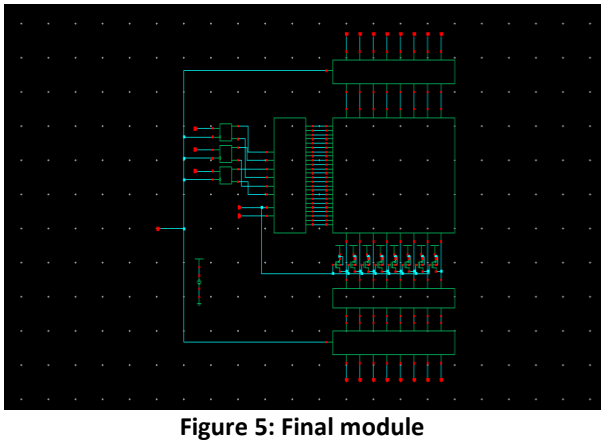

Figure 5: Final module

5. Result

Simulations are performed at 180nm using cadence tool. The static power, dynamic power and total power dissipation of different SRAM designs [1,2] are tabulated in table 1.

The SNM for each design is also tabulated in table 2. The SNM graph of 13T SRAM is shown in fig. The simulated waveform of 64-bit module is shown in fig. the static and dynamic power dissipation of the 64-bit module is 4.513mW and 22µW respectively at 200MHz.

Table I: Power dissipation in various SRAM design.

Design	Dynamic Power	Static Power	Total Power
6T	313.04pW	802.121uW	802.121uW
8T	1.493nW	561.886uW	561.887uW
11T	149.317nW	373.487uW	373.636uW
13T	161.273nW	283.14uW	283.33uW

Table II: SNM of various SRAM design

Design	Read SNM (V)	Write SNM(V)
6T	0.75	0.03
8T	0.70	0.04
11T	0.70	0.14
13T	0.70	0.685

6. Reference

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