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# Design of Low Power 14T SRAM using 45 nm CMOS Technology

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***Abstract*— SRAM (Static Random Access Memory) is a memory used to store data. Low-Power and High-Performance have become a burning issue in VLSI industries these days. Among the various embedded memory technologies, SRAM has the ability to provide the highest performance while maintaining low standby power consumption. High leakage current in deep submicron technology is becoming a significant contributor to the power dissipation of CMOS circuits as the threshold voltage, channel length and gate oxide thickness are reduced. Due to excessive scaling of CMOS device, low power is the major challenge for today's electronics industries. Over the last few decades, we are scaling down the CMOS devices to achieve better performance in terms of speed, power dissipation, size, and reliability.**

**In this paper, our main focus is to make a 14-T SRAM 1-bit cell and 14-T SRAM for 8-bit cell, with low input voltage and lower power consumption. In general, the electronics devices are becoming more compact in terms of size, better speed, less power consumption so we are moving towards the new technology. This can be done by making memories compact and faster so the scaling of CMOS is done.**

**The technology used to implement the 14-T SRAM is 45 nm technology and the software used is Tanner EDA.**

***Keywords*— SRAM, Low-Power, High-Performance, etc.**

## I. INTRODUCTION

With the advancement in design technology, it is now possible to integrate millions of transistors on a smaller area [1].

This dissertation work revolves around low power consumption of 14-T SRAM and comparison with 12-T SRAM in 45 nm technology. SRAM is a type of semiconductor memory which uses bi-stable latching circuitry to store a single bit [2]. The word static means that it need not be refreshed periodically unlike DRAM (Dynamic Random Access Memory). SRAM exhibits data-remanence but still, it is volatile memory as it eventually loses the data when memory is not powered [3].

According to ITRS roadmap in 2013, SRAMs occupy more than 90 percent of chip area [4] so its power dominates the overall power of the chip. The main part of the power dissipation in SRAMs is its leakage power; switching power consumption of big capacitances on bit-lines and word-lines of SRAM array. One of the most effective solution to reduce the power consumption of SRAM is by reducing the supply voltage of the chip [5].

Embedded SRAMs provide a direct means of bringing the benefits of transistor-level density-scaling to the circuit and architecture levels and therefore vital to this new model of IC scaling [6]. SRAMs must be specially designed by keeping their application in mind, it is worth considering the application constraints. This work specifically considers the number of applications where required area, power consumption, and high performance are paramount. Of course, the SRAM challenges associated with high-performance applications, including desktop and server computing, requires very targeted and innovative solutions as well [7] [8] [9]. Some of the applications of SRAMs with highly energy-constrained are:-

TABLE I. EXISTING & EMERGING APPLICATIONS OF SRAM FOR VARIOUS DEVICES

| **Application** | **Performance Specification** | | |
|---|---|---|---|
| | ***Power*** | ***Processor*** | ***Energy Source*** |
| Pacemaker & Cardioverter – defibrillator [10] [11] | < 10 µW | 1 Khz DSP | 10 years life-time battery |
| Hearing aid & cochlear implant [12] [13] [14] | 100 – 2000 µW | 32 Khz – 1Mhz DSP | 1 week life-time battery |
| Neural recording [15] [16] | 1-10 µW | n/a | Inductive Power. |
| Body – area monitoring [17] | 140 µW | < 10 Mhz DSP | Battery |
| Mobile Multimedia | Minimize Power (For Long Battery Life) | Up to 100 Mhz | Battery |
| Industrial & automotive sensing | < 100 µW | ~ 100 Khz | Battery |
| Environment Monitoring | < 100 µW | ~ 100 Khz | Battery |
| Structural Monitoring | < 100 µW | ~ 100 Khz | Battery |
| Military Surveillance & Detection | < 100 µW | ~ 100 Khz | Very small battery with high life-time. |

Over the last few decades, we are scaling down the CMOS devices to achieve better performance in terms of speed, power consumption, noise margin, delay, etc. But due to excessive scaling of CMOS technology, we are facing some challenges, the minimum spacing between the transistors is reduced. So, multiple transistors are susceptible to the charge

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deposited from a single particle strike compared to the older process where only one transistor was affected [18].

The charge sharing results in Single-Event-Multiple-Node upsets (SEMNUs), which is becoming the main effect of energetic particle strike in emerging nanometer CMOS technology [19] [20]. In addition to it, if the supply voltage is reduced further, it increases the susceptibility of circuits to radiation. Thus, the requirement of radiation-hardening technologies in digital circuits is extremely urgent [21]. Due to the larger sensitive volume per bit and lower node capacitance than the dynamic counterpart, SRAM is more prone to soft errors. Therefore, the soft error rate (SER) [22] in SRAM is increased with more technology scaling toward nanometer regime. The rest of the paper is organized as follows. Section II reviews the structure of 45 nm 12T SRAM bitcell. Section III introduce and explain the proposed 45 nm 14T SRAM bitcell and 45 nm 14T SRAM for 8-bit cell. Section IV describes the simulation steps and present the performance analysis. Section V concludes the discussion.

## II. 45 NM 12-T SRAM BITCELL

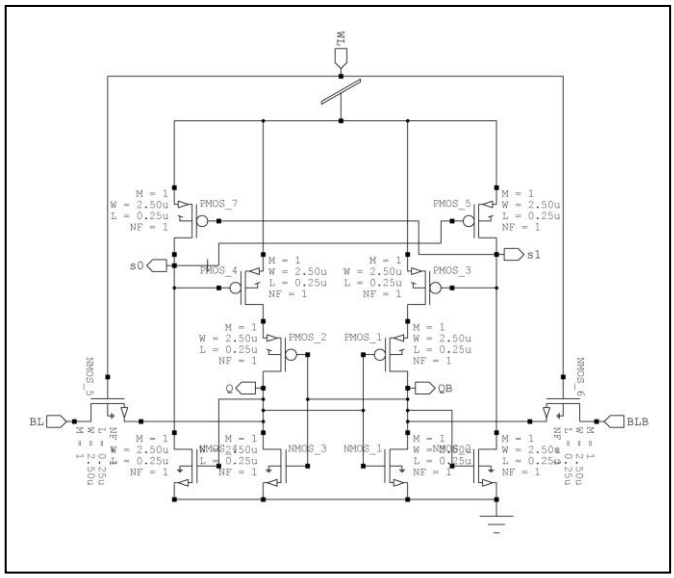


Fig. 1. 12T SRAM Bitcell

The functional analysis of the existing 12T SRAM bitcell as shown in Fig. 1. Is presented as:

1. Write Operation: We assume that Q = '1' & QB = '0' and the bitlines BL and BLB are set to '0' and '1', respectively. Then when the WL is activated, the value stored in Q and QB will be changed to '0' and '1' respectively. Then when the WL is activated, the value stored in Q and QB will be changed to '0' and '1' respectively. After that, once WL is discharged to '0', the new state of the memory cell is stored.

2. Read Operation: The BL and BLB are precharged to '1'. When the selected WL is enabled, the transistors NMOS_5 and NMOS_6 are turned ON, BLB will be discharged through transistors NMOS_6 and NMOS_1. As a result, the differential voltage of the BL & BLB will be generated and amplified by the sense amplifier.

3. Hold Operation: WL is deactivated and the storage nodes are isolated from the BL & BLB; thus they maintain the initial state [23].

The 12T SRAM bitcell gives the favourable radiation hardness performance. Beside the tolerance for a Single-Event-Upset (SEU) on any of its internal single nodes, it can also provide the SEMNUs immune to some extent. Unfortunately, the slow write speed, as well as large power consumption, limits the application of it [24].

## III. PROPOSED 45NM 14T SRAM BITCELL

In the existing method implementation part, the performance analysis and comparison between different parameters like power consumption and delay of existing 45 nm 12T SRAM and proposed 45 nm 14T SRAM is shown here.

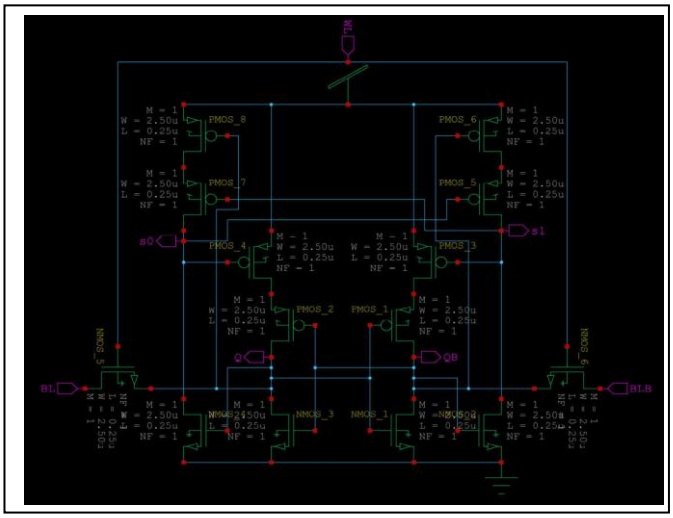


Fig. 2. 14T SRAM Bitcell

The read, write and hold operations of the proposed 45 nm 14T SRAM bitcell is same as the 12T SRAM. In this design shown in Fig. 2. the transistors PMOS_6 and PMOS_8 are used to control the connection or cutoff between the power supply and transistors PMOS_5/PMOS_7, which are beneficial to improve the write speed and power consumption.

Proposed 45 nm 14T SRAM for 8-bit cell

In this proposed design we have connected eight 14T SRAM to make a 8-bit SRAM cell as shown in the figure below.

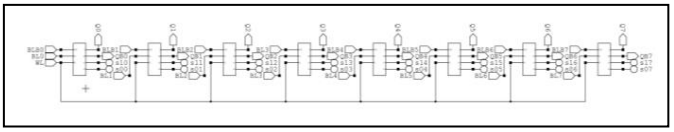

Fig. 3. 14T SRAM for 8-bit cell

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## IV. SIMULATION RESULTS AND PERFORMANCE ANALYSIS

The proposed SRAM architectures are realized in 45 nm CMOS process technology using Tanner EDA tool. The performance evaluation is done by subjecting the schematics topology to various combinations of inputs.

The effectiveness of the topology is analyzed for power supply of 0.9V to 12T SRAM and 14T SRAM respectively.

### *A. Testbench of Existing 12T SRAM bitcell*

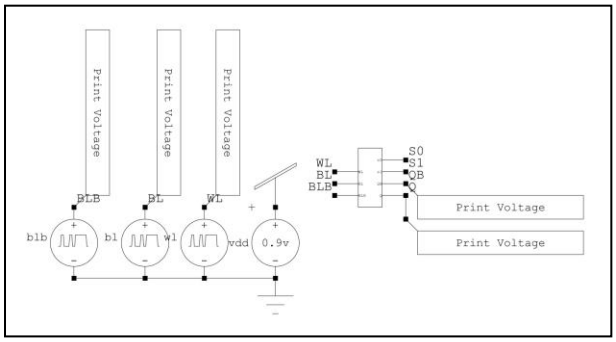


Fig. 4. Testbench of 12T SRAM bitcell

### *B. Waveforms of 12T SRAM bitcell when $V_{DD}$ = 0.9V at 45 nm*

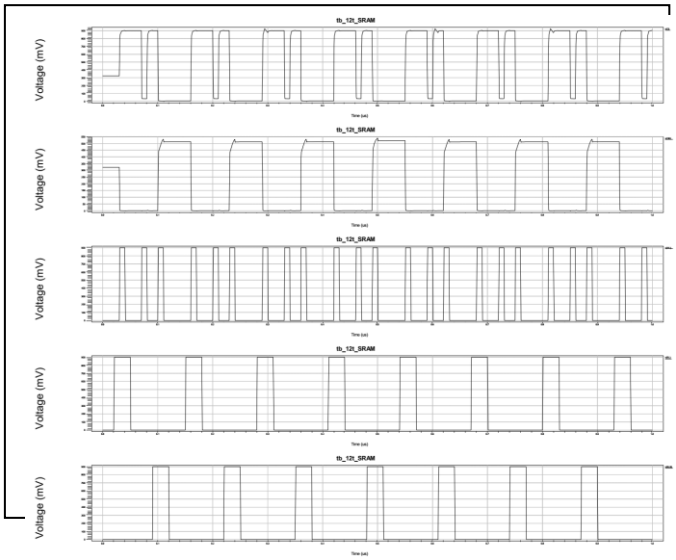


Fig. 5. Simulation waveform of 12T SRAM

TABLE II. PERFORMANCE ANALYSIS OF 12T SRAM BITCELL

| Name of Topology | Input Voltage | Transistor Count | Delay (nS) | Power (nW) |
|---|---|---|---|---|
| 12T SRAM bitcell | 0.9 V | 12 | 20.013 | 24494.51 |

### *C. Testbench of Proposed 14T SRAM bitcell*

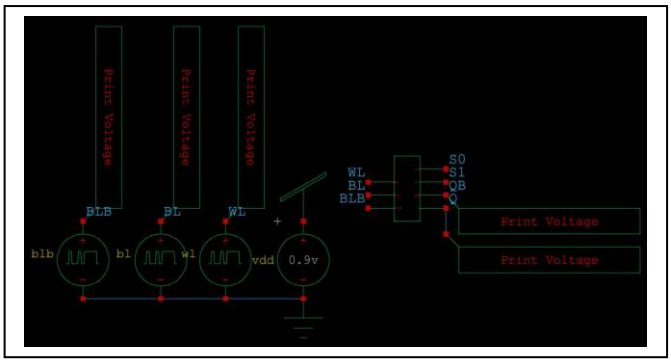


Fig. 6. Testbench of 14T SRAM bitcell

### *D. Waveforms of 14T SRAM bitcell when $V_{DD}$ = 0.9V at 45 nm*

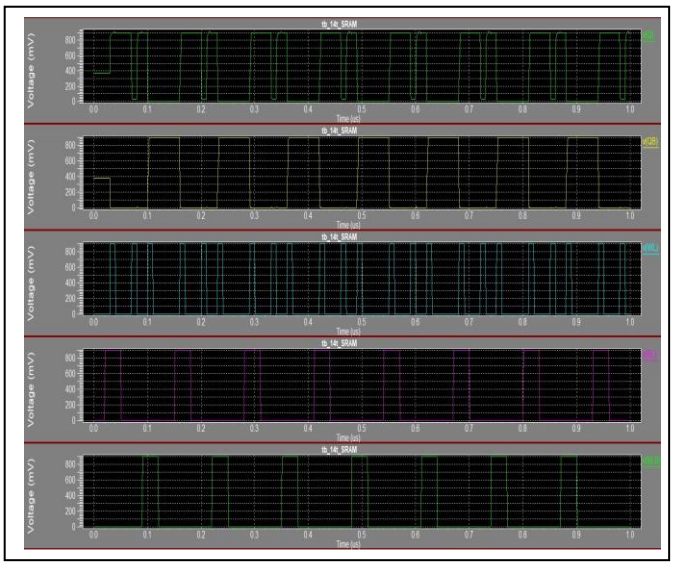


Fig. 7. Simulation waveform of 14T SRAM

TABLE III. PERFORMANCE ANALYSIS OF 14T SRAM BITCELL

| Name of Topology | Input Voltage | Transistor Count | Delay (nS) | Power (nW) |
|---|---|---|---|---|
| 14T SRAM bitcell | 0.9 V | 14 | 20.016 | 5440.613 |

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### *E. Testbench of Proposed 14T SRAM for 8-bit cell*

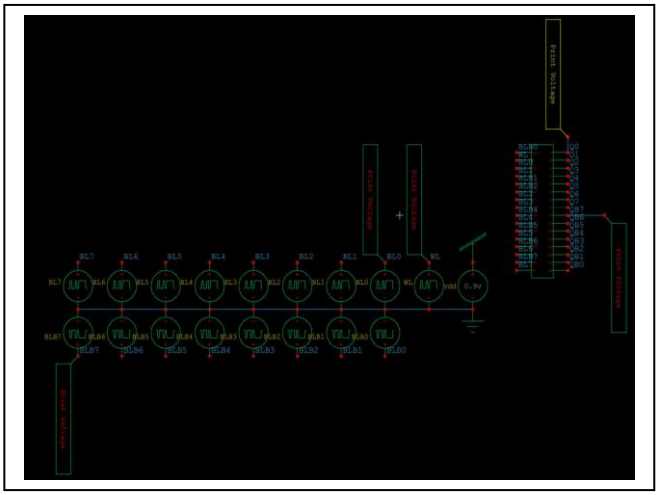

Fig. 8. Testbench of 14T SRAM for 8-bit cell

### *F. Waveforms of 14T SRAM for 8-bit cell when $V_{DD}$ = 0.9V at 45 nm*

Fig. 9. Simulation waveform of 14T SRAM for 8-bit cell

TABLE IV. PERFORMANCE ANALYSIS OF 14T SRAM FOR 8-BIT CELL

| Name of Topology | Input Voltage | Transistor Count | Delay (nS) | Power (nW) |
|---|---|---|---|---|
| 14T SRAM for 8-bit cell | 0.9 V | 112 | 19.659 | 36504.41 |

TABLE V. COMPARISON OF DELAY AND POWER OF VARIOUS SRAMS

| Sl. No. | Different SRAM Architectures | Input Voltage | Delay (nS) | Power (nW) |
|---|---|---|---|---|
| 1. | 12T SRAM bitcell | 0.9 V | 20.013 | 24494.51 |
| 2. | 14T SRAM bitcell | 0.9 V | 20.016 | 5440.613 |
| 3. | 14T SRAM for 8-bit cell | 0.9 V | 19.659 | 36504.41 |

The performance of the 14T SRAM architecture proposed in the paper is compared to the existing 12T SRAM, the comparison results are tabulated in TABLE V. The low power 14T SRAM realized in 45 nm technology accounts for a delay of 20.016 nS which is a little bit more than 12T SRAM. Also, the power consumption associated with it is 5440.613 nW which is much less than the existing 12T SRAM.

The data in TABLE V also shows that a 8-bit SRAM designed with 14T SRAM has delay around 19.659 nS and power consumption of 36504.41 nW and from this, we can observe that power consumption of 8-bit SRAM is also much less when designed with 14T SRAM.

The power consumption associated with the proposed design has become much lower than the previous design, though the delay is a little bit more. The overall performance offered by the proposed design is much better compared to the previous design architecture.

## V. CONCLUSION

The power dissipation is the main concern in high-speed memories. In this paper, a novel low voltage & low power based 14T SRAM has been proposed which gave the better average power than the 12T SRAM. From the results, we can observe that 14T SRAM is the better one. The result table can be helpful to select an SRAM to design and fabricate memory chips which are best suitable for different types of applications.

For power constrained devices like space applications the SRAM cell which consumes minimum power should be used, for area-constrained like biomedical devices the SRAM cell which consumes minimum area should be used and for very fast processing devices the SRAM cell having minimum delay must be used. Although the number of transistors, area, and delay increased in this proposed SRAM cell but low power dissipation can shadow these drawbacks. This proposed SRAM cell can provide low power requirement where we require high-speed memory operation.

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