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Design of Low Noise Amplifier for mm-Wave Applications

Namita Palecha
Assistant Professor
Electronics and Communication Department,
RVCE Bengaluru, India

Praneet Jain
Electronics and Communication Department,
RVCE Bengaluru, India

Nikith K Kottary
Electronics and Communication Department,
RVCE Bengaluru, India

***Abstract*—This paper proposes a transformer based low noise amplifier in 45 nm CMOS process and working at E band frequency range. The CS amplifier is used because of better noise performance and the cascade stage is used for higher gain. The impedance matching network is used to obtain 50 ohms .This LNA gives a gain of 11db at a frequency 67 Ghz and noise figure of 43 dB at 67 Ghz frequency.**

***Index Terms*—CMOS process, CS amplifier, LNA, Noise figure**

I. INTRODUCTION

The E band range (71-76 and 81-86 GHz) of frequency has become extremely important with the advancements in the 5G communications [2].The data rates can be increased to a good number if the communication takes place at this range. This can eliminate the cost of optic fibers which are usually used for high speed communication [2].

LNA(Low noise amplifiers) play an important role in the wireless receiver system and its gain variable is of very high importance at a high frequency [1] [2] .There have been some research on E band LNA at 90nm.[1][2] This paper proposes a LNA at 45nm technology which will help in reducing the area and also increases the speed which better fits the receivers used in the new generation 5G phones

II. CIRCUIT DESIGN

In this high frequency low noise amplifier design cascade topology and common source topology are used. Although the cascade topology (the stacked structure) provides higher gain but requires a high drive voltage. The common source stage is used as it has a better noise performance and also it consumes a very less dc power which is suitable for low power application [4]. Hence a combination of both is used so that there is an equal trade-off between the power and the gain.Figure 1 shows the implemented high frequency 3 stage low noise amplifier. The inductor values are chosen such that they match the input impedance of the transistors for next stage [1]. The capacitors are used for eliminating the dc components if any and provide good waveform at the output. The last stage consist of a common source stage that amplifies the power of the signal transmitted.

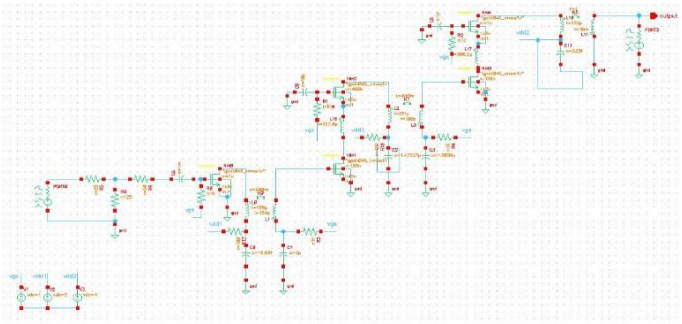

Fig. 1. Schematic Diagram

III. CIRCUIT SPECIFICARIONS

The transistors NM0, NM2 and NM4 have larger width than usual in order to provide adequate current to drive the next stage.Whereas NM1 and NM3 have usual 120nm width to provide less resistance in the path.It is worth noting that there less resistance is required because they act as input resistance to a common gate amplifier(the stacked structure behaves as a common gate amplifier).The tableI list the dimensions of the transistors and library used to simulate them.

TABLE I MOSFET SPECIFICATIONS

Component Used	Library	Values
NM0	gpdk045	45 nm X 1 um
NM1	gpdk045	45 nm X 120 nm
NM2	gpdk045	45 nm X 600 nm
NM3	gpdk045	45 nm X 120nm
NM4	gpdk045	45nm X 1um

The resistor(R),capacitor(C),inductor values have been de- termined for proper matching and biasing.The table II lists the values used.

IV. SIMULATION RESULTS AND ANALYSIS

Above schematic has been designed in the Virtuoso Tool using Schematic Editor XL.The analysis that have been per- formed are as follows:-

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TABLE II
ANALOG COMPONENTS SPECIFICATIONS

Component Used	Library	Values
R0	analogLib	1K ohms
R1	analogLib	1K ohms
R2	analogLib	1K ohms
R3	analogLib	1K ohms
R4	analogLib	1k ohms
R5	analogLib	25 ohms
R8	analogLib	25 ohms
R9	analogLib	50 ohms
R15	analogLib	100 ohms
R17	analogLib	100 ohms
L0	analogLib	188 pH
L1	analogLib	194 pH
L2	analogLib	151 pH
L3	analogLib	180 pH
L10	analogLib	253 pH
L11	analogLib	10 mH
L17	analogLib	306.2 pH
L18	analogLib	352.6 pH
C0	analogLib	16.83 Ff
C1	analogLib	2 pF
C2	analogLib	1.4752 pF
C3	analogLib	1.9039 pF
C5	analogLib	1 mF
C8	analogLib	10 pF
C9	analogLib	1 pF
C11	analogLib	223 f F

- Transient:- The transient analysis has been performed for 200ps with a -20 dBm source as input at 67 GHz frequency which is the starting frequency of E-Band.
- S-Parameter :- S-Parameter analysis have been performed for frequency ranging from 67 GHz to 90 GHz with port0 as input port and port3 as output port.
- NF(Noise Figure) :- Noise figure plot has been obtained by using the direct plot options in the ADE-L window. The direct plot option contains various results that can be plotted from the various analysis performed.
- VSWR(Voltage Standing Wave Ratio) :- VSWR plot has been plotted from the direct plot option present in the results option of the ADE-L window.

The gain obtained is 10.96 dB (Fig.2) and the Noise figure ranges from 43.1 db to 43.5 db (Fig. 4) in the spectrum of
67 Ghz to 90 Ghz frequency range. The s parameters are used to analyze any high frequency circuit. The provide us a method to characterize any high frequency circuit.The very low value of S11 (Fig. 3) suggest that there are very few reflections which is very much necessary for the rf circuits. The reflections (if there are any) in any rf circuits can cause the circuit to misbehave and increase the power loss.

VSWR provides information about the standing waves aris- ing due to reflection of electromagnetic waves from the metal contacts.VSWR values ideally should be 1 and in the current design it has a value of 1.0108.The VSWR Plot(Fig. 5) is as shown below.

The results are tabulated and is shown in the following table III

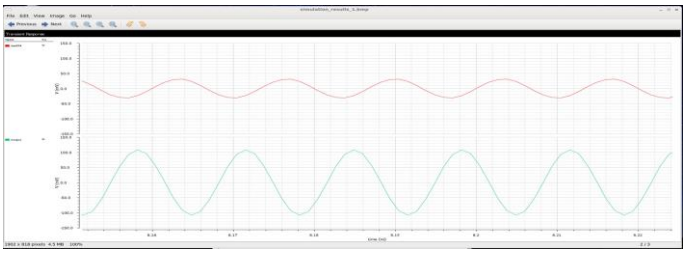

Fig. 2. Gain Plot

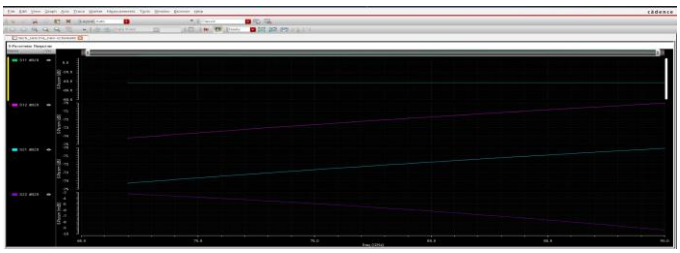

Fig. 3. S Parameters Plot

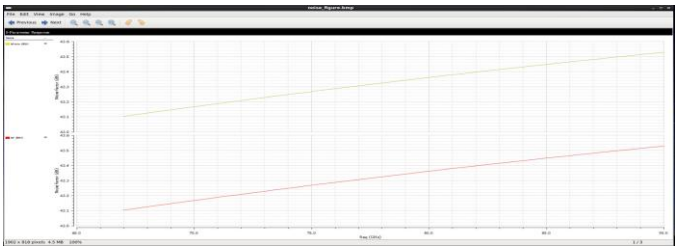

Fig. 4. Noise Figure Plot

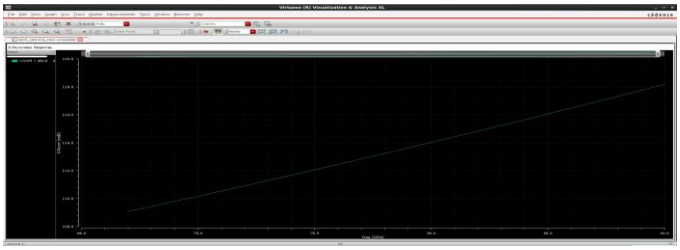

Fig. 5. VSWR Plot

TABLE III
RESULTS OBTAINED AT 67 GHZ FREQUENCY

Parameters	Value
Gain	10.959 dB
VSWR	0.109 dBm
NF	43.1 dB

V. Conclusion

The LNA has been designed and simulated using Virtuoso and Spectre tool of Cadence design system respectively. The complete design is done using 45nm technology library and the analogLib file for the resistors , capacitors and inductors. The gain is around 11db and can be further improved by correct matching circuit. The VSWR and NF parameters are also plotted and calculated using hb and sp analysis respectively.

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