Design of High Speed Fir Filter

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Abstract:- **FIR filter is used in almost all digital applications. Efficient implementation of FIR filter can be achieved by the usage of efficient adder in the FIR filter. The Proposed method implements the FIR filter in a Xilinx environment using carry select adder and found to be having 5% decreased delay than the conventional FIR filter**.

I. INTRODUCTION

FIR (Finite Impulse Response) filter is a digital filter, which produces Finite Impulse Response as output for a given finite input sequence [1]. FIR filter is used in digital applications. Some of the advantages of FIR filter are stability, easy to design and has no feedback. FIR filter consists of multiplier, adder, and delay unit. These adder and Multiplier used in FIR filter produce high computational Delay. This delay can be commendably reduced by the usage of efficient adder. Figure 1 shows block diagram of conventional FIR filter.

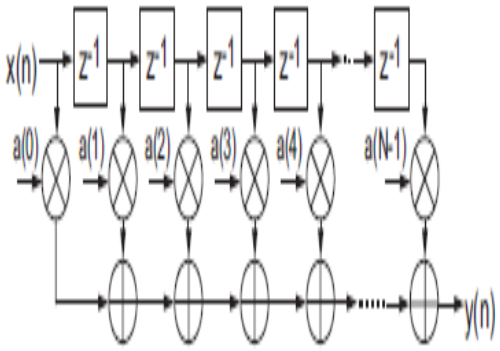

Fig. 1. Block diagram of Conventional FIR Filter [1]

II. MAC UNIT

In digital signal processing, the multiply and accumulate operation is a common step that computes the product of two numbers and adds that product to an accumulator. This multiply and accumulate unit is commonly referred to as MAC unit as in figure 2. MAC unit is also used in FIR filters. Efficient design of MAC unit means the efficient design of FIR filter. This paper deals with FIR filter implemented using MAC unit containing Wallace tree multiplier and carry select adder.

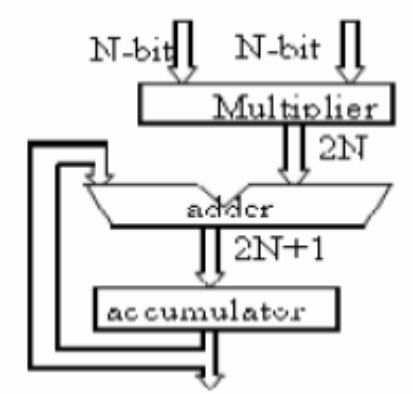

Fig. 2. MAC unit [1]

III. CARRY SELECT ADDER

The Carry select adder comes in the category of conditional sum adder. Conditional sum adder works on some condition. Sum and carry are calculated by assuming input carry as 1 and 0 before the input carry comes. When actual carry input arrives, the actual calculated values of sum and carry are selected using a multiplexer [2].

The carry select adder (CSLA) generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry-in being zero and the other assuming it will be one. After two results are calculated, the correct sum, as well as the correct carry-out is then selected with the help of multiplexer once the correct carry-in is known. The basic structure of carry select adder is given in figure 3.

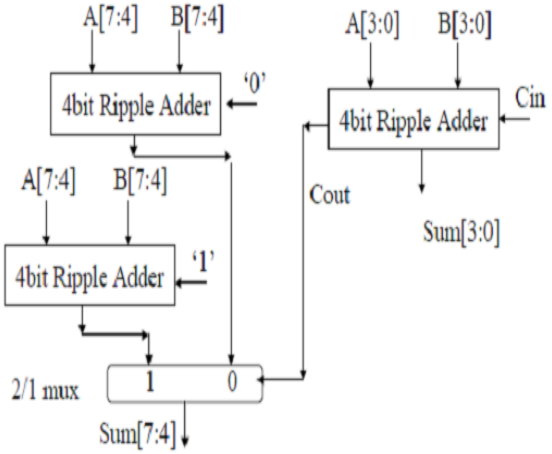

Fig. 3. Carry select adder

IV. WALLACE TREE MULTIPLIER

With the recent advances in technology, a number of multiplication techniques have been implemented for fulfilling the requirement of producing high speed, low power consumption, less area or a combination of them in one multiplier. Speed and area are the two major constraints, which conflict with each other. Therefore, it is the designer's task to decide proper balance in selecting an appropriate multiplication technique as per requirements.

Parallel multipliers are the high-speed multipliers. Therefore, the enhanced speed of the multiplication operation is achieved using various schemes and Wallace tree is one of them [3]. Wallace tree multiplier uses carry save adder to add partial products. The structure of 8-bit Wallace tree multiplier is shown in figure 4.

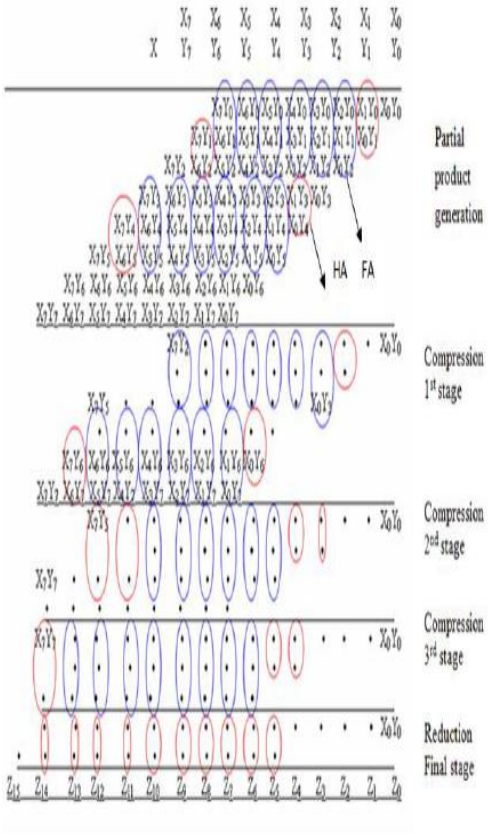

Fig. 4. 8-bit Wallace tree multiplier

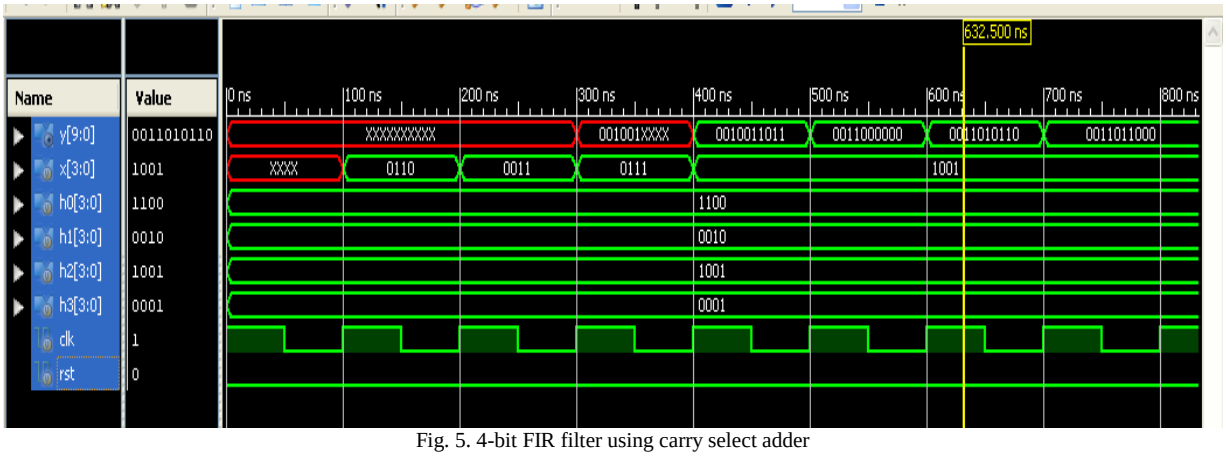

Fig. 5. 4-bit FIR filter using carry select adder

V. RESULTS AND DISCUSSION

The proposed FIR filter is simulated and implemented in Xilinx 12.1 environment targeted for the device Spartan 6 XC6SLX16. The simulation result for 4-bit and 8-bit FIR filter using carry select adder is shown in figure 5 and 6 respectively. 4-bit and 8-bit FIR filter using carry skip adder is shown in figure 7 and 8 respectively. Existing system using carry skip adder is compared with proposed system using carry select adder in terms of delay and it is shown in table 1.

Table. 1 Delay comparison

	Adder used	**Delay (ns)**
Existing	Carry skip	30.77ns
proposed	Carry select	29.01ns

Fig. 6. 8-bit FIR filter using carry select adder

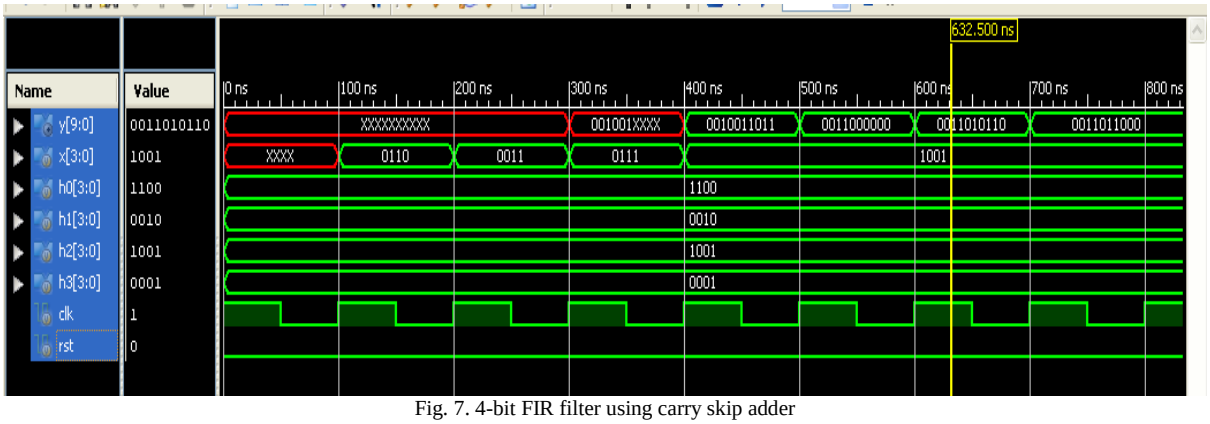

Fig. 7. 4-bit FIR filter using carry skip adder

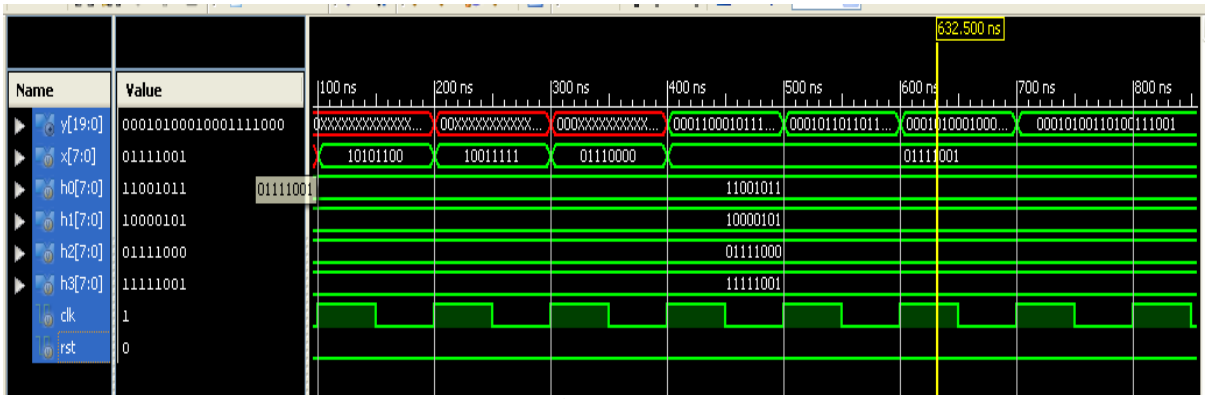

Fig. 8. 8-bit FIR filter using carry skip adder

VI. CONCLUSION

In this paper, 4-bit and 8-bit third order FIR filter is simulated with carry skip as well as carry select adder. Results show that carry select adder has lower delay when compared with carry skip adder. Higher bit FIR filter will be interesting for future work.

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