Design of High Speed and Area Efficient Modified Carry Select Adder

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***Abstract*— Adders are commonly used in many data-processing processors to perform arithmetic operations. Regular Carry Select Adder is one of the techniques used to perform addition faster and computes n+1 bit sum for two n-bit numbers. Regular Carry Select are faster than the ripple carry adder. The Modified Carry Select adders are area efficient when compared to the regular carry select adder which used two ripple carry adder. Modified carry select adder uses BEC to add one circuit and reduces area furthermore, such that total gate count is reduced. Area efficient modified carry select adder further reduces area by modifying the circuit. The result shows that the area efficient modified carry select adder is better than the modified carry select adder.**

***Key words* — Regular Carry Select adder, Modified Carry Select adder, Area Efficient Modified Carry Select adder.**

I. INTRODUCTION

The optimization of gates in digital circuits is essential. In VLSI system design the design of area and power efficient high speed logic systems are most essential. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.

The regular CSA which uses two sets of Ripple carry adders for cin=0 and cin=1. The CSLA is used in many systems to overcome the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum.

The Modified Carry Select Adder replaces the RCA block with the Binary to Excess-1 converter to reduce the area. The gates utilization in the BEC block is less compared to the RCA block. The main advantage of this BEC logic comes from the lesser number of logic gates than Full Adder (FA) structure.

The Area Efficient Modified Carry select adder further reduces the usage of gates. The full adders are replaced by the half adders, thus the area can be greatly reduced.

The outline of the paper is as follows. In this paper the section II describes the evaluation of gates in the adder block; the section III describes the evaluation of gates in the Modified Carry select adder, and section IV describes the evaluation of gates in the area efficient modified carry select adder, and section V describes the result. Finally; the conclusion of the paper.

II. EVALUATION OF GATES

The utilization of gates for the various adder structures are listed out in the table I.

Table1. Adder Block:

ADDERS BLOCK	GATES
Full Adder	13
Half Adder	6
XOR	5
2:1 Multiplexor	4

From the table I we can come to know that how many gates are been utilized for the half adder, full adder, multiplexers structures.

III. GATE EVALUATION IN MCSLA:

The modified carry select adder uses RCA block for the carry cin=0 and BEC-1 converter block for the carry cin=1. The structure of group 1 Modified carry Select Adder is shown in fig 1a.

The Boolean expressions of the 4-bit BEC is listed as

X0 = ~B0

X1 = B0 ^ B1

X2 = B2 ^ (B0 & B1)

X3 = B3 ^ (B0 & B1 & B2)

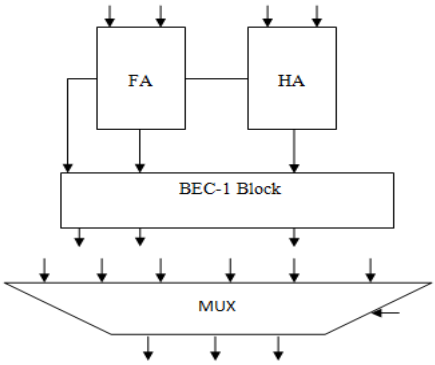

Fig 1a. Group 1

The group 1 structure uses a half adder and a full adder to perform the carry cin=0 operation and for carry cin=1 the BEC-1 converter block is used.

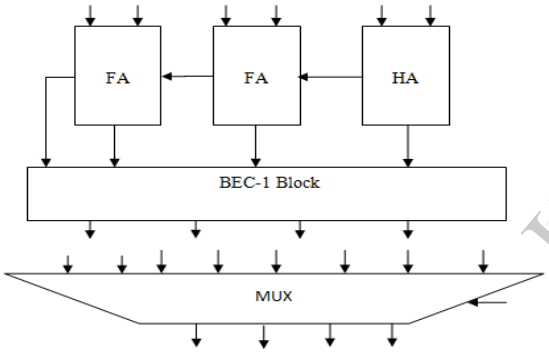

Fig 1b. Group 2

The group 2 structure uses a half adder and two full adders for cin=0 and BEC-1 block for cin=1.

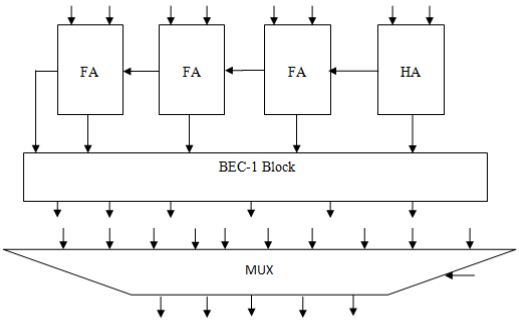

Fig 1c. Group 3

The fig 1c shows the group 3 structure. The group 3 consist of a half adder and a three full adder for cin=0 and the BEC-1 block for the cin=1.

The table 2 shows the gates required for Modified Carry Select Adder for the various groups.

Table 2. Gate count for MCSLA:

GROUPS	MCSLA
GROUP-1	43
GROUP-2	66
GROUP-3	89

IV. Gate Evaluation in Area Efficient MCSLA:

The area efficient modified carry select adder is shown in the fig. The group 1 structure has been shown Fig 2a. Two input variables of 2-bit length.

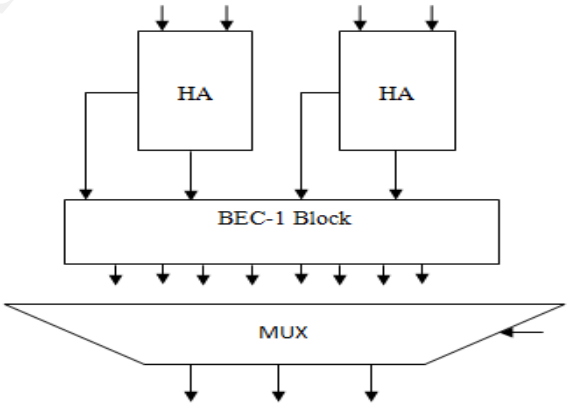

Fig 2a.Group 1

The group 1 structure uses Two half adder for cin=0 and BEC-1 block for cin=1. The MUX are used to select the sum and the carry for cin=0 or cin=1 depending upon the select input to the MUX. One full adder has been replaced with the half adder in order reduce the gate count. The group 2 structure has been shown in the Fig 2b.

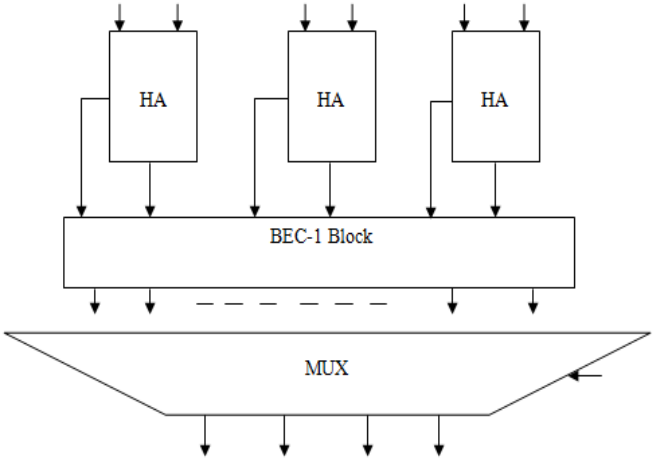

Fig 2b. Group 2

The group 2 structure uses Three half adder for cin=0 and BEC-1 block for cin=1. Two full adders have been replaced with the half adder in order to reduce the area.

The group 3 structure uses four half adder and the BEC1 converter and the MUX to select the required sum and the Carry. Three full adders have been replaced by the half adder in this structure.

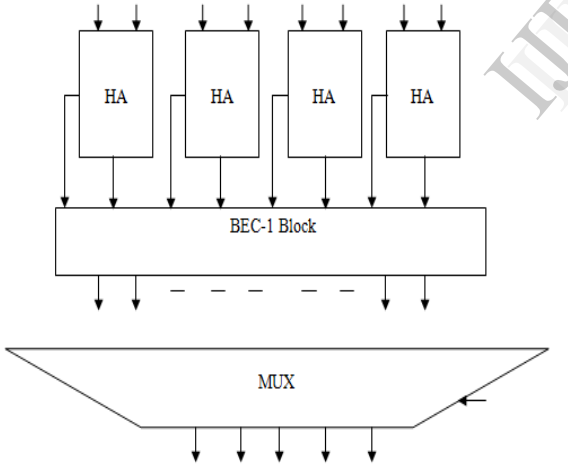

Fig 2c. Group 3

The Table 3 shows the total gates required for the Area Efficient Modified Carry Select Adder for various groups.

Table 3. Gate count for AE-MCSLA:

GROUPS	AE-MCSLA
GROUP-1	40
GROUP-2	60
GROUP-3	80

The total gate count for the regular carry select adder, modified carry select adder and area efficient modified carry select adder are shown in the table 4.

Table 4. Comparison of Gates Used in adders:

GROUPS	RCSLA	MCSLA	AE-MCSLA
GROUP-1	57	43	40
GROUP-2	87	66	60
GROUP-3	117	89	80

V. RESULTS

The proposed design has been successfully tested using the Xilinx tool. The simulated results have been shown in the Fig 3. The proposed design requires less number of gates to compare to the existing technique. Thus the area can be greatly reduced by using the area efficient modified carry select adder. The simulation results for various groups have been shown in the fig 3a, fig 3b, fig 3c.

Table 5: area comparison of various adder:

Groups Cell area	RCSLA	MCSLA	AE-MCSLA
Group-1	73	61	56
Group-2	114	94	85
Group-3	156	127	113

Table 6: delay comparison of various adder:

Groups	MCSLA DELAY(ns)	AE-MCSLA DELAY(ns)
GROUP-1	6.837	6.798
GROUP-2	8.933	7.898
GROUP-3	9.179	8.959

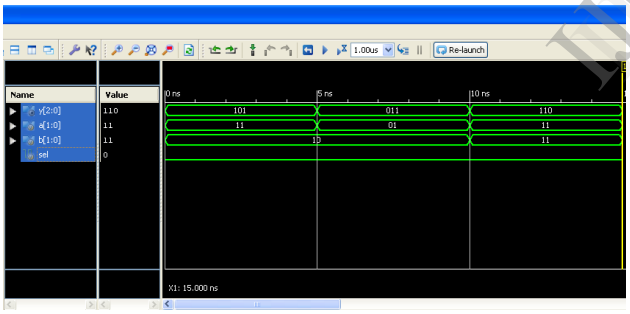

Fig 3a.Simulation Result of Group 1 AE-MCSA

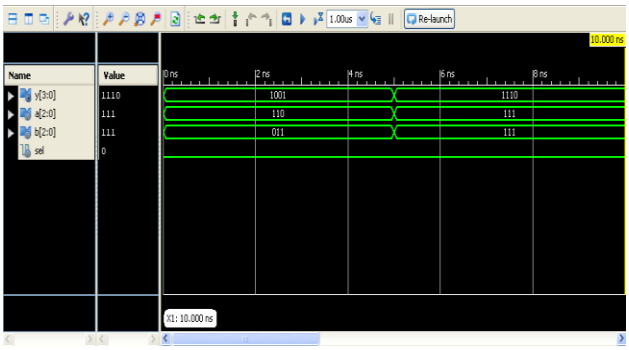

Fig 3a.Simulation Result of Group 2AE-MCSA

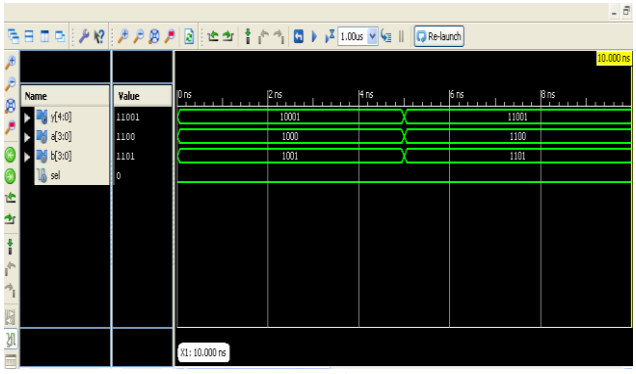

Fig 3a.Simulation Result of Group 3 AE-MCSA

VI. Conclusion

A simple approach is proposed in this paper to reduce the area of modified carry select adder architecture. The vast reduction in the total number of gates is advantageous in terms of both area and power..

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