Design of high gain operational amplifier with low noise constraints.

Miss.Rajashri Deshmukh, Dr.M.A.Gaikwad, Prof. D.R.Dandekar
Research scholar,B.D.College of engg sevagram,wardha(M.S)India
Prof. and Dean(R & D),B.D.College of engg. Sevagram,wardha(M.S)India.
P.G. Department of electronics engg.B.D.College of engg sevagram,wardha(M.S)India

Abstract

In this paper the method has been proposed for the design of a high gain CMOS operational amplifier (Op-Amp) with low noise constraints. which operates at 1.8V supply voltage and design has been carried out in ADS tool for tsmc 0.18 micron CMOS technology. The OP-AMP designed is a three-stage CMOS OP AMP with feed-forward compensation method. The proposed feed-forward compensation overcomes the drawback of bandwidth narrowing . It can improve the phase margin as well as optimize the bandwidth of the op amp. The OPAMP is designed to exhibit a high gain of 37 dB, and low noise of 1.2 dB for a wide bandwidth of 3 GHz. The power is observed to be 1.31mW , the unity gain bandwidth is observed to be 6 GHz.

1. Introduction

Operational amplifiers (op amps) are most versatile and integral part of many analog and mixed signal systems. The op amp is a high gain, dc coupled amplifier designed to be used with negative feedback to precisely define a closed loop transfer function. The basic requirements for an op amp are sufficiently large gain , Differential inputs and Frequency characteristics that permit stable operation when negative feedback is applied. Other requirements are High input impedance, Low output impedance, High speed/frequency. They are employed from dc bias applications to high speed amplifiers and filters. General purpose op amps can be used as buffers, summers, Integrators, Differentiators, Comparators, Negative impedance convertors and many other applications. Its performance makes significant impact on the analog systems. Here our requirement is of high gain and to increase the gain of cmos devices the trend is to shrink the gate oxide thickness. Op amp has different topologies such as single stage op amp, cascode op amp, two stage op amp, and three stage op amp. Single stage op amp has limited gain. In two stage op amp first stage is for high gain and second stage provides high swing . whereas three stage op amp achieves higher gain than two stage op amp so multistage amplifiers are widely used in the analog and mixed signal circuits to achieve higher dc gain and large output signal swing simultaneously. Multistage amplifiers are widely used to boost the gain by increasing the number of gain stages horizontally. However all multistage amplifiers suffer from closed loop stability problem due to the presence of multiple poles. Different frequency compensation topologies for multistage amplifiers have been used. They are as Nested miller compensation, Feed-forward compensation, Indirect frequency compensation method. Nested miller compensation (NMC) is a basic well known technique for compensating multistage amplifiers but it suffers from reduced bandwidth when gain stages increases. Some other techniques also have been used recently with some modifications in NMC. Objective of compensation is to achieve stable operation when negative feedback is applied around the op amp. Types of Compensation 1. Miller - Use of a capacitor feeding back around a high-gain, inverting stage. 2. Self compensating - Load capacitor compensates the op amp. 3. Feed-forward - Bypassing a positive gain amplifier resulting in phase lead.

In this paper noise is one of the parameter to which we have to reduce. Noise limits the minimum signal level that a circuit can process with acceptable quality. Amplifier generates random voltage at the output even when there is no signal applied this can be due to thermal noise and flicker noise of the devices for applications with high gain or high bandwidth noise become a very important factor. There are two types of noise device electronic noise and environmental noise. Device electronic devices consist of thermal noise and

flicker noise. There are three primary factors which need to be optimized to minimize the noise level: choice of Input pair type, Bias current of the input pair, Sizes and aspect ratios of the MOSFETs. The choice of the input pair as NMOS or PMOS depends on specific application and the CMOS process used for the design. Mostly NMOS devices are chosen as the input pair. The reason behind selecting NMOS for its lager mobility often 2 to 3 times of that of PMOS results in reduced thermal noise. The NMOS flicker noise coefficient KFn is smaller than that of PMOS which is helpful for achieving lower flicker noise. And NMOS has a higher transition frequency fT than PMOS, which can help to achieve a high bandwidth. The bias current of the input pair must be maximized to reduce both types of noise. This is achieved by choosing a large size and high aspect ratio for the input pair. To reduce the flicker noise, a large size for (W/L) is chosen. There are three different approaches for reducing noise first is the classical approach in which the enlargement of gate area is the classical way of noise reduction. Second is the chopper technique in which the basic idea is to transform the input signal spectrum by a first chopper into a frequency range where the op amp generates less noise then the amplified signal is recovered by second chopper. Third one is the auto zero technique, there are several ways of performing an auto zero op amp which actually depend on the environment in which the op amp operates. Channel length split method is also used to reduce the noise in which the area of transistor (W,L) can be increased to effectively decrease the flick noise. Channel length split method is used to separate the differential input transistor into two transistors in series by using this method we can achieve high stability, high gain, wide swing.

As commonly known, it becomes more difficult to measure the op amp characteristics, especially the open loop gain, as power supply voltages continue to decrease. When the multiplication of input referred noise and the open loop gain of the op amp exceeds the power supply voltage, it is difficult to directly test the open loop gain of the op amp. In addition, if the signal magnitude is smaller than the noise. The open loop gain of op amp determines the precision of the feedback system employing the op amp. The required gain can be adjusted according to the application. Trading with the parameters such as speed and output voltage swing.

2. Design diagram and description

In this paper we have design three stage operational amplifier having high gain, low noise and wide bandwidth is carried out in ADS tool using tsmc 0.18 micron cmos technology. The proposed active feed-forward is used to compensate the multistage operational amplifier with good phase margins as well as drastic improvement of the bandwidth of the amplifier compared to the most widely used pole splitting Miller capacitor compensation approaches. The reference circuit diagram of three stage operational amplifier with feed-forward compensation is taken from [2]. In which a feed-forward compensation technique is used to stabilize the three stage op amp without reducing the bandwidth.

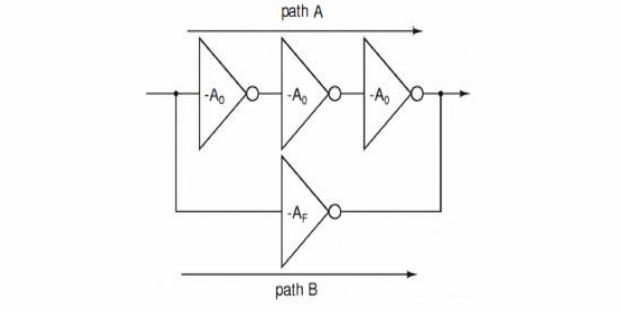


Fig. 1. Block diagram of proposed three stage operational amplifier with feed-forward compensation

Fig. 1 shows the block-diagram of a three stage operational amplifier with feed-forward compensation. In which The three stage cascaded amplifier on path A provides a gain of - (Ao)3 at low frequency, where –Ao is the gain of each cascaded amplifier. At high frequencies, since path B is faster, the amplifier will typically have a gain of only -Af, the gain of the feed-forward amplifier. At the same time, to first order, the gain bandwidth product will be given by Af times the bandwidth of path B. A class AB push pull amplifier (a CMOS inverter) has been used to implement each of the single stage amplifiers. This proposed feed-forward compensation method is fully compatible with the classical general purpose operational amplifier configuration. This architecture also has the advantage of stabilizing the op amp without reducing the bandwidth as much as most commonly used

compensation methods do. Fig. 2 shows the transistor level implementation of the pseudo differential operational amplifier

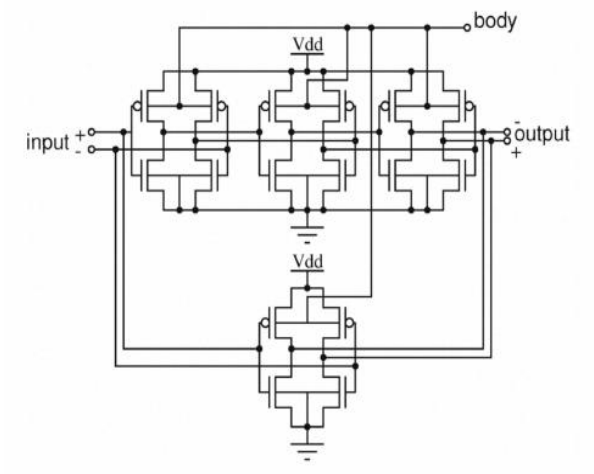
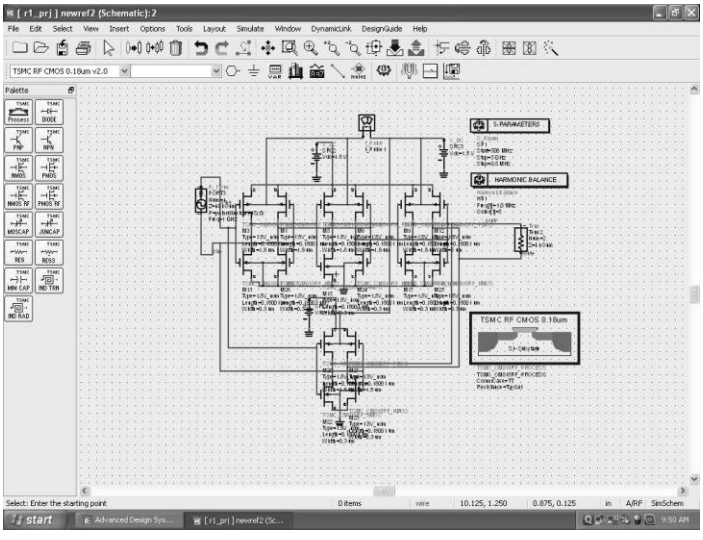


Fig. 2. Transistor level implementation

The feed-forward architecture is much easier to design compared to other schemes. It is very convenient to develop the proposed active feed-forward in the classical three stage operational amplifier with capabilities to drive large capacitive loads. Most existing op amp structures may be easily adapted to apply the proposed feed-forward configuration. The basic concept of feed-forward is to add a signal with less phase shift to the amplified signal, so that the resulting output has an improved phase response. The proposed feed-forward stage does not change the gain from the differential input stage to the output stage. In fact, the feed-forward stage feeds a modified output instead of the exact output voltage back to the inverting input terminal in order to change the closed loop transfer function. The ratio of the altered feedback voltage to the positive input voltage forms the loop gain of the feed-forward compensated op amp.

3. Schematic design



The above schematic shows the three stage op amp using feed- forward compensation method carried out in ADS tool in 180 nm technology. In this we have to do s- parameter simulation for finding the gain and noise parameter. Within the required frequency range and for finding the power we use the transient analysis by which we get the current with the help of I_Probe. And then the product of current and supply voltage vdd= 1.8. gives the power 1.31mw In the proposed design of three stage op amp parameters such as high gain, low noise, wide bandwidth and power are achieved after the simulation. The results after simulation are as follows.

4. Simulation result

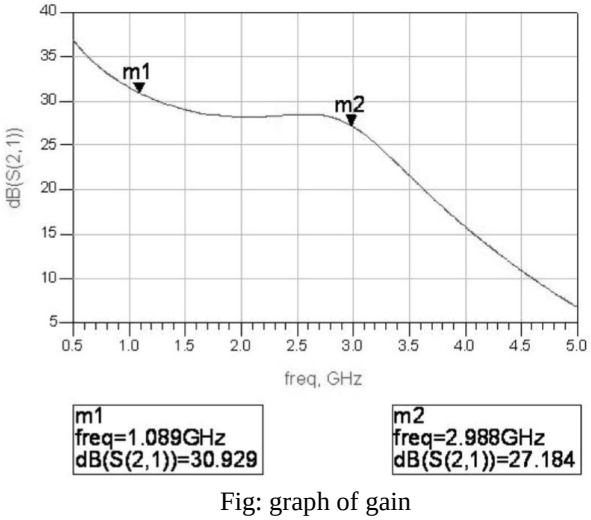


Fig: graph of gain

The above graph of gain shows the peak gain 37 dB. And average gain of 28 dB for frequency band 1 to 3 GHz. So the wide bandwidth is found to be 3GHz.

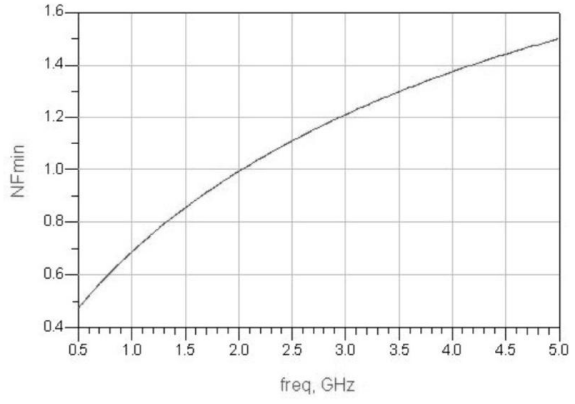


Fig: graph of noise

As the noise graph shows at wide bandwidth 3GHz there is noise of 1.2 dB .which is considered as less noise because it is less than 3 dB.

5. Table. 1

Comparison table :

parameters	[2]	This work
Technology	130nm	180 nm
Supply voltage	1.2 v	1.8 v
Gain	39dB	37dB
Noise	NA	1.2dB
power	18 mW	1.31 mW

6. Conclusion

The technique of a feed-forward compensation method of op amps is introduced and presented in which a feed-forward compensation based pseudo-differential op amp has been implemented by keeping a single stage pseudo-differential amplifier in the feed-forward path in order to achieve high gain without sacrificing the bandwidth. when three stage op amp using feed-forward compensation method is designed and simulated for achieving the parameters high gain a low noise, wide bandwidth and low power consumption. Then it is seen that at low supply voltage of 1.8v, we get high peak gain of 37 dB , and the average gain of 28 dB for frequency range 1GHz to 3GHz. So the wide bandwidth is observed to be 3 GHz. Whereas the gain of reference paper is 39 dB this may differ due the technology and platform change, and noise is found to be 1.2 dB at 3GHz frequency. Whereas noise varies from 0.5dB to 1.5dB for a frequency range of 0.5 GHz to 5 GHz. Which is less than 3 dB so considered as very low noise. The power is found to be 1.31mW where as in reference paper the value of power is 18 mw. So we achieve the low power as compared to the refer paper design. The unity gain bandwidth is 6 GHz.

7. References

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