Design of Four Port Router for Network on Chip

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Abstract: **Network on Chip is a new paradigm to make the interconnections inside a System on Chip (SoC). Bus structures is used to make interconnections in SoC. New technology will not be satisfied by bus structure, as integration surges it becomes narrow and in the worst case it begins to block traffic. NoC is a technology that is intended to solve the short coming of buses. Network in NoC technology replaces the bus structure. Blocks communicate with each other and sends data in the form of packet over this network. NoC network consists of routers, route the data packets and wires connect devices to routers and routers to other routers. Processors, memories and other IP-blocks (Intellectual Property) or processing elements (PE) are connected to routers. The router which is a main component should be properly designed to implement efficient NoC architecture. In this paper we designed and simulated the 1X4 tree topology NoC Router using Verilog HDL and implemented on Spartan3 Xc3s400 FPGA.**

Keywords: SoC, NoC, FPGA, Router.

I INTRODUCTION

SoC consists of computing cores, I/O subsystems, memory controllers, connections between them, and means of switching (buses, crossbars, Network on Chip (NoC) elements). Advancement in the semiconductor technology results in a Multiprocessors System on Chip (MPSoC) which includes multiple microprocessors. Processor bus is the connecting element between these cores. Only one processor block can transfer data at a time is the main drawback. All other cores can only be recipients at that time. Packet-based switching/routing systems is implemented to overcome the drawback of MPSoC. Relationship between the processor blocks is established by routing the data packets is called NoC. The 1 X 4 Router design is implemented by utilizing the FIFO, Register, Synchronizer and FSM.

II LITERATURE SURVEY

In [1] Author proposed the 2D NoC router design and its usage to configure (4 x 4) mesh topology NoC and the XY routing technique used to address the nodes in the NoC. It is one of the simplest techniques for addressing the nodes and route the data packets from one to another nodes or processing elements inside NoC. In the design 16 processing elements or nodes can intercommunicated using their routers in forward packet scheme. The arbiter assigns the priority in case of multi request and round robin scheduling. The developed chip supports 400 MHz frequency, 102468 kB memory and 24 IOs.

In [2] Author proposed an implementation of torus topology NoC using FPGA. Long wire problem in torus topology can be handled by pipelining both the long and short wires and by lengthening the input buffers attached to the long wires. This permits to maintain good performances in the network with a small increase of the resources.

In [3] Author said that the critical path delay of the router is 637us and the area is 2X(4,4) X 103flm2 by doing a logic synthesis based on 5500um CMOS standard-cell library. The maximum data throughput is 703.3 Gbps under the maximum support. Therefore, the lightweight NoC router can meet the need of multi-core NoC system in special field, and it also has a high cost performance.

Communication latency and power has been reduced in [4] in which author proposed a hybrid scheme based on virtual circuit switching.

To enhance the performance of on-chip communication has been enhanced in [5] in which author proposed a Bidirectional channel Network-on-Chip (BiNoC) architecture.

III METHODOLOGY

Fig.1 shows the block diagram of 1 X 4 router. Packet-based protocol is used. Address in the packet drives the incoming packet from input port to output ports in the router. Except reset all signals are active high signals and all are activated to the negative edge of the clock signal and router is sensitive to the positive edge of the signal in order to have sufficient setup and hold time. The basic components of the 1 X 4 router are First In First Out (FIFO) buffer , Finite State Machine (FSM) , Register and Synchronizer.

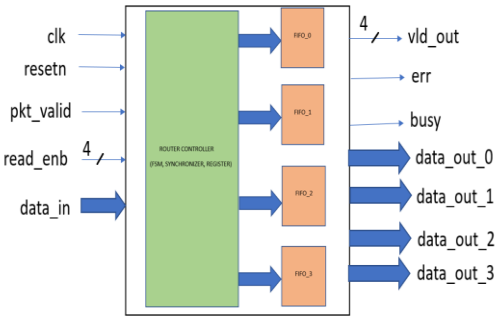

Fig.1 Block diagram of 1 X 4 router

Data packet format is shown in the Fig.2 The three parts of the packet are Header consists of destination address and the length of the payload, payload consists of actual data to be transmitted and parity to check the parity of the data , each having 8-bit width. The payload length can be extended between 1 byte to 63 bytes.

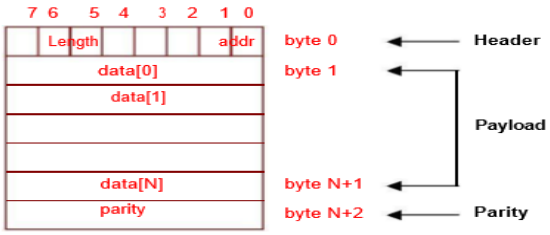

Fig.2 Data Packet Format

FIFO

FIFO is a buffering element used to stores packets before actual transmission to the respective destination node. There are four 16X9 FIFOs used in the router design. The system clock controls the FIFO and a synchronizer reset active low signal which is used to reset the FIFO. Internally FIFO is reset using soft signal_reset. During time out state of the router synchronizer generates active high Soft_reset signal. Logic for FIFO module based on Read and Write signal. Data stored in the FIFO by using write address, whenever it receives write enable signal from synchronizer module. Data is read out from memory location indicated by read address after receiving read enable signal. The two status signals of FIFO are Full and Empty. FIFO is ready to receive data is indicated by the signal Empty while Full indicates there is no space to write data in FIFO.

Register

This module has internal register in which data packet is divided as header, parity and payload. It checks signals from FSM controller and accordingly identifies address of the destination. Example, the incoming data is header is identified by the lfd_state and detect-add high signals. It considers that incoming data is actual payload if it receives ld_state high with input data. It stores data in the internal register if full_state and fifo_full signals are high. It starts sending newly received data to the output if laf_state is high. Register also stores internal parity for parity matching. Header byte is XORed with payload byte and previous parity values to calculate internal parity is shown below:

parity_reg=parity_reg_previos^headr_byte

parity_reg=parity_reg_previos^paylod_byte

Synchronizer

For checking validity of data packets and generating soft reset signal synchronizer module has logic. Based on FIFO condition validity of packet is decided. It will generate Valid_out signal for data transmission when FIFO empty status observed to be high. Soft Reset Logic is designed in Synchronizer. Logic is determined as, module waits for 10 clock cycles for receiving read enable signal from target node after assertion of valid_out signal. Soft reset signal asserted to be high if it does not receive read enable within that period. To internally reset buffer this soft reset signal further used by FIFO modules. Synchronization is main purpose of this module hence full status from all FIFO's are integrated to generates one single FIFO-full signal to inform FSM about full status of FIFO. It also provides write enable signal to FIFO.

FSM

The controller circuit for the router is the FSM module. When new packet is sent to router FSM generates all the control signals. Other modules uses these control signals to send data to the output, writing data into the FIFO. FIFO is empty or not is checked by the FSM. The data is load to FIFO if it is empty, otherwise waits till FIFO becomes empty. Finally, the parity is checked at the output of the router. Correct data packet reception is indicated if the output receives same parity as that of the input. Fig. 3 shows the FSM flow for four port router.

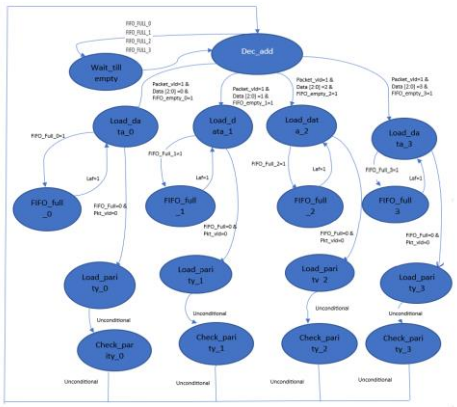

Fig.3 FSM Flow

Fig. 4 shows the RTL schematic of 1X4 router.

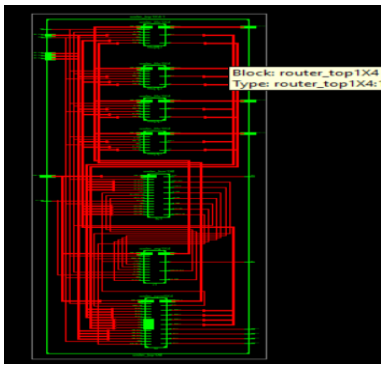

Fig.4 RTL schematic of 1X4 router

IV EXPERIMENTAL RESULTS

The 1X4 router is synthesized and simulated through Verilog code using Xilinx ISE 10.1 and implemented on Spartan3 Xc3s400 FPGA successfully. Fig. 5 shows the simulation waveform of 1X4 router. Fig. 6 shows the Router implementation on Spartan 3 FPGA device

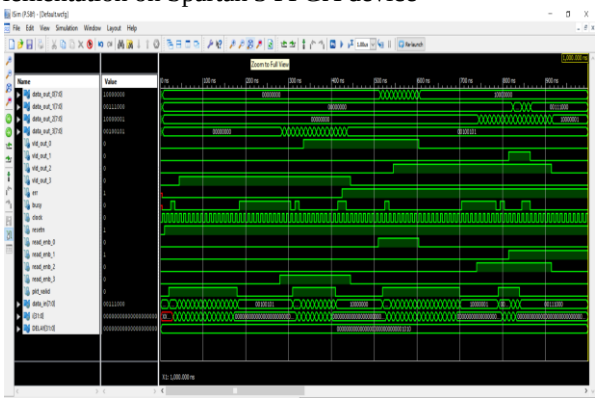

Fig.5 simulation waveform of 1X4 router

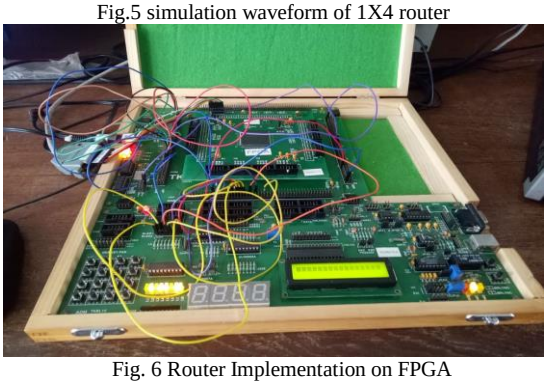

Fig. 6 Router Implementation on FPGA

Device Utilization Summary of 1 X 4 Router

Table 1: Device Utilization Summary of Xilinx ISE 14.5 design suite

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	25	960	2%
Number of Slice Fli Flops	24	1920	1%
Number of 4 input LUTs	59	1920	3%
Number of bonded IOBs	31	66	46%
Number of GCLKs	1	24	4%

Table 2: Device Utilization Summary of Xilinx ISE 10.1 design suite

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	608	3584	16%
Number of Slice Fli Flops	697	7168	9%
Number of 4 input LUTs	633	7168	8%
Number of bonded IOBs	53	141	37%
Number of GCLKs	1	8	12%

Router Device Utilization Summary using Xilinx ISE 14.5 design suite is shown in Table 1 and Device Utilization Summary using Xilinx ISE 10.1 design suite is shown in Table2.

V CONCLUSION

In this paper we have designed and verified the 1 X 4 Router using Verilog and implemented on Spartan 3 FPGA. Future scope is to design a 4 X 4 mesh topology and synthesized using EDA tool.

REFERENCES

[1] Arpit Jain, Rakesh Dwivedi, Adesh Kumar, Sanjeev Sharma "Network on Chip Router for 2D Mesh Design", International Journal of Computer Science and Information Security (IJCSIS), Vol. 14, No. 9, Sept. 2016.

[2] Angelo Kuti Lusala, Philippe Manet, Bertrand Rousseau, Jean-Didier Legat " NoC Implementation in FPGA using Torus Topology", International Conference on Field Programmable Logic and Applications 2007, ISSN: 1946-147X

[3] Yi-Ran Du, Wei LI, Zi-Bin Dai "Lightweight Network-on-Chip Router on Research and Design " , 2016 13th IEEE International Conference on Solid-state and Integrated Circuit Technology (ICSICT), ISBN 978-1-4673-9719-3.

[4] S. Shenbagavalli, S. Karthikeyan "An Efficient Low Power NoC Router Architecture Design", 2015 Online International Conference on Green Engineering and Technologies (IC-GET 2015), ISBN 978-1-4673-9781-0/15.

[5] Ying-Cherng Lan1 Shih-Hsin Lo, Yueh-Chi Lin, Yu-Hen Hu, Sao-Jie Chen1, "BiNoC: A Bidirectional NoC Architecture with Dynamic Self-Reconfigurable Channel", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol.30, Issue: 3 , March 2011 ,ISSN-0278-0070, pp 427 – 440.

[6] U. Saravanakumar, R. Rangarajan and K. Rajasekar "Hardware Implementation of Pipeline Based Router Design for On chip Network", ICTACT Journal on Communication Technology Dec. 2012, Vol. 03, Issue: 04, ISSN: 2229-6948, pp 646- 650.

[7] Qi Chen and Qiang Liu "Pipelined NoC Router Architecture Design with Buffer Configuration Exploration on FPGA", School of Electronic Information Engineering Tianjin University, China, **2015** 25th International Conference on Field Programmable Logic and Applications (FPL), ISBN 978-0-9934-2800-5/15.

[8] P. Veda Bhanu, S. Jagadeesh, Vasanth Bhat, Garima Agarwal, and Soumya J "FPGA Implementation of Novel Routing Algorithm for Butterfly-Fat-Tree Topology based NoC Design", 2019 15th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), ISBN:978-1-7281-3549-6.

[9] S. Kumar, A. Jantsch, J. Soininen, M. Forsell, M. Millberg, J. Oberg, K. Tiensyrja, and A. Hemani, "A network on chip architecture and design methodology", Proceedings IEEE Computer Society Annual Symposium on VLSI. New Paradigms for VLSI Systems Design. ISVLSI 2002, April 2002, pp. 117–124.

[10] Ivan MIRO PANADES STMicroelectronics, Alain GREINER The University of Pierre and Marie Curie, "Bi-Synchronous FIFO for Synchronous Circuit Communication Well Suited for Network-on-Chip in GALS Architectures", First International Symposium on Networks-on-Chip (NOCS'07), ISBN 0-7695-2773-6/07.

[11] Zhen Zhang, Alain Greiner, Sami Taktak "A Reconfigurable Routing Algorithm for a Fault-Tolerant 2D-Mesh Network-on-Chip ",2008 45th ACM/IEEE Design Automation Conference, ISBN 978-1-60558-115-6/08, ISSN 0738-100X.

[12] Mohammad Ayoub Khan , Jamia Millia Islamia, " n-Bit Multiple Read and Write FIFO Memory Model for Network on Chip", 2011 World Congress on Information and Communication Technologies , ISBN 978-1-4673-0126-8/11.

[13] Yilian Ribot, Geoffrey Nelissen "Design and implementation of an FPGA-based NoC for Real Time Systems", 31st Conference on Real-Time Systems, 2019 - cister-labs.

[14] Jakub Siast, Adam Łuczak, Marek Domański, "RingNet: A Memory-Oriented Network-on-Chip Designed for FPGA" IEEE Transactions on Very Large Scale Integration (VLSI) Systems , Volume: 27 , Issue: 6 , June 2019.

[15] Sharma, V. V. Joshi, V. M. Rohokale, "Performance of Router Design for Network on Chip [mplementation", [nternational Conference on Communication, Information & Computing Technology (lCCICT), Oct. 19-20, Mumbai, India 2012.