Design of efficient low power CMOS full-adder for high-performance digital systems & arithmetic applications

S.Solairaj
M.E Communication Systems
Dept.,of ECE
Shivani Engineering college,
Trichy, Tamil Nadu, India
solairaj.24@gmail.com

S.D.Sundar
M.E Applied Electronics
Dept.,of ECE
Paavai Group of Institutions ,
Namakkal, Tamil Nadu, India
09738449631

ABSTRACT: In this paper, a new two high-speed and low-power full-adder cells designed and implemented in RCA (ripple carry adder) with an alternative internal logic structure and pass-transistor logic styles that lead to have a reduced power-delay product (PDP). We carried out a comparison against other full-adders reported as having power consumption and area. All the full-adders were designed with a 0.18µm CMOS technology; Simulation results illustrate the superiority of the resulting proposed adder against conventional CMOS full-adder in terms of power, delay and PDP. The proposed full-adders outperform its counter parts exhibiting an average PDP advantage of 75%, with only 40% of relative area.

Key Terms: RCA (ripple carry adder) Arithmetic, full-adder, PDP, high-speed & low-power.

I. INTRODUCTION

In most VLSI applications, arithmetic operations play an important role. Commonly used operations are addition, subtraction, multiplication and accumulation, the Full Adder (FA) cell is the building block for most Implementations of these operations. Energy-efficiency is one of the most required features for modern electronic systems designed for high-performance and/or portable applications. In one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. On the other hand, the general trend of increasing operating frequencies and circuit complexity, in order to cope with the throughput needed in modern high-performance processing applications, requires the design of very high-speed circuits. The power-delay product (PDP) relates the amount of energy spent during the realization of a determined task, and stands as the more fair performance metric when comparing optimizations of a module designed and tested using different technologies, operating frequencies, and scenarios. Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) architectures and microprocessors. This module is the core of many arithmetic operations such as addition/subtraction, multiplication, division and address generation. As stated above, the PDP exhibited by the full-adder would affect the system's overall performance [1]. Thus, taking this fact into consideration, the design of a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital systems. In this paper, we report the design and performance comparison of two full-adder cells implemented with an alternative internal logic structure, based on the multiplexing of the Boolean functions XOR/ XNOR and AND/OR, to obtain balanced delays in SUM and CARRY outputs, respectively, and pass-transistor powerless/groundless logic styles, in order to reduce power consumption. The resultant full-adders show to be more efficient on regards of power consumption and delay when compared with other ones reported previously as good candidates to build low-power arithmetic modules.

The rest of this paper is organized as follows: Section II presents details the existing techniques Section III describes the proposed method in detail. Section IV explains the The effectiveness of the method is the comparison carried out to obtain the power and speed performance of the full-adders. Section V reviews the results obtained from the simulations, and VI concludes this work.

II. EXISTING FULL-ADDER BLOCK

The internal logic structure shown in Fig. 1 has been adopted as the standard configuration in most of the enhancements developed for the 1-bit conventional structure of full-adder module.

In this configuration, the adder module is formed by three main logical blocks: a XOR-XNOR gate to obtain *(A xor B)* and *(A xnor B*) (Block 1), and XOR blocks or multiplexers to obtain the *SUM (So)* and *CARRY (Co*) outputs is (Blocks 2 & 3).

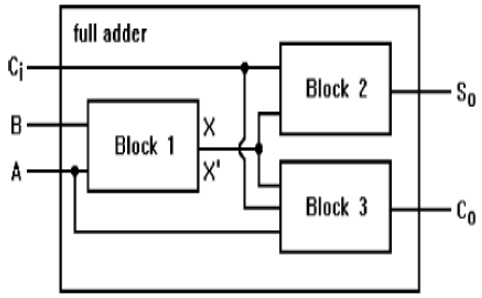

Fig.1 Conventional design of Previous Full adder logic cell blocks

$Sum = X \text{ xor } C_{in}$
$C_{out} = A.X' + C_{in}.X$

Where , X = A xor B
X' = A xnor B

An important conclusion was pointed out in that work: the major problem regarding the propagation delay for a full-adder built with the logic structure shown in Fig. 1, is that it is necessary to obtain an intermediate signal (A xor B) and its complement, which are then used to drive other blocks to generate the final outputs.

A. Standard CMOS-CPL logic style

The standard CMOS-complementary pass logic full adder design is the most conventional method. Several alternates of static CMOS logic styles have been used to implement low-power 1-bit adder cells [2, 4-6]. In general, they can be largely divided into two major categories: The complementary CMOS and the pass-transistor logic circuits. The complementary CMOS full adder (C-CMOS) of Fig. 1(a) is based on the CMOS structure with PMOS pull-up and NMOS pull-down transistors. The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing, which are essential to provide reliable operation at low voltage and arbitrary transistor sizes [12]. In this method the propagation delay in the XOR/XNOR block has been slightly increased due to this fact the overall delay and the power consumption also increased.

So, Thus, the overall propagation delay and, in most of the cases, the power consumption of the full-adder depend on the delay and voltage swing of the (A xor B) signal and its complement generated within the cell. So to increase the operational speed of the full-adder, it is necessary to develop a new logic structure that does not require the generation of intermediate signals to control the selection or transmission of other signals located on the critical path.

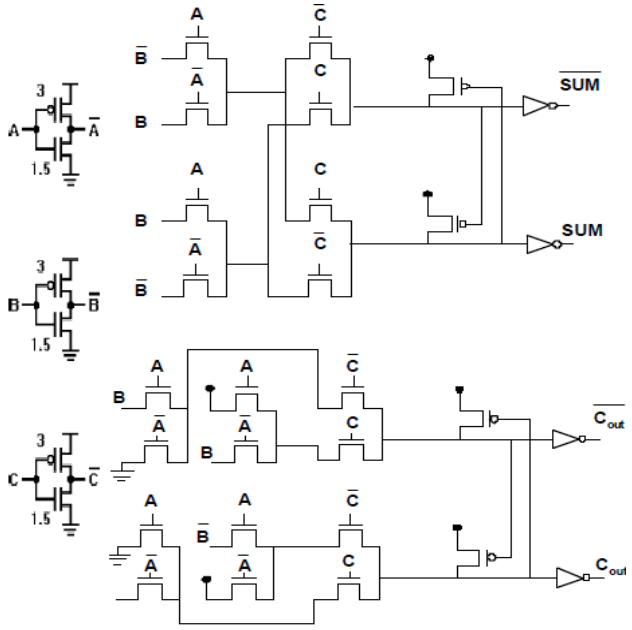

Fig.1(a).Standard existing CMOS-CPL Full adder design

PROPOSED LOGIC STRUCTURE FOR A FULL-ADDER

In this category, the Sum and Carry outputs are generated by the proposed full adder and the general form of this category is shown in Fig.2

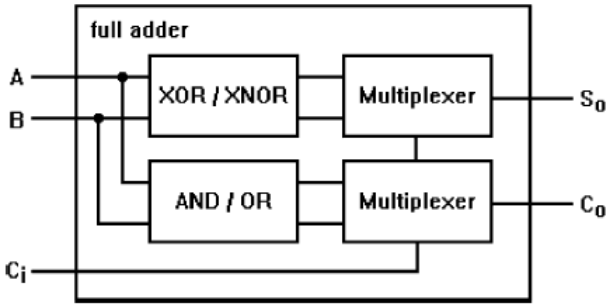

Fig.2 Proposed Logic Scheme for Designig Full Adder cells

Following the same criteria, the *Co* output is equal to the *A xor B* value when *Co=0* , and it is equal to value *(A xnor B)* when *Co*=1. Again, *Co* can be used to select the respective value for the required condition, driving a multiplexer. The Sum and Carry outputs are generated by the following expression.

Sum = (A xor B) Ci+ (A xnor B) Ci'
Cout = (A and B)Ci+(A or B) Ci'

The proposed structure implemented in RCA (ripple carry adder) application and the structure is shown in figure.3 true-table for a 1-bit full-adder: a, b, and c are inputs;so and co are outputs

C	B	A	SO	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

-

Table I- true-table for a 1-bit full-adder

Hence, an alternative logic scheme to design a full-adder cell can be formed by alogic block to obtain the (*A xor B)* and *(A xnor B*) signals, another block to obtain *(A and B*) and *(A or B*) signals, and two multiplexers being driven by the *C* input to generate the *So* and *Co* outputs, as shown in Fig. 2 [13].

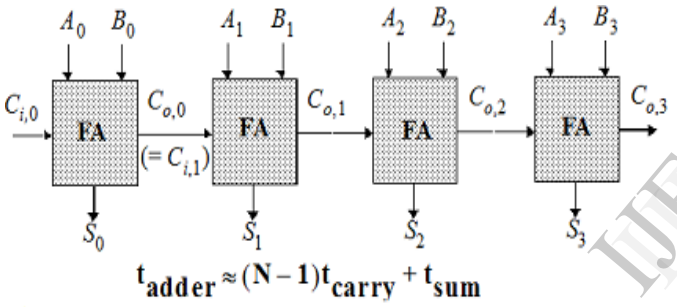

Fig.3.Implimentation of proposed full adder in RCA

The features and advantages of this logic structure are as follows.

• There are not signals generated internally that control the selection of the output multiplexers. Instead, the *C* input signal, exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reducing so the overall propagation delays.

• The capacitive load for the *C* input has been reduced, as it is connected only to some transistor gates and no longer to some drain or source terminals, where the diffusion capacitance is becoming very large for sub-micrometer technologies. Thus, the overall delay for larger modules where the *C* signal falls on the critical path can be reduced.

• The propagation delay for the *So* and *Co* outputs can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates; this feature is advantageous for applications where the skew between arriving signals is critical for a proper operation (e.g., wave pipelining), and for having well balanced propagation delays at the outputs to reduce the chance of glitches in cascaded applications.

• The inclusion of buffers at the full-adder outputs can be implemented by interchanging the XOR/XNOR signals, and the AND/OR gates to NAND/NOR gates at the input of the multiplexers, improving in this way the performance for load-sensitive applications.

Based on the results obtained in [3], two new full-adders have been designed using the logic styles DPL and SR-CPL, and the new logic structure presented in Fig. 2. Fig. 3 presents a full-adder designed using a DPL logic style to build the XOR/XNOR gates, and a pass-transistor based multiplexer to obtain the *So* output. In Fig. 4, the SR-CPL logic style was used to build these XOR/XNOR gates. In both cases, the AND/OR gates have been built using a powerless and groundless pass-transistor configuration, respectively, and a pass-transistor based multiplexer to get the *Co* output.

B. SIMULATION ENVIRONMENT

Fig. 5 shows the test bed used for the performance analysis of the full-adders. This simulation environment has been used for comparing the full-adders analyzed in [9], [14], with the addition of the inverters Fig. 3. Full-adder designed with the proposed logic structure and a DPL logic style (Ours1).Fig. 4. Full-adder designed with the proposed logic structure and a SR-CPL logic style (Ours2).

DPL logic style

In this style of logic full adder design has three section of design. First the inverter logic is designed using CMOS (complementary MOS) technology. Second the XOR/XNOR gate is designed with the XOR/XNOR output expression (i.e. *A□□B=A.B'+A'.B)*. The last section is based on multiplexer operation with TG (transmission gate).The third input carry bit *C* will be act as a carry selector line in the sum circuitry. In carry circuit also has designed with same pass transistor logic. This type of double transistor logic designed with minimum number of MOS transistor, therefore the power consumption and the gate fan-in &fan-out has reduced when compared with the existing system design.

SR-CPL logic style

Swing restored complementary pass-transistor logic (SR-CPL) is the second method of design of full adder circuit. It has reduced gate transistor to improve the system power requirment. The figure shows that the design of SR-CPL.In this design the sum circuit in the previous CPL circuit is modified with swing restored CPL which provide both XOR/XNOR operation in the same module.

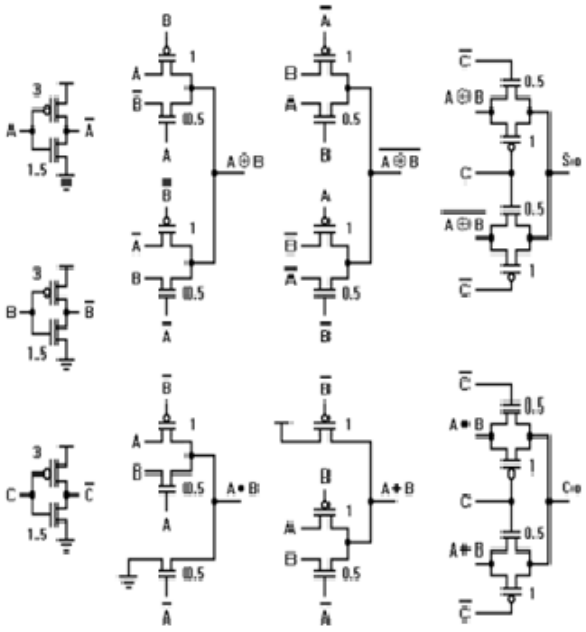

Fig. 3. Full-adder designed with the proposed logic structure and a DPL logic style (Ours1).

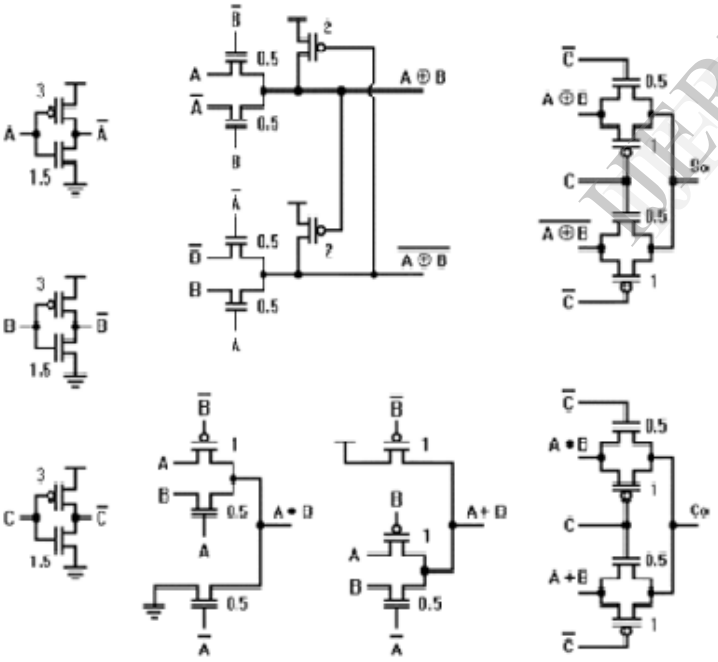

Fig. 4. Full-adder designed with the proposed logic structure and a SR-CPL logic style (Ours2).

In both cases, the AND/OR gates have been built using a powerless and groundless pass-transistor configuration, respectively, and a pass-transistor based multiplexer to get the *Co* output. In the last section of the design is same as the design which has used in the DPL logic design style.

C. SIMULATION RESULTS

Some of the main advantages of proposed method over standard CMOS design are 1) high speed, due to the small node capacitances; 2) low power dissipation, as a result of the reduced number of transistors; and 3) lower interconnection effects [7], [8], due to a small area. We compared the performance of 7 full-adders, named: CPL/Hybrid [10], Ours1 and Ours2. Simulations were carried out using Xilinx tool [6] to determine the power consumption features of the designed full-adders, and Hspice [8] to measure the propagation delay for the output signals.

SCHEME	AREA COUNT	POWER (mW)	PDP %
CPL/hybrid	607	176	41.3
RCA-APPLICATION	4961	163	41.3
DPL	488	139	16.9
RCA-APPLICATION	3883	143	16.9
SR-CPL	383	121	15.8
RCA-APPLICATION	3043	102	15.8

Table II. Simulation results for full-adders performance comparison.

Table II shows the simulation results for full-adders performance comparison for different methods in the ripple carry adder, regarding power consumption, propagation delay, and PDP. All the full-adders were supplied with 1.8 V and the maximum frequency for the inputs was 200 MHz .It is worth to observe that in some cases, the power consumed from the power-supply (pwr supply) for the full-adder is smaller than the total average power (avg power). This is because of, for some logic styles (e.g., pass-transistor style). From the results in Table II, we can state the following.

With regards of the speed, it can be seen the advantage of the logic structure introduced here,

• Only two full-adders exhibit static-dissipation which are implemented with logic styles that have an incomplete voltage swing in some internal nodes, causing this consumption component.
• The power consumption improvements of the full-adders of our proposals show savings up to 60%, and considering the consumption of the standalone full-adder the savings are up to 80%. These savings can be justified by the joint reduction of dynamic and short-circuit power components.
• The short-circuit consumption optimization is related to the powerless/groundless configuration of the constituent

AND/OR gates, and the dynamic consumption optimization comes from the fact of reduced capacitances in the internal nodes for pass-transistor logic styles, and for the well balanced propagation delays inside the full-adder, which results in less glitches at the outputs.

• since both realizations designed using this scheme (Ours1 and Ours2) exhibit the smallest propagation delay, only matched by the CPL full-adder. It shows a propagation delay improvement around 25% compared with the other full-adders.

• The power-delay product (PDP) column confirms the energy-efficiency for the full-adders built using the new internal logic structure. They present the lowest PDP metric, up to 85%of saving, due to the combined reduction of power consumption and propagation delay.

• On regards of the implementation area obtained from the layouts, it can be seen that the proposed full-adders require the smallest area (up to 40% of relative area), which can also be considered as one of the factors for presenting lower delay and power consumption.

Finally, we determined the maximum frequency that each full adder can operate, while being supplied with 1.8 V. The proposed full-adders reach up to 1.25 GHz, only surpassed by cpl cell, at the expense of major power consumption and area.

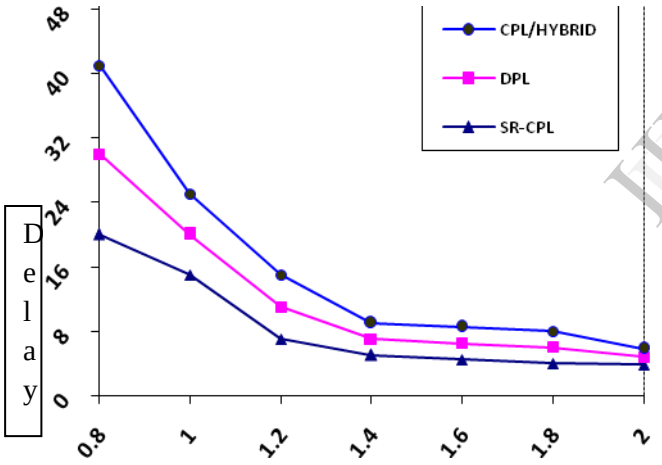

Fig.5 voltage Vs delay performance of different style.

III. Conclusion

An alternative internal logic structure for designing full-adder cells was introduced. In order to demonstrate its advantages, two full-adders were built in combination with pass-transistor powerless/groundless logic styles. They were designed with a TSMC 0.18-µm CMOS technology, and were simulated and compared against other energy-efficient full-adders reported recently. Hspice and Nanosim simulations showed power savings up to 80%, and speed improvements up to 25%, for a joint optimization of 85% for the PDP. The area utilization for the proposed full-adders is only 40% of the largest full-adder compared. All new full-adder cells are shown to have low-energy consumption as compared to several standard full-adder cells therefore are suitable for low energy and low voltage operation.

Rerefence

[1] H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power 10-transistor full adders using XORXNOR Gates," *IEEE Trans. On Circuits and Systems II*, Vol. 49, no. 1, pp. 25-30, Jan 2002.

[2] R. Zimmermann and W. Fichtner, "Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic," *IEEE Journal of Solid-State Circuits*, Vol 32. no. 7, July 1997.

[3] N. Zhuang and H. Wu, "A new design of the CMOS full adder," *IEEE J. of Solid-State Circ.*,vol. 27,pp.840- 844,May 92.

[4] N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design, A System Perspective*. Reading, M.A: Addison-Wesley, 1993.

[5] E. Abu-Shama and M. Bayoumi, "A new cell for low power adders," *Procdings of the International Symposium on Circuits and Systems*, 1996, Vol. 4, pp. 49-52.

[6] A.M. Shams, T. K. Darwish, M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 10, Issue: 1, Feb. 2002, pp.20 – 29.

[7] D. Radhakrishnan, "Low-voltage Low-power CMOS Full Adder," *IEE Procd. of Circ. Dev. Sys.*,vol. 148,no.1, Feb. 2001

[8] K. Yano, K. Yano, T. Yamanaka, T. Nishida, M. Saito, K. Shimohigashi,and A. Shimizu, "A 3.8 ns CMOS 16□16-b multiplier using complementary pass-transistor logic," *IEEE J. Solid-State Circuits*, vol.25, no. 2, pp. 388–395, Apr. 1990.

[9] M. Suzuki, M. Suzuki, N. Ohkubo, T. Shinbo, T. Yamanaka, A.Shimizu, K. Sasaki, and Y. Nakagome, "A 1.5 ns 32-b CMOS ALU in double pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 28,no. 11, , Nov. 1993.

[10] M. Zhang, J. Gu, and C. H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," in *Proc. IEEE Int. Symp.Circuits Syst.*, May 2003, pp. 317–320.