Design of Digital Section of Pipeline Analog to Digital Converter

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Abstract

This paper proposes a methodology for designing digital section of Pipeline Analog to Digital Converter using VHDL-based behavioural descriptions. This paper analyzes 8-bit, 10-bit, 16-bit Pipeline ADC's for their conversion speed and size in terms of gate count. The work also proposes an architecture for designing controller for selection of 8/10/16 bit resolution. The controller design reduces IOBS and gate count. High speed ADC's are always key components for high resolution devices. There is always a variable demand from customer for device speed, accuracy and power consumption. In ADC, accuracy of device depends on resolution of a system. The Work proposed here shows design of digital section for 8 bit, 10 bit, 16 bit Pipeline ADC and its control unit.

Keywords - Accuracy, Pipeline ADC, Resolution, ,Sample and Hold etc.

1. Introduction

An analog-to-digital converter (abbreviated ADC, A/D) is a device that uses sample (analog) to convert a continuous signal to digital form. Fig.1 represents the basic block diagram of ADC. This paper mainly focuses on Digital encoding section of Pipeline ADC. Pipeline ADC can be algorithmic or iterative, N-Bit algorithmic pipeline ADC contains N stages and N comparators for N bit output. It takes input multiply by two and add/subtract the reference voltage based on sign of previous output.
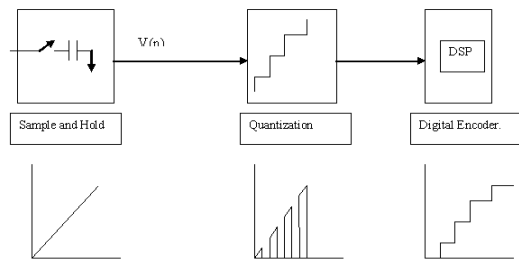

Fig -1 ADC block diagram [1]

Fig.2 represents the basic block diagram for Pipeline ADC. Pipeline algorithmic ADC has disadvantage that it takes N clock cycles for each sample hence iterative Pipelined ADC is the solution which use sample and hold circuit to hold the previous stage and sample before conversion.[1,2]
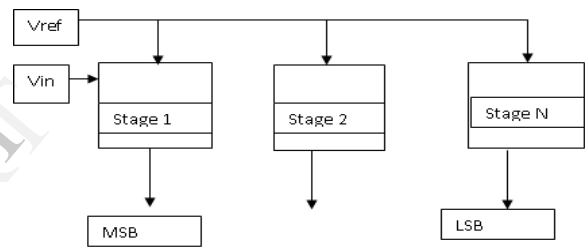

Fig-2. Pipeline ADC architecture. [1]

2. PIPELINE ADC DIGITAL SECTION ARCHITECTURE

The proposed architecture of pipeline ADC's digital section is shown in Fig.3. Output of each stage is stored using shift register at every clock cycle. As each stage is followed by sample and hold circuit, at next clock, result of next stage will be shifted and at same time next sample result is stored. For 8 bit ADC, digital output correspond to first sample is made available after 8 cycles while at 9th clock cycle second sample result is made available, and so on.
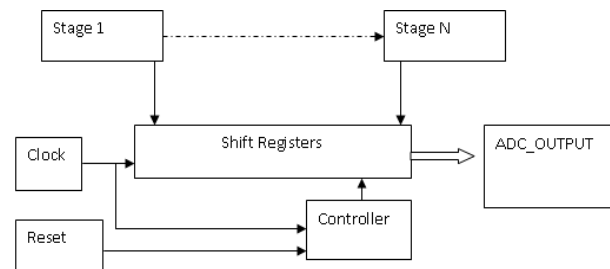

Fig -3 Digital Section of Pipeline ADC.

Controller block will generate signal 'done' when digital output for first sample is available. Similar

architecture is designed for 10 bit and 16 bit Pipeline ADC. N represents 8/10/16.

3. PIPELINE ADC DIGITAL SECTION SIMULATION RESULTS

Fig.4 represents the Spartan device summary report. [10, 14]. Fig.4 represents the synthesis result for digital decoder logic for 8 bit Pipeline ADC. Device xa3s1600e-4fgg400 summary contains detail on numbers of IOBS used are 26 out of 304 hence 8% utilization of existing IOBS on device also represents the device utilization in terms of flip-flop or LUT (look up table) . It shows total logic available on device, used and percentage for utilization also equivalent gate count. In this design 16bit input and 8 bit output is used hence device summary includes 26 IOBS out of 304 hence compared with 10 bit it will be more.

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note
Number of Slice Flip Flops	9	29,504	1%	
Number of 4 input LUTs	21	29,504	1%	
Logic Distribution				
Number of occupied Slices	15	14,752	1%	
Number of Slices containing only related logic	15	15	100%	
Number of Slices containing unrelated logic	0	15	0%	
Total Number of 4 input LUTs	21	29,504	1%	
Number of bonded IOBs	26	304	8%	
IOB Latches	16			
Number of GCLKs	1	24	4%	
Total equivalent gate count for design	281			
Additional JTAG gate count for IOBs	1,248			

Fig-4. 8 bit Pipeline ADC summery.

Fig.5. represents 8 bit Pipeline ADC simulation result for 8 bit Pipeline ADC. Signal msb_lsb is driven from testbench which is sequentially passed to each stage; each stage result is stored in different registers for 8 bit 8 registers are required. Signal done indicate the correct ADC output is available.
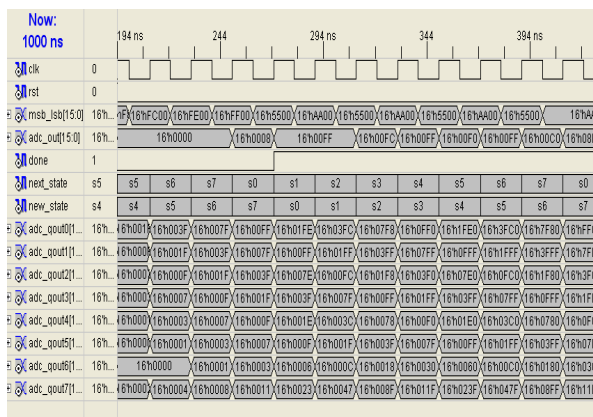

Fig-5. 8 bit Pipeline ADC Simulation.

Fig.6 represents 10 bit Pipeline ADC simulation result for 10 bit Pipeline ADC. Signal msb_lsb is driven from testbench which is sequentially passed to

each stage, each stage result is stored in different registers for 10 bit ,10 registers are required. Signal done indicate the correct ADC output is available.
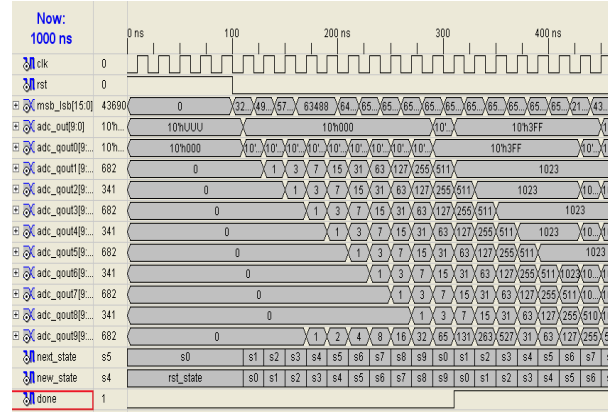

Fig-6. 10 bit Pipeline ADC Simulation.

Fig.7 represents the Spartan device summary report. Fig.7 represents the synthesis result for digital decoder logic for 10 bit Pipeline. Device xa3s1600e-4fgg400 summary contains detail on numbers of IOBS used are 22 out of 304 hence 7% utilization of existing IOBS on device also represents the device utilization in terms of flip-flop or LUT (look up table) . It shows total logic available on device ,used and percentage for utilization also equivalent gate count. In this design 10bit input and 10 bit output is used hence device summary includes 22 IOBS out of 304 hence compared with 8 bit it will be less.

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	11	29,504	1%
Number of 4 input LUTs	75	29,504	1%
Logic Distribution			
Number of occupied Slices	44	14,752	1%
Number of Slices containing only related logic	44	44	100%
Number of Slices containing unrelated logic	0	44	0%
Total Number of 4 input LUTs	75	29,504	1%
Number of bonded IOBs	22	304	7%
IOB Latches	10		
Number of GCLKs	1	24	4%
Total equivalent gate count for design	591		
Additional JTAG gate count for IOBs	1,056		

Fig-7. 10 bit Pipeline ADC summery.

Fig-8. represents 16 bit Pipeline ADC simulation result for 16 bit Pipeline ADC. Signal msb_lsb is driven from testbench which is sequentially passed to each stage, each stage result is stored in different registers for 16 bit, 16 registers are required. Signal done indicate the correct ADC output is available.
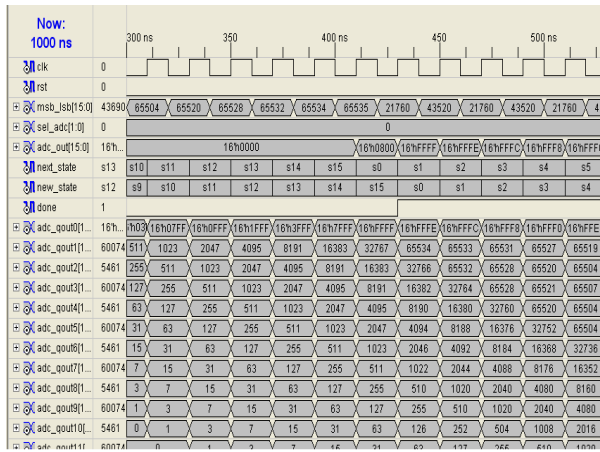
Fig-8. 16 bit Pipeline ADC simulation results.

Fig.9 represents the Spartan device summary report. Fig.9 represents the synthesis result for digital decoder logic for 16 bit Pipeline. Device xa3s1600e-4fgg400 summary contains detail on numbers of IOBS used are 34 out of 304 hence 11% utilization of existing IOBS on device also represents the device utilization in terms of flip-flop or LUT (look up table) .

Fig-9.16 bit Pipeline ADC device Summary.

Table 1 represents gate count, IOBs and conversion cycle for 8bit, 10 bit, 12bit, 16bit resolution respectively.

Table.1 Performance Parameter for Pipeliine ADC

	8 bit	10 bit	12 bit	16 bit
Gate Count	281	591	779	1347
IOBs	26/8%	22/7%	26/7%	34/11%
Conversion time	8 Cycle	10 Cycle	12 Cycle	16 Cycle

Fig.10 represents the trade off graphs for resolution vs conversion time, Conversion cycles increases with increase in resolution. For first sample it will take N cycles in next cycle it will give next sample output hence latency for first sample is N cycles. First sample residue signal sampled thro N stages while next sample is preceded. It takes N cycles thro N stage for first sample while second will proceed on N+1 the cycle.
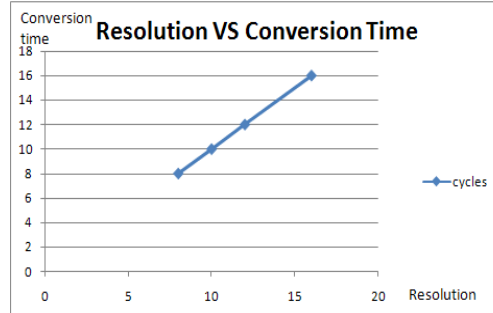

Fig-10 Resolution vs Conversion Time graph.

Fig.11 is trade off graph for resolution vs size in terms of gate count. Gate count increase with increase in resolution.
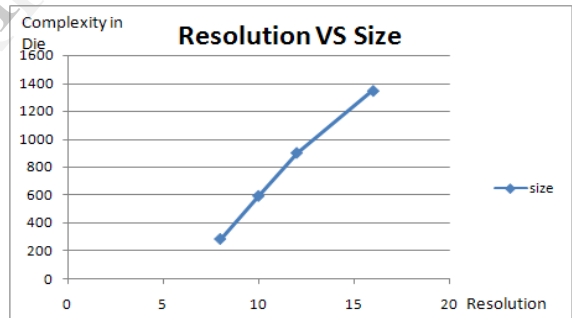

Fig-11 Resolution vs Size graph(In terms of gate count)

4.   CONTROLLER LOGIC DESIGN FOR ADC

Fig.12 represents RTL for the control logic to select the particular resolution of Pipeline ADC digital section from 3 different resolution and output the specific ADC result. VHDL is used to design and Xilinx tool is used to simulate the design.[7,8]

Role of Controller is to select ADC resolution and output respective ADC results. In this controller it select one of 8bit ,10 bit ,16 bit Pipeline ADC digital section .All module level component for 8 bit Pipeline ,10 bit Pipeline and 16 bit Pipeline ADC are used in hierarchy.

ADC_sel (1:0) decide which ADC resolution type ADC to be selected , 00-8 bit , 01 –10 bit and 10 or 11 is 16 bit Pipeline ADC is selected . Based on

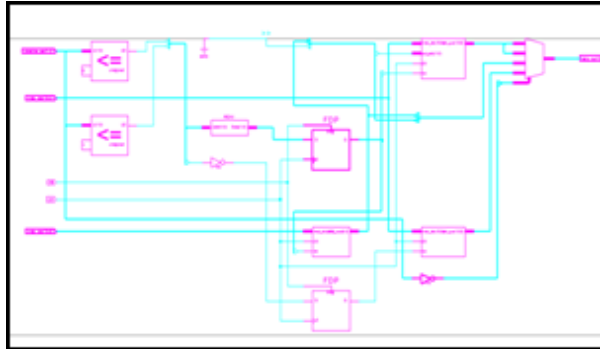ADC_selection bits ADC_out result represents the selected ADC output.

Fig-12 ADC Controller RTL

Fig.13 represents Pipeline ADC controller simulation result for 8/16 bit Pipeline ADC selection. Signal msb_lsb is driven from testbench which is sequentially passed to each stage. adc_out represents the selected ADC output. Pipeline_sel [1:0] is used to select 8bit,10bit,16 bit pipeline ADC. There is 1 more clock cycle delay for selection of ADC.
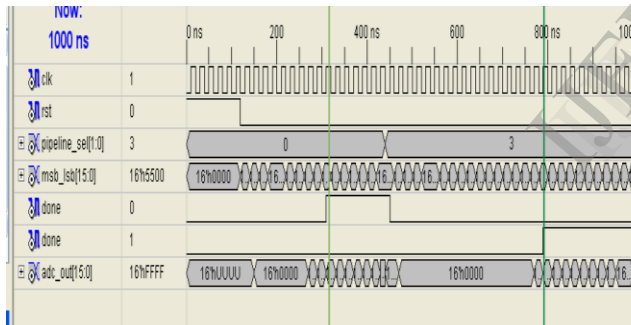

Fig-13 Pipeline ADC Controller Simulation Results

Fig.14 represents device summary for Pipeline Controller.Device xa3s1600e-4fgg400 summary contains detail on numbers of IOBS used are 36 out of 304 hence 11% utilization of existing IOBS on device also represents the device utilization in terms of flip-flop or LUT (look up table) .

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Total Number Slice Registers	43	29,504	1%
Number used as Flip Flops	40		
Number used as Latches	3		
Number of 4 input LUTs	290	29,504	1%
Logic Distribution			
Number of occupied Slices	166	14,752	1%
Number of Slices containing only related logic	166	166	100%
Number of Slices containing unrelated logic	0	166	0%
Total Number 4 input LUTs	292	29,504	1%
Number used as logic	290		
Number used as a route-thru	2		
Number of bonded IOBs	36	304	11%
Number of GCLKs	1	24	4%
Total equivalent gate count for design	2,087		
Additional JTAG gate count for IOBs	1,728		

Fig-14 ADC Controller Summary

CONCLUSION

Performance evaluation has been done based on resolution, word conversion time in terms of conversion cycle, size in terms of gate count . Accuracy increase with increase in resolution and increase in resolution it shows increase the number of gate count. From device summary if 8 bit, 10 bit, 16 bit overall gate count is 2119. While controller is used to choose of 8bit ,10 bit or 16 bit it has reduced gate count of 2087. Also overall number of IOB's are reduced by 46 in pipeline controller.

Acknowledgements

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