Design of Compressors for Multiplication

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***Abstract*— Current mode signaling scheme with dynamic overdriving is one of the most promising scheme for high speed low power communication over long on-chip interconnects. They are sensitive to parameter variations due to reduced voltage swing on the line. The proposed current mode signaling scheme and a competing Current mode signaling Bias scheme are fabricated in 180nm CMOS technology. Measurement results show that the power will be reduced in the proposed scheme when compared with the current mode signaling bias scheme. In proposed scheme we use D-latch as a Delay element. By using D-latch as a delay element throughput will be increased that depends on the latency. In our proposed scheme we can also reduce the area by combining the Vbn, Vbp bias circuits.**

Keywords—CMOS technology; CMS scheme, weak driver; strong driver.

I. INTRODUCTION

On-chip communication is getting more attention, as global interconnects are rapidly becoming a speed, power and reliability bottleneck for digital CMOS systems. While gate speed increases under scaling, smaller cross-sectional wire dimensions will decrease the interconnect bandwidth for a given length. In the deep-submicron era, interconnect wires (and the associated driver and receiver circuits) are responsible for an ever increasing fraction of the energy consumption of an integrated circuit. Most of this increase is due to global wires, such as busses, clock, and timing signals. For gate array and cell-library- based designs, found that the power consumption of wires and clock signals can be up to 40% and 50% of the total on-chip power consumption, respectively. The impact of interconnect is even more significant for reconfigurable circuits. Measured over a wide range of applications, more than 90% of the power dissipation of traditional FPGA devices have been reported to be due to the interconnects.

Speed and power consumption of on-chip interconnect network have become important in advanced CMOS technologies. It is difficult to meet desired power and performance specifications of modern system-on-chips (SoCs) and multicore processors. Many alternate repeater circuits and signaling schemes have been suggested in recent past to achieve high-speed low-power communication over long on-chip interconnects. In modern CMOS technologies, process variations cause significant variations in device parameters which can lead to performance degradation of these signaling techniques. Hence, a signaling scheme for on-chip interconnects is also required to be robust against parameter variations. Current-mode signaling (CMS) scheme has the potential to improve both speed and dynamic power consumption. It consumes much less power compared to the improved repeater circuits.

The huge reduction in energy consumption offered by the low-swing signaling schemes and the CMS schemes is mainly due to the reduced voltage-swing on the line. However, low voltage swing on the line reduces the noise margin of the data communication system. Hence, CMS schemes are more susceptible to parameter variations than the voltage-mode repeater insertion scheme. In highly scaled technologies, process variations cause significant variations in device parameters. The variations in the transistor parameters can be categorized as either inter-die variations or intra-die parameters. In the case of inter-die variations similar devices on a chip have identical electrical parameters but the device parameters vary from die to die, wafer to wafer and batch to batch. In modern technologies, variations in the parameters of devices on the same chip are also significant. This class of variations is referred to as intra-die variations. The variations can cause the voltage swing on the line to change which can lead to significant changes in the performance of a scheme.

Existing system

This scheme uses feedback at both the transmitter and the receiver ends to adjust the operating points of these circuits. The transmitter used by this scheme is shown below: The feedback inverter converts low swing logic levels on the line to full rail to rail CMOS. levels. The NAND/NOR gates ensure that the strong driver is turned on only during data transitions and is turned off as soon as the line crosses the switching point of the feedback inverter to make the logic level on the line equal to the input. The weak driver supplies I_{static} and the line voltage swing at the receiver end is VCM Rx ± I_{static} RL. The receiver also uses feedback to adjust its common-mode voltage. Take the case where V_{CMTx} at the transmitter end.

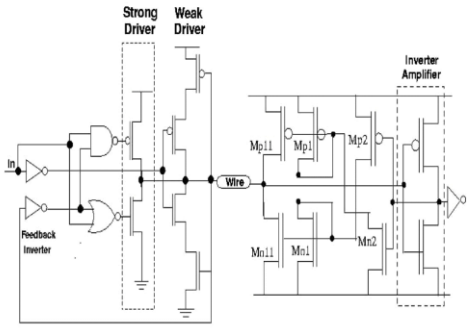


Fig 1. Existing system

Limitations

- Increased delay due to the feedback in the CMS- FB.
- The delay of CMS-Fb becomes 2.5 times its nominal value in the presence of intra-die variations.

- Robust against only inter-die variations due to the feedback in the transmitter and receiver circuits.

Proposed system

The proposed transmitter employs two drivers (a strong driver and a weak driver) with NAND and NOR gates like the transmitter of CMS- Fb scheme.

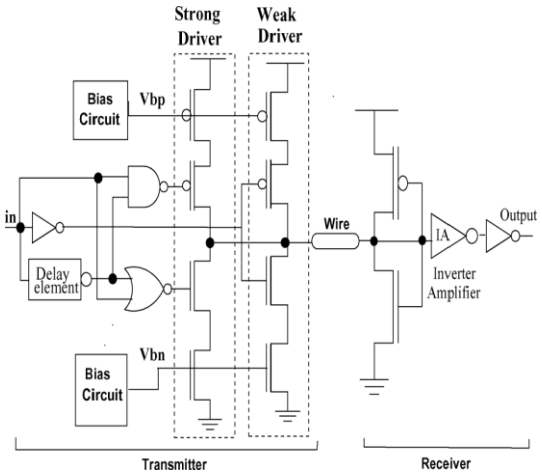


Fig 2. Proposed system

In the proposed transmitter, duration for which the strong driver is turned on is controlled by a delay element and not by the feedback. The strong and weak drivers employ single transistor current sources. The bias voltages (and) of these current sources are generated from a specially designed bias circuit such that current through strong and weak driver remain constant across all process corners. Operation of the bias circuit is discussed in the next section. The proposed receiver uses a diode connected pMOS and nMOS (terminating inverter) followed by an inverter chain. The terminator inverter holds the line voltage near its switching. threshold. Inverter amplifier (IA) and subsequent inverters amplify the small line voltage swing to digital logic levels

II. BIAS GENERATION CIRCUIT

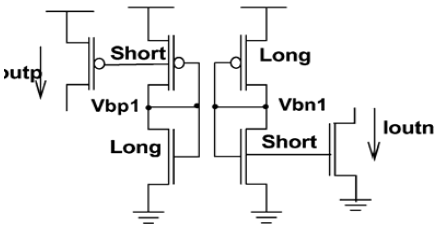


Fig 3. diode-connected transistor based

Bias circuit is used to set an operating point, which provides a steady state operating condition of an active device. The receiver uses a diode connected pMOS and nMOS (terminating inverter) followed by an inverter chain. The bias circuit in the transmitter and the inverter amplifier in the receiver is used for static power consumption.

Weak driver

The weak driver provides the minimal drive required to keep the line (terminated by low impedance) at the desired voltage level. When the input is 1, the p channel driver gate is low. (Weak) Driver (enabled). These charges up the output. As the line voltage reaches VDD − V_{Tp}, the upper p channel transistor turns off, restricting line voltage swing in the up direction. Similarly when the input is 0 the n channel driver transistor is enabled by a high level at its gate.

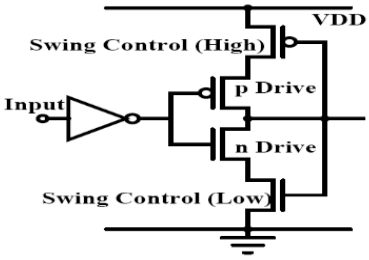


Fig. 3. Steady State (Weak) Driver

The transistor discharges the line. However, when the line voltage approaches V_{Tn} during discharge, the lower transistor turns off, stopping the discharging process. Thus the line can only swing between VDD – V_{Tp} and V_{Tn}.

Strong Driver

The strong driver should be enabled only when the input and the level on the output line do not represent the same logic. The feedback inverter acts as an inverting amplifier converting low swing logic levels on the wire to full swing (inverted) CMOS logic level on its output. The P channel gate is low (enabled) only when both inputs to the NAND are 1. This will happen only when the input is high AND the line is at 0. This is indeed the condition when we we want the strong driver to charge the line. The N channel gate is high (enabled) only when both inputs to the NOR gate are 0. This will happen only when the input is low AND the line is at 1.Notice that the input to the feedback inverter is a low swing level around VDD/2. There-fore it consumes static power. The action of the strong driver is self-limiting. This is because both NAND and NOR receive the input and the inverted logic level of the line. If the input and the logic level of the line are the same, NAND and NOR are fed with input and input. Thus one of the inputs to NAND/NOR is 1, while the other is 0. This ensures that the output of NAND is 1, while that of NOR is 0, so that both the p and n channel transistors are OFF. Therefore the strong driver does not need a series transistor as was the case for the weak driver. When the Input = 1 and Wire voltage < Vm, the inverter output = 1, NAND output = 0 and NOR output = 0.The P channel driver is ON and dumps current to charge the line. When the Input = 0 and Wire voltage > Vm, the inverter output = 0, NAND output = 1 and NOR output = 1.the N channel driver is ON and sinks current to discharge the line. As soon as low swing logic level on the line becomes equal to the logic level at the input Inverter output = input, and so NAND output = 1, NOR output = 0; which disables both drive transistors automatically

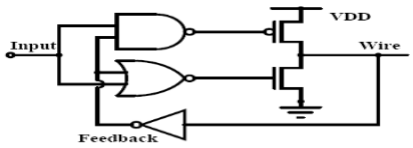


Fig. 4. Dynamic (Strong) Driver

III. ON CHIP TEST CIRCUITS

Two delay measurement schemes were implemented on the chip: one with a 2* 1 multiplexer-de multiplexer (2 *1ux-demux) and the other with a 4 *1 multi plexer-de multiplexer (4* 1 Mux-De mux). A 2* 1 Mux-De mux scheme includes CMS-Fb scheme and CMS-Bias scheme. Hence, it gives only the difference in delay of the two CMS schemes. A 4*1 Mux-De mux scheme includes the two CMS schemes as well as an RO with direct connection. Hence, 4 *1 Mux-De mux scheme also gives the absolute delay of the CMS schemes. Separate pins are assigned to of the digital circuits, output buffers and CMS schemes.

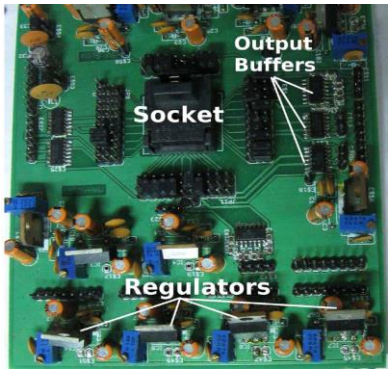


Fig. 5. PC board used for testing

The currents through weak drivers in both the signaling schemes are made externally programmable by using additional current mirrors on the chip . The frequency of the ring oscillator was divided by 16 using a 4-bit on-chip counter before taking it to I/O pads. The counter outputs are buffered by on-board buffers and the frequency is measured using a 6-digit frequency counter. The chip was placed in a socket mounted on a PC board for testing The PC board also includes electronics for generation of variable supply and substrate bias.

Software specification

Tools Used:

Tanner EDA

- S-EDIT
- TSPICE
- W-EDIT

IV. SIMULATION RESULTS

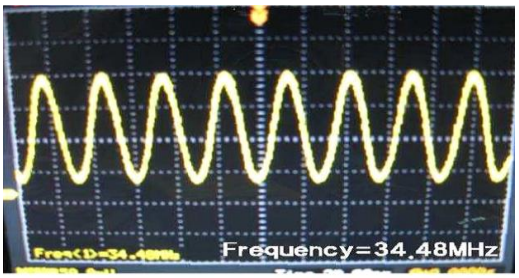
Performance in nominal conditions

Performance in nominal conditions summarizes measured results of the CMS schemes under nominal operating condition (no additional currents and 1.8 V). Frequency measurements of 2 1 Mux-De muxbased scheme show that delay of CMS-bias scheme is less than that of CMS-Fb scheme by 143 ps. Measurement results from 4 1 Mux-De mux-based scheme show that CMS-bias scheme offers 9% improvement in delay over CMS-Fb. This difference is primarily because the inverter amplifier in the receiver of CMS-Fb scheme has to drive transistors and unlike

CMS-Bias scheme The additional capacitive load offered by and is significant as their channel lengths are chosen to be more than 180 nm in order to reduce static power consumed in the receiver.

oscillator signal divided down by 16 as observed on a digital storage oscilloscope (DSO). Since CMS-Fb scheme has more delay than CMS-Bias scheme, the ring oscillator oscillates at lower frequency when CMS-Fb is selected. For fair comparison of energy/bit, of digital circuits (multiplexers, de multiplexers and inverters) was adjusted so that the ring oscillates at the same frequency in both the cases. Hence, for the digital circuit was kept 2.5 V when CMS-Fb was selected and 2.0V when CMS-Bias was selected for energy measurements. The proposed CMS scheme offers 34% gain in energy/bit and 42% improvement in EDP at data rates of 0.64 Gbps over CMS-Fb scheme. Measurements on 2 1 Mux-Demux-based scheme show that the proposed scheme consumes 0.622 pJ/bit at data rate of 0.78 Gbps.

Effect of Inter-Die variations



To assess the effects of inter-die variations, we vary N Well bias in the transmitter and the receiver from 1.8 to 2.3 V identically. Table III shows the delay and energy/bit of both the schemes for different N Well bias voltages. The last two

columns in the table shows the data rate at which the energy/bit was measured. It is apparent from the table that delay of both the signaling schemes do not change much with inter-die variations. Also, they do not consume much additional energy to keep the delay constant with inter-die variations.

These experiments do not capture the effect of variations in parameters of nMOS transistors. energy/ bit and throughput of the two schemes in all process corners. It shows that delay and throughput of both the schemes remain practically the same in the four digital process corners and the nominal case without consuming much additional energy. The local feedback in the transmitter and receiver of CMS-Fb scheme that makes it susceptible to intra-die variations makes it robust against inter-die variations. As long as these of the inverters in the transmitter and in the receiver are matched, CMS-Fb scheme is robust against inter-die variation.

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