DESIGN OF COMPARATOR FOR 7 BIT 100MHz FLASH ADC

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***Abstract*- This paper describes the design of Comparator for 7 bit 100MHz flash A/D converter in CMOS technology. A fully differential CMOS dynamic comparator using positive feedback suitable for FLASH A/D converters with low power dissipation, low offset, low noise and high speed is proposed. Nearly 4.65 mV offset voltage is easily achieved with the proposed structure making it favorable for flash and pipeline data conversion applications. The proposed topology is based on two cross coupled differential pairs positive feedback, has a small power dissipation, less area. The Comparator is the quantizing unit of the Flash ADC. Comparators in flash converter generate what is commonly known as a thermometer code. When everything is working ideally, the collection of comparator outputs should resemble a thermometer. In this paper, a detailed design of fully differential comparator using positive feedback for ADC is given. All the simulations are done in Cadence Virtuoso Analog Design Environment using TSMC 90nm technology.**

I. INTRODUCTION

ADCs are utilized broadly in signal processing systems for converting analog signals into digital signals. An ADC is a device that uses sampling to convert a continuous quantity to a discrete time representation in digital form. It may also provide an isolated measurement such as an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current. The function of an ADC is to accurately convert an analog input signal into digital output represented by a coded array of binary bits. The output bits are generated by processing the analog input signal through a number of comparator steps. The number of bits in the generated code represents the resolution of ADC.

II. FLASH A/D CONVERTER

A Flash ADC (also known as a Direct conversion ADC) is a type of analog-to-digital converter that uses a linear voltage ladder with a comparator at each "rung" of the ladder to compare the input voltage to successive reference voltages.

The output of these comparators is generally fed into a digital encoder which converts the inputs into a binary value. Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. Flash ADCs are suitable for applications requiring very large bandwidths. The basic block diagram of folding A/D converter is shown in Fig.1

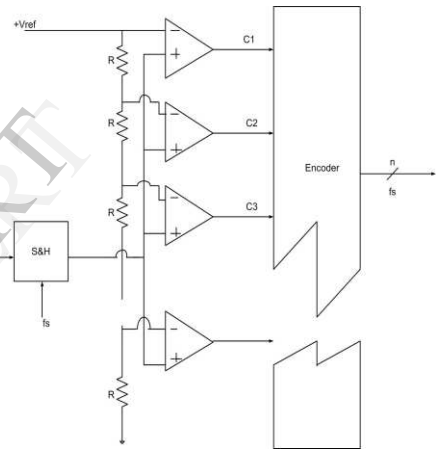

Fig.1.Block diagram of flash ADC.

III. COMPARATOR

Comparators are most probably second most widely used electronic components after operational amplifiers in this world. Comparators are known as 1-bit analog-to-digital converter and for that reason they are mostly used in large abundance in A/D converter.

In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. The conversion speed of comparator is limited by the decision making response time of the comparator. The basic functionality of a CMOS comparator is used to find out whether a signal is greater or smaller than zero or to compare an input signal with a

reference signal and outputs a binary signal based on comparison. The schematic symbol and basic operation of a voltage comparator are shown in Fig.2

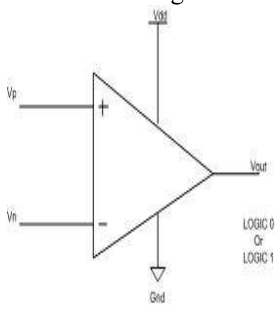

Fig.2. Schematic of Comparator

A. Working of a Comparator

The comparator is a circuit that compares an analog signal (voltage)with another analog voltage or reference voltage and outputs a binary signal based on the comparison.

Fig.3 shows its ideal transfer characteristics. $_{Vp}$ is the input voltage (Pulse voltage) applied to the positive input terminal of comparator and V_n is the reference voltage (constant DC voltage) applied to the negative terminal of comparator. Now if V_p, the input of the comparator is at a greater potential than the V_n, the reference voltage, then the output of the comparator is a logic1, where as if the Vp is at a potential less than the V_n, the output of the comparator is at logic 0.

Comparators can be divided into open-loop and regenerative comparators. The open-loop comparators are basically op amps without compensation. Regenerative comparators use positive feedback, to accomplish the comparison of the magnitude between two signals. A third type of comparator emerges that is a combination of the open-loop and regenerative comparators. This combination results in comparators that are extremely fast.

Nowadays, analog-to-digital converter requires lesser power dissipation, low noise, better slew rate, high speed, less hysteresis, less Offset. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. The power consumption, speed takes major roll on performance measurement of ADCs. Dynamic Comparators are being used in today's A/D converters extensively because these comparators are high speed, consume lesser power dissipation, having zero static power consumption and provide full-swing digital level output voltage in shorter time duration. Back-to-back inverters in these dynamic comparators provide positive feedback mechanism which converts a smaller voltage difference in full scale digital level output.

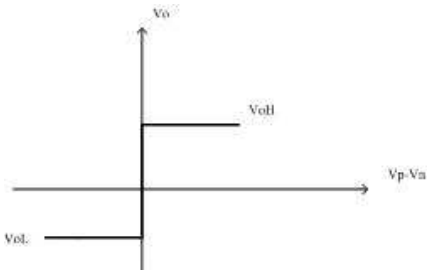

Fig .3 Ideal characteristics

B. Comparator characteristics

There are two types of characteristics namely static and dynamic characteristics.

I. Static characteristics

Static characteristic comprises of gain, output high (V_{OH}) and low states (VOL), Input Resolution, Offset and Noise.

i. Gain

Gain of comparator can be written as:

Gain = Av = $\lim_{\Delta v \to 0} \frac{(V_{OH} - V_{OL})}{\Delta v}$ where Δv is the input voltage change.

ii. Resolution

It is the input voltage change which is necessary to make output swing to valid binary states.

iii. Input Offset Current

The input offset current is the difference between the separate currents entering the input terminals of a balanced amplifier.

iv. Input Offset Voltage

The input offset voltage is that voltage which must be applied between the input terminals to balance the amplifier.

v. Output Offset Voltage

The output offset voltage is the dc voltage present at the output terminal when the two input terminals are grounded.

vi. Input Common Mode Range (ICMR)

This can be defined as the range of input voltage where comparator functions normally meets all required specifications.

II . Dynamic Characteristics

Dynamic characteristics of the comparator comprises of Propagation delay and Gain.

IV. DYNAMIC COMPARATOR

A fully differential typical dynamic comparator[2] is shown in fig .4 The comparator consists of two cross coupled differential pairs with inverter latch at the top. Comparison is made based on the inverter currents, which are related to the inputs, when the CK goes high. The trip point can be changed by appropriate input transistor sizing.

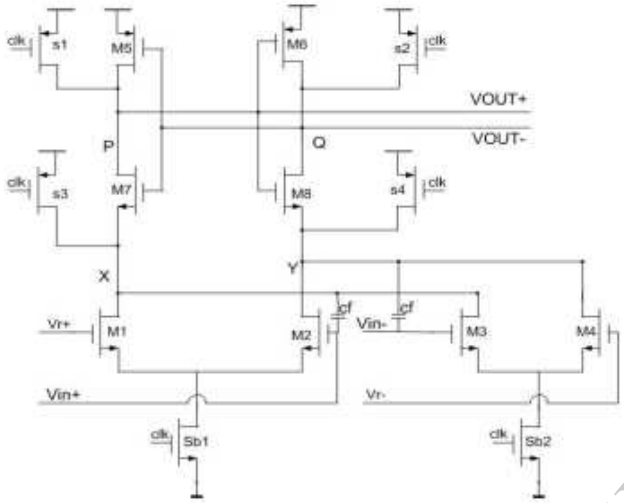

Fig.4 Dynamic Comparator used in Flash ADC.

Few points are worth noting in regard to the problems present in this structure.

- The first drawback of normal differential comparator is related to the clocking of the tail current. When clock signal goes high, the tail current will go into linear region and will be function of the inputs of the respective differential pair[1].
- The second problem is related to the inputs of a differential pair[2]. A large difference between the two inputs to a differential pair will result in the turning of one of the differential pair MOSFET and all of the tail current will be drawn into the other MOSFET. Hence, in effect comparator will be only comparing V_{in}+ with V_{ref}+ (or V_{in}- with V_{ref}-) rather than a comparison of differential Vin with differential V_{ref}.
- The third potential problem associated with the previous code dependent biased decision

To overcome the drawbacks of the typical differential pair comparator, a dynamic comparator has been proposed as shown in fig: 4 which addresses the above listed problems.

A. Dynamic Comparator Operation

The comparator works in two phases, reset phase and regeneration phase during one cycle of comparison. Reset phase happens when the clock signal is low. When CK is low, Sb_1 and Sb_2 are off, S_1- S_4 are ON and nodes P,Q, X, and Y are pre-charged to V_{DD} , placing the comparator in reset mode. When CK goes high, Sb_1 and Sb_2 are turned ON and M_1-M_4 compare the input voltages.

The design of the comparator used in ADCs directly affect the speed and power dissipation[5] of the over all converter. The comparator shown in the Fig:4 is the high speed comparator utilized in Flash ADC. When CK is low, Sb_1 and Sb_2 are OFF, S_1-S_4 are ON and nodes P, Q, X, and Y are pre charged to V_{DD} , placing the comparator in reset mode. When CK goes high, Sb_1 and Sb_2 are turned ON and M_1-M_4 compare the positive input voltage Vin+ with the positive reference voltage V_{r+} and the negative voltage Vin- with the negative reference voltage V_{r-}. Since M5 and M8 are initially off, the resulting differential current first flows through the total capacitance seen at nodes X and Y, creating a differential voltage at these nodes by the time M7 and M8 turn on. After the cross coupled devices turn on, the circuit regeneratively amplifies the voltage, producing rail-to-rail swings at P and Q.

The comparator of Fig. 6.1 offers three important properties that make it attractive for high-speed design. First, the static power dissipation is zero. Second, the circuit requires only a single-phase clock, greatly simplifying the routing across the chip. Third, the input offset is dominated by that of the differential pairs rather than by the offset of the cross-coupled devices. To explain this property, we reexamine the comparator in the amplification mode.

After CK goes high, the input difference is amplified by M1-M4 and the parasitic capacitances at nodes X and Y until V_X and V_Y drop below V_{DD} by V_{THN} . At this point, M7 and M8 turn on but M5 and M6 are still off. The amplification then continues while M5 and M6 contribute a small regenerative gain until M5 and M6 turn on, and initiate the final regeneration. The key point here is that the input is amplified substantially before M5-M8 turn on.

Another important phenomenon in the comparator is the large kick-back noise[5][3] produced at the beginning of reset and regeneration modes. This effect is particularly critical in the first stage and can introduce significant dynamic offsets, saturating the second stage and creating non-linearity. Adding a pair of cross-coupled capacitors equal to 8 fF at the input reduces the kick-back noise.

B. Kickback Noise

An important issue in ash converters is the accumulative effect of the kick back noise introduced by comparators. When comparator is clocked nodes X and Y start falling. Due to C_{gd} the decay gets coupled back to V_{in} and V_r. That is there is a kick to the input and reference voltage. Now, V_r is coming from resistor ladder. The kick should be small such that the reference voltage does not move that much from cycle to cycle. That is the reference voltage should settle back to its ideal value before next sample is quantized. There are many solutions to this problem, a few techniques are discussed below.

C. Kickback Noise Reduction Techniques

This technique[3]can be used in any latched comparator, being specially suited to the cases where the circuit preceding it is in reset, during the regeneration phase of the comparator. Insert sampling switches before the input differential pair, which are opened during the regeneration phase. The kickback noise is eliminated in this phase, and a sampling function is implemented, which may be convenient in some applications. The sampling switch is placed before the comparator inputs. During the regeneration phase these switches are opened and disconnect the inputs from rest of the circuit. The switches should be sized as small as possible compared to the total capacitances at the inputs to minimize the effect of charge injection. This has the downside of increasing the offset voltage, due to the mismatches in the charge injection of the input switches.

1) Detect when the latched comparator has already decided and make an asynchronous reset of the sampled input voltage. This prevents the previous sampled voltage from disturbing the next comparison.

V. Comparator Design

- Vref+ = 900 - 300 = 600mV
- Vref =Vref+ -(-Vref+)
  = 600 -(-600)
  = 1200mV
  = 1.2V
- LSB = Vref / 2^n
  Here, n = 7
  Therefore, LSB = 1.2 /2^7
  LSB = 9.3mV
- Offset voltage can be calculated as,
  Offset voltage=LSB/2
  = 9.3mV / 2
  = 4.65 mV
- Offset Voltage = A /(√WL)

From this equation, we can find the width of the input transistors M1,M2, M3 and M4.The length of the input transistors should be minimum to avoid channel length modulation, so the length of the transistors selected as 100nm.Using the above equation, the width is calculated as, W = 11.56u.For PMOS transistors, the width is double that of the NMOS transistors..The input capacitances of 127 comparators obtained from the calculation is 8pF.

VI. Simulation Results

The below figure shows the simulation result of ideal flash ADC. i.e., the comparators used are ideal. If the transient sum of the comparator output follows the input, then we can say that the comparator is working. In other words, when CK is high, the comparator tracks the input, and when CK goes low, it stores the instantaneous polarity of Vin+ - Vin-. Thus, if all the comparators are strobes at the same time, they collectively store the polarity of the difference between Vin and each Vj , thereby operating as a distributed sample-and-hold. From the graph, it is observed that the output follows the input.

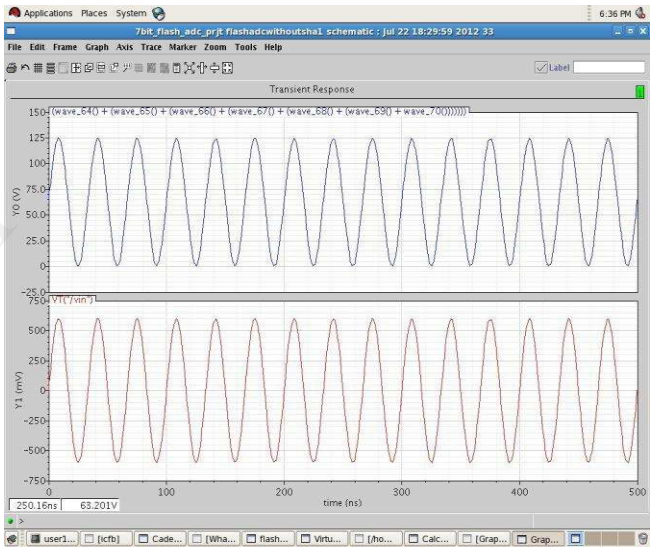

Fig 5: Simulation result of ideal FLASH ADC.

The below figure shows the simulation result of real flash ADC. i.e., the comparators used are dynamic differential comparators. Here also, when CK is high, the comparator tracks the input, and when CK goes low, it stores the instantaneous polarity of Vin+ - Vin-. From the graph, it is observed that the output follows the input.

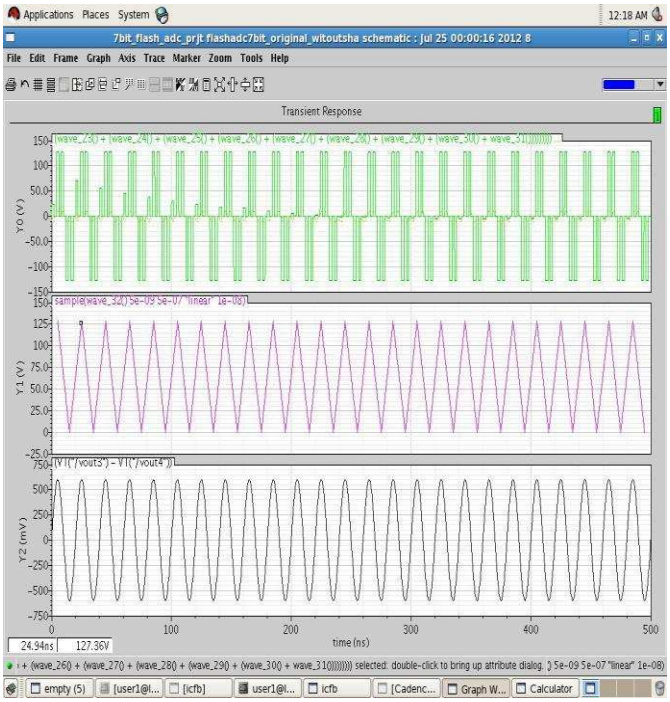

Fig 6: Simulation result of FLASH ADC

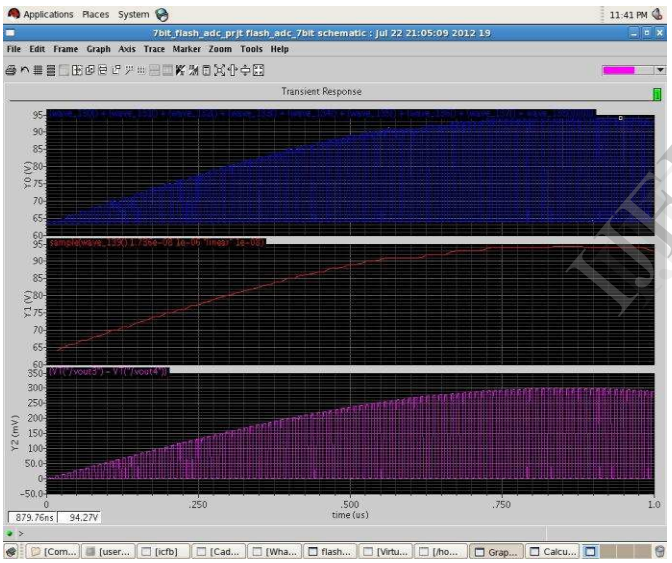

Fig 7: Simulation result of FLASH ADC.

VII. Conclusion and Future Scope

A. Conclusion

A dynamic comparator using positive feedback was proposed for high speed, low offset, low power dissipation targeted for ADC application. The proposed structure shows significantly low power dissipation, high speed, low noise low offset. The modifications made to the typical differential pair dynamic comparator can easily reduce the overall offset to only few milli volts as compared to hundreds of milli volts. With the positive feedback, Dynamic comparator width is reduced to the mV range with the 100 MHz clock. This comparator is used to design a 7bit 100MHz Flash ADC with
Sample and Hold. The Comparator is the quantizing unit of the Flash ADC. Flash ADCs employ parallelism and distributed sampling to achieve a high conversion speed. Comparators in a ash converter generate what is commonly known as a thermometer code. If a particular comparator's reference point is below the level of the input signal, the comparator's output is high; if the reference point is above the input, its output is low. When everything is working ideally, the collection of comparator outputs should resemble a thermometer: The encoder is used to convert the thermometer code, generated by the comparators, into a binary code that approximates the input

B. Scope for future work

From simulation results shows that Dynamic comparator gives less offset voltage, low noise ,low power dissipation compared to conventional comparators. In the future by using Auto zeroing techniques, one can reduce the offset voltage, power consumption, noise response. By decreasing the number of transistors, we can reduce the Area, Power dissipation. And also by reducing the size of each transistor one can get less power dissipation, high speed, matching accuracy.

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