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Design of CMOS Full Adder Cells for Arithmetic Applications

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Abstract

Full adders are the important components in applications such as digital signal processor (DSP) architectures and microprocessors. In addition to its main task, which is adding two numbers, it participates in many other useful operations such as subtraction, multiplication, division, address calculation, Etc. In most of these systems the adder lies in the critical path that determines the overall speed of the system. This paper carried out a comparison against cmos full adders designed in different logic styles in terms of power and delay. The simulation results are produced using the Micro wind & DSCH software's. And using these cmos full adders various arithmetic applications are developed.

Keywords: - Full adder cells; Micro wind;

I. INTRODUCTION

Circuit realization for low power and low area has become an important issue with the growth of integrated circuit towards very high integration density and high operating frequencies. The full adder circuit adds three one-bit binary numbers (Cin, A, B) and outputs two one-bit binary numbers, a sum (SUM) and a carry (COUT). Due to the important role played by Full adder in various arithmetic units, optimized design of Full adder to achieve low power, small size and delay is needed. The primary concern to design Full adder is to obtain low power consumption and delay in critical path and full output swing with low number of transistors to implement it.

Micro wind is truly integrated EDA (Electronic design automation) software encompassing IC designs from concept. Micro wind integrates traditionally separated front-end and back-end chip design into an integrated flow, accelerating the design cycle and reduced design complexities. It tightly integrates mixed-signal implementation with digital implementation, circuit simulation, transistor-level extraction and verification.

In this paper, we propose the design of arithmetic applications using the full adder cells. The paper is organized as follows: section II, gives a brief review of the cmos full adders subsequently, section III describes the arithmetic applications using the cmos full adders. In section IV, the comparison results of the full adders are given and discussed. Finally a conclusion will be made in the last section.

II. FULL ADDERS

A basic Full adder cell in digital computing systems is the 1-bit full adder which has three 1-bit inputs (A, B, and C) and two 1-bit outputs (sum and carry). The relations between the inputs and the outputs are expressed as:

SUM = A ⊕ (B ⊕ C)
COUT = AB + BC + AC

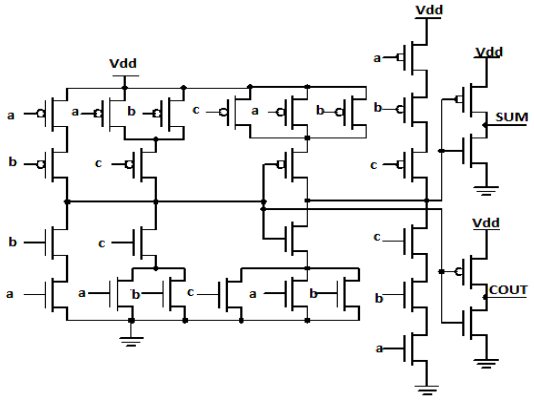

Fig 1:- A Conventional full adder

The above shown Conventional full adder [1] is a combination of PMOS pull up transistor and NMOS pull down transistor. It is well known for its robustness and scalability at low supply voltages. But the use of substantial number of transistors results in high input loads, more power consumption and larger silicon area.

Another conventional adder is the (CPL) Complementary Pass Transistor Logic[2]. It provides high-speed, full-swing operation and good driving capabilities due to the output static inverters and fast differential stage of cross coupled PMOS transistors. But due to the presence of a lot of internal nodes and static inverters, there is large power dissipation.

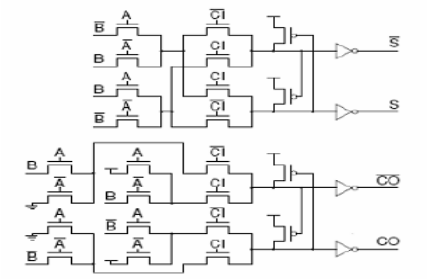

Fig 2:-CPL full adder

In the SERF adder cell [3], the implementation of XOR and XNOR of A and B is done using pass transistor logic and an inverter is to complement the input signal A. This implementation results in faster XOR and XNOR outputs and also ensures that there is a balance of delays at the output of these gates. This leads to less spurious SUM and Carry signals. The energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic. The combination of not having a direct path to ground and the re- application of the load charge to the control gate makes the energy-recovering full adder an energy efficient design. Although it is low-cost and low-area cell the outputs are not full-swing and cannot work correctly at low voltages and it exhibits high delay when the cells are cascaded to make large full circuits.

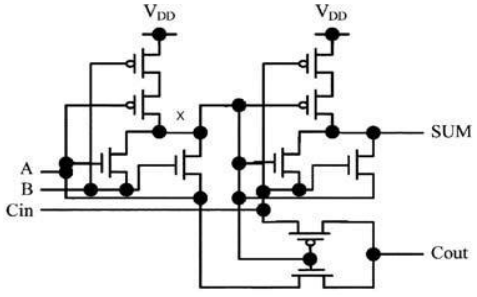

Fig 3:-Static energy recovery full adder

The new 14T adder [3] requires only 14 transistors to realize the adder functions. It produces the better result in threshold loss, speed and power by sacrificing four extra transistors per adder cell which exists in the SERF by inserting the inverter between XOR Gate outputs to form XNOR gate. The power dissipation in this circuit is more than the 28T adder. However with same power consumption it performs faster

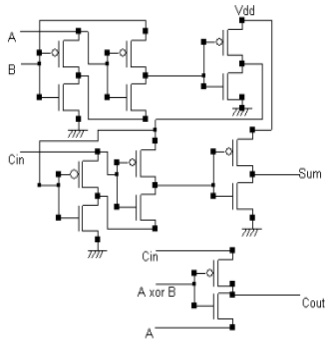

Fig 4:-Improved 14T adder

The 9T adder [4] requires only 9 transistors to realize the adder functions. In this circuit an XOR gate and a multiplexer are used to implement Sum and one multiplexer to implement the Cout. The sum output is basically obtained by cascading 3T XOR gate in addition to an extra transistor M9. Carry is implemented using 2T multiplexer. The main drawback of this design is threshold loss problem.

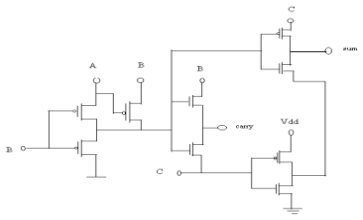

Fig 5:-9T full adder

III. FULL ADDERS IN ARITHMETIC APPLICATIONS:

1. RIPPLE CARRY ADDER:

The ripple carry adder is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. It is called a ripple carry adder because each carry bit gets rippled into the next stage.

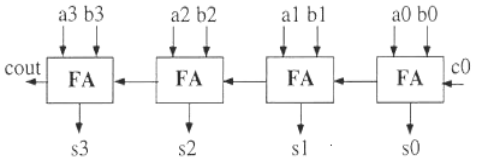

Fig 6:-Ripple carry adder

2. CARRY SAVE ADDER:

The carry-save adder reduces the addition of 3 numbers to the addition of 2 numbers. The carry-save unit consists of *n* full adders, each of which computes a single sum and carries bit based solely on the corresponding bits of the three input numbers. The entire sum can then be computed by shifting the carry sequence left by one place and appending a 0 to the front (most significant bit) of the partial sum sequence and adding this sequence with RCA produces the resulting *n* + 1-bit value.

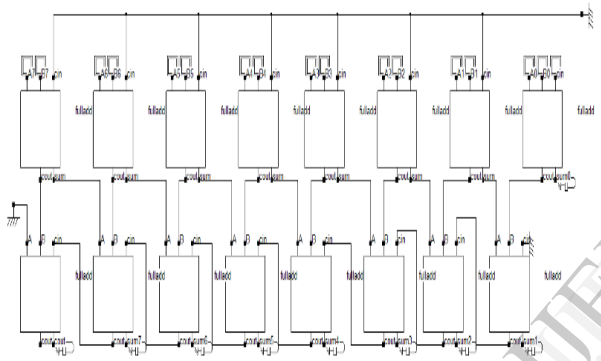

Fig 7:-Carry save adder

3. CARRY INCREMENT ADDER:

An 8-bit increment adder includes two RCA (Ripple carry adder) of four bit each. The first ripple carry adder adds a desired number of first 4-bit inputs generating a plurality of partitioned sum and partitioned carry. Now the carry out of the first block RCA is given to CIN of the conditional increment block. Thus the first four bit sum is directly taken from the ripple carry output. The second RCA block regardless of the first RCA output will carry out the addition operation and will give out results which are fed to the conditional increment block.

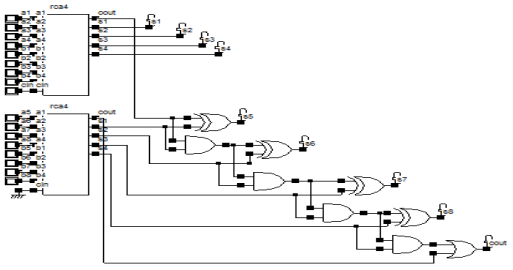

Fig 8:-Carry increment adder

4. CARRY SKIP ADDER:

A carry-skip adder consists of a simple ripple carry-adder with a special speed up carry chain called a skip chain. Carry skip adder is a fast adder compared to ripple carry adder when addition of large number of bits take place; carry skip adder has O (_n) delay provides a good compromise in terms of delay, along with a simple and regular layout. A carry-skip adder is designed to speed up a wide adder by aiding the propagation of a carry bit around a portion of the entire adder.

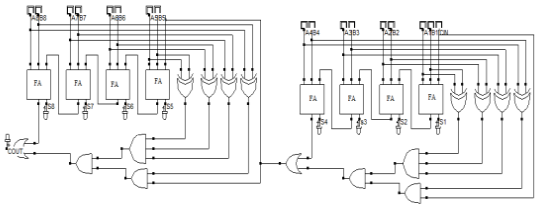

Fig 9:-Carry skip adder

5. CARRY BYPASS ADDER:

As in a ripple-carry adder, every full adder cell has to wait for the incoming carry before an outgoing carry can be generated. This dependency can be eliminated by introducing an additional bypass (skip) to speed up the operation of the adder. An incoming carry Ci,0=1 propagates through complete adder chain and causes an outgoing carry C0,3=1 under the conditions that all propagation signals are 1. This information can be used to speed up the operation of the adder, In a CBA the full adders are divided into groups; each of them is "bypassed" by a multiplexer if its full adders are all in propagating.

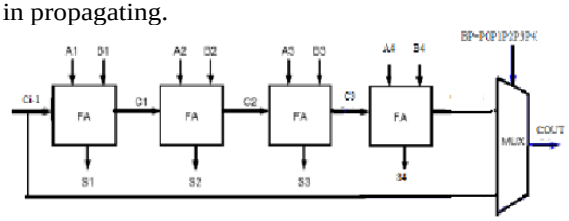

Fig 10:-Carry bypass adder

6. NEGATIVE NUMBER GENERATOR CIRCUIT:

The 4-bit negative number generator circuit generates a 4-bit negative number for a given binary number using the cmos full adders. The circuit consists of 4 full adders and 4 ex-or gates. The Neg input controls the overall operation of the circuit.

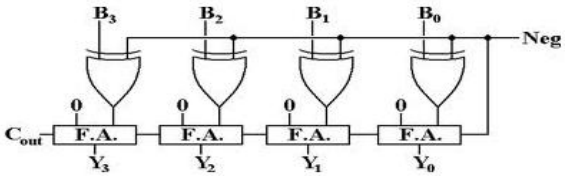

Fig 11:-Negative number generator circuit

7.*2-BIT COMPARATOR USING FULL ADDERS:*

The Comparator is a very basic and useful arithmetic component of digital systems. Full adder based comparator is a 2-bit comparator consist of 2 full adders, 2 inverters. There are two outputs. One shows A=B and another shows B>A.

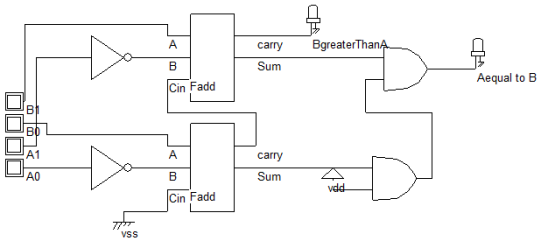

Fig 12:-2-BIT Comparator

IV.SIMULATION RESULTS

The simulation results are obtained by verifying the functionality of the full adders in digital schematics and for these full adders the layouts are drawn in micro wind. The layout of the 9T full adder is as shown in the figure below.

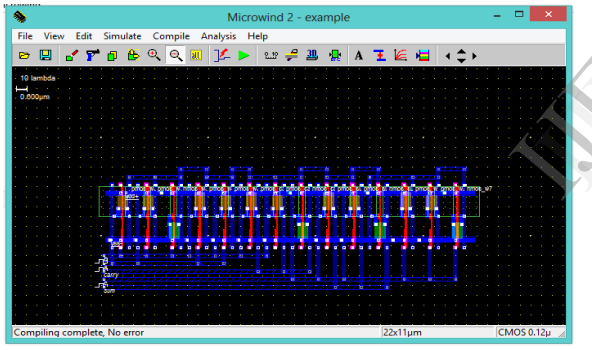

Fig 13:-Layout view of the 9T full adder

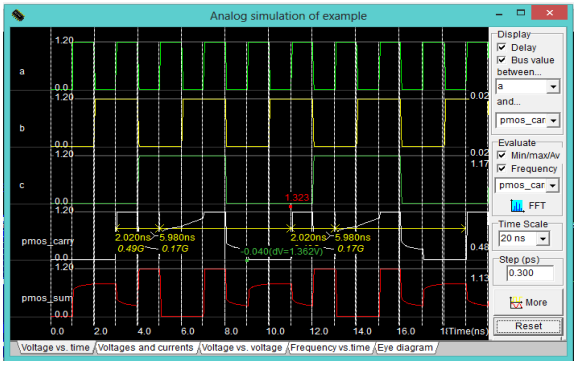

Fig 14:-Simulation analysis of the 9T full adder

Type of full adder	Power(uw)	Delay	No.of transistors	Area	Vdd(V)	Idmax	F	PDP
CCMOS	20.412	31ps	28	317.1	1.20	2.076mA	0.50G	$6.32x10^{-14}$
CPL	52.655	52ps	24	550.8	1.20	7.487mA	0.50G	$2.7x10^{-13}$
SERF	6.965	15ps	10	179.6	1.20	1.077mA	0.25G	$1.00x10^{-15}$
14T	14.767	56ps	14	248.1	1.20	0.579mA	0.25G	$9.9x10^{-14}$
9T	1.036	27ps	9	158.0	1.20	0.563mA	0.12G	$2.79x10^{-15}$

Fig 15:-Comparison of Full adders

Among the above discussed cmos full adders the 9T full adder is having the l area, low speed, low power. And also the SERF full adder is having the low area, low pdp but it could not provide the full swing at the output. Even though the new 14T Full adder provides the full swing the pdp value is more. The above results are obtained from the layouts drawn in micro wind in 0.12um cmos technology.

V. CONCLUSION

The cmos full adders in different logic styles are designed and simulated. From the simulation results it is observed that the 9T full adder is having the low PDP, low area and also it consumed low power. Any arithmetic circuit which uses this low power full adder consumes low power. And using these cmos full adders many arithmetic applications like comparator, ripple carry adder etc are designed and simulated.

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