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Design of Charge Pump Circuit for PLL Application: A review

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***Abstract*—In this paper, deals with different approaches to design a high speed CMOS charge pump circuit for PLL application. A charge pump is a kind of DC to DC converter that uses capacitors as energy storage elements to create either a higher or lower voltage power source. Charge pump make use of switching devices for controlling the connection of voltage to the capacitor. Charge pump is one of the important parts of PLL which converts the phase or frequency difference information into a voltage, used to tune the VCO.**

Keywords— Charge pump, PFD, loop filter, phase-locked loops (PLL).

I. INTRODUCTION

A charge pump IC converts, and optionally regulates, voltages using switching technology and capacitive-energy storage elements. Charge pumps offer high-efficiency and compact solutions for applications with generally low-output current requirements. Charge pump maintain constant output with a varying voltage input. A charge pump based Phase lock loops (PLL) are widely used as a clock generator in a variety of applications including microprocessor, wireless receivers, and disk drive electronics [4]. As technology changes, our demands are also increases, high speed, portable and low power consumption communication system has become increasingly day by day. These systems require high-precision local clock generator (local oscillator) and difficulty is deal with the help of PLL circuit design. Due to the irreplaceable advantages, this technology is most widely in cmos charge pump phase lock loop (CPLL). CPLL is a very simple and efficient method of designing PLL having low jitter and low power, zero static phase error and high speed [15]. The charge pump circuit is the heart of PLL. The chare pump (CP) based PLL is the most popular architecture. The CP-PLL derives its name from the fact that the phase detector (PD) output is a current source as opposed to a voltage source and "pumps" current into and out of the loop-filter. This form of PLL is popular because it is adaptable to integration in microcircuit devices. This type of the CPLL consists of a phase frequency detector (PFD), a CP, a passive loop filter (LF), and a voltage controlled oscillator (VCO). In a PLL the phase difference between the reference signal (often from a crystal oscillator) and the output signal is translated into two signals – UP and DN. The output of the PFD is fed to a charge pump circuit to get a constant current at the output. The charge pump output is passed through a low pass filter to generate the control voltage for the VCO circuit. Figure1 show block diagram of PLL [1].

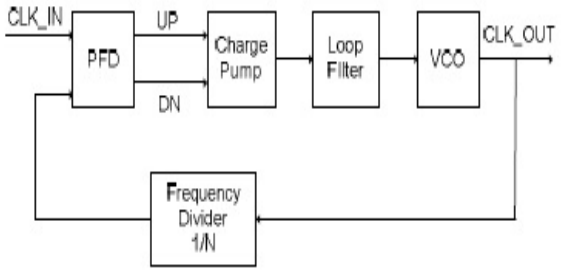

Figure 1: phase locked loop

Hence there are five functional blocks in a PLL circuit such as phase frequency detector (PFD), Charge Pump, loop filter, voltage controlled oscillator (VCO) and frequency divider.
In this paper explain Charge Pump circuit and also taken result of many research worker.

II. OVERVIEW OF BASIC CHARGE PUMP

A charge pump is a three position electronic switch which is controlled by the three states of PFD. Current sources I_1 and I_2 are identical. Two outputs of PFD QA and QB are given to the X and Y inputs of charge pump (CP) respectively. Capacitor Cp serves the purpose of loop filter. Figure 2 shows the combined architecture of the charge pump and loop filter [7].
If QA=QB=0, then S1 and S2 are off and Vout (or Vcont) remains constant. If QA is high and QB is low, then I_1 (UP current) charges Cp. Conversely if QA is low and QB is high, then I_2 (DOWN current) discharges Cp. Hence, if suppose, A leads B, then QA continues to produce pulses and V_{out} rises steadily.

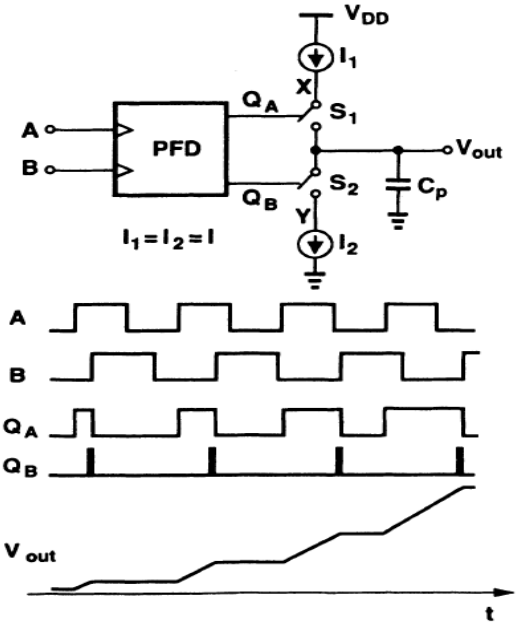

Figure 2: PFD-CP-Loop Filter Combination

III. REVIEW OF PREVIOUS CHARGE PUMP DESIGN

Today is the world of electronics and sizes of their products are regularly decreasing but its efficiency and reliability increasing, due to explosive growth in VLSI technology. Wireless communication has led to increased demand for products that are low cost, low power, and compact size. Recently CMOS technology is used to design RF components such as low-noise amplifiers, mixers, and VCO because it easily achieves high level of RF/analog/digital integration in single chip system implementation. CHARGE PUMP is a key component of PLL which used to tune VCO. So a large number of research papers are published on improvement of CHARGE PUMP.

Yogendra Pratap Singh et al. proposed new Charge Pump circuit which consist of pull up and pull down network. The pull up current I1 and pull down current I2 are both set to 10uA. The operating frequency is 400MHz. In this circuit use 50nm technology, 1V power supply, and output voltage range is from 995mV up to 1015mV.in this work analyses the design of a mixed signal Phase Lock Loop for faster phase and frequency locking [1].

Rajesh B. Langote et al. design Charge Pump to remove instability and ripple in the control voltage. A precise current mirror is used to remove instability. The output control voltage Vcntrl will increase/decrease depending on whether UP/DN pulse occurs. It uses 0.18um technology, 3.3V power supply. In this paper presented a PLL with better lock time. The lock time of the PLL mainly depends upon the PFD architecture used and the parameter of the Charge Pump and Loop filter. So by properly choosing the PFD architecture and adjusting the Charge Pump current we can achieve a better lock time [2].

Huili Xu1 et al. design Charge Pump for PLL. The proposed charge pump circuit includes a charge pump core circuit and two operational amplifiers. In which actual, the reference current IREF is implemented using current Mirror. The switches are implemented by connecting the source and drain of NMOS and PMOS to avoid the inherent mismatch of NMOS and PMOS. The gates of the switch transistors are connected to the outputs of PFD which turn on the switches or not. In this CP reduce mismatch current, reduce phase noise. In this design use 0.18um technology, 1.8V power supply [4].

The results of the Charge Pump given by different researcher are shown below.

B. Razavi give an idea about CMOS charge pump circuit shown in fig. but there is a non ideal effects such as leakage current, mismatch between up and down current and limited Acquisition range. Circuit diagram of basic charge pump are shown in fig.3 Simulation result of conventional charge pump and PFD are given below [7].

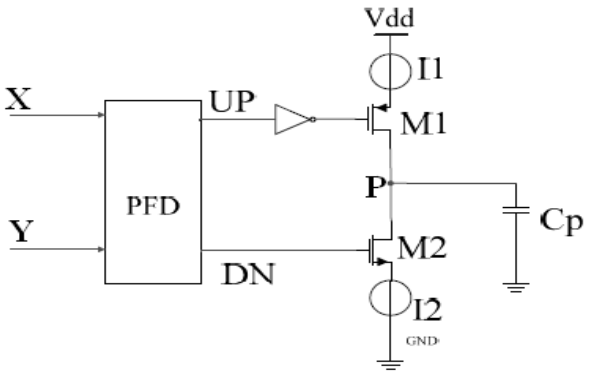

Figure 3: simple model of charge pump

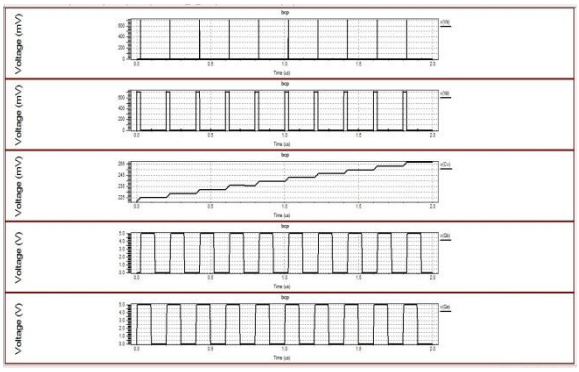

Figure 4: simulation results of PFD and conventional charge pump

Shaungshuang Zheng et al. present a novel Charge Pump circuit. A rail to rail operational amplifier is used to enable the CP charge and discharge currents to be match well in a wide output voltage range. The proposed CP designed in 0.18um CMOS process. The test result show that the output voltage range of 0.23V to 1.72V, with the charge pumps current of 100uA.the average power consumption of the charge pump in the locked condition is around 0.57mW under 1.8V supply voltage [16].circuit of charge pump and simulation result are shown in fig.

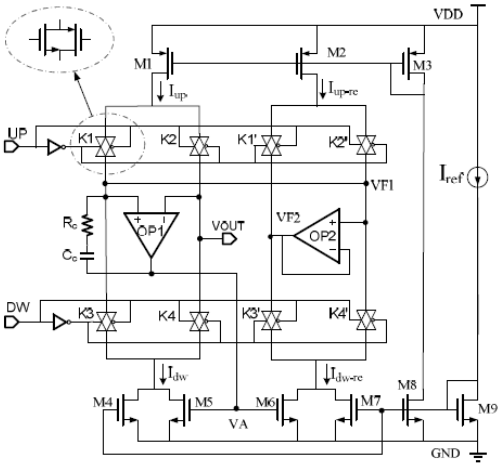

Figure 5: structure of charge pump [16]

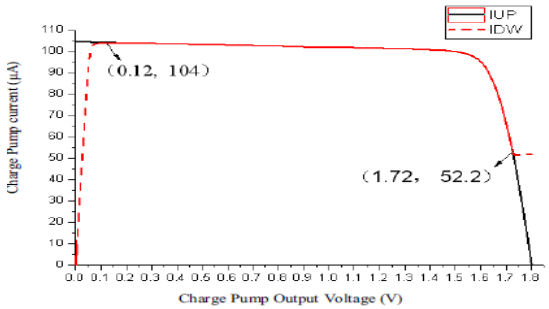

Figure 6: simulation result of current match characteristic of charge pump [16]

Jyoti Gupta et al. present a high speed CMOS charge pump circuit for PLL application using 90nm CMOS technology that operates at 1V power supply. It has output voltage range from 995mV up to 1010mV. The pull up and pull down current are both set to 100uA.the operating frequency is 1000MHz [15].

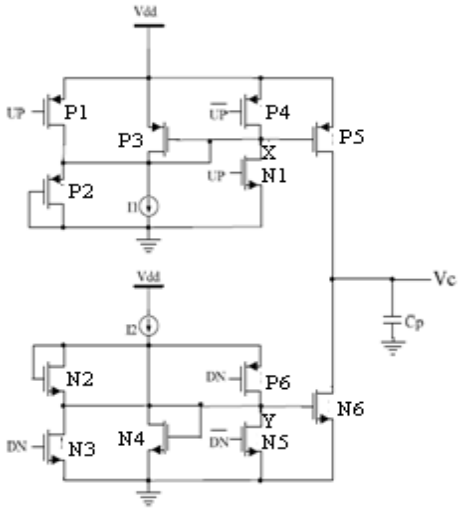

Figure 7: structure of charge pump [15]

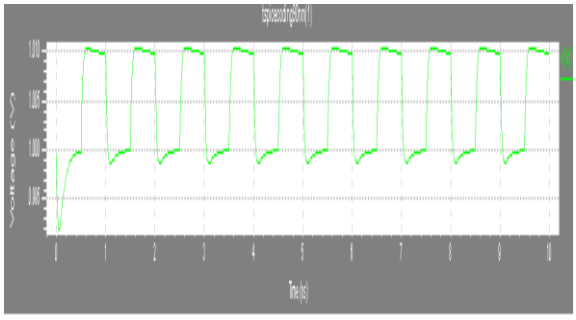

Figure 8: charging & discharging waveform of the charge pump [15]

Sheng Chen et al. proposes improved current steering charge pump in high speed application in 90nm technology. In order to improve the conventional current steering charge pump performance, the proposed charge pump consisting of current compensation circuit, clock feed through reduction circuit, accelerating acquisition circuit, and rail to rail voltage follower is shown in Fig.7.
The proposed circuit has two amplifies, AMP1 and AMP2. Both of the amplifiers are designed by rail to rail. AMP1 is used to improve the matching precision between charging current and discharging current. Similarly, AMP2 is added to reduce the effect of charge sharing, which makes Voltage of point Vout1 follow the voltage of point *V*out [14].

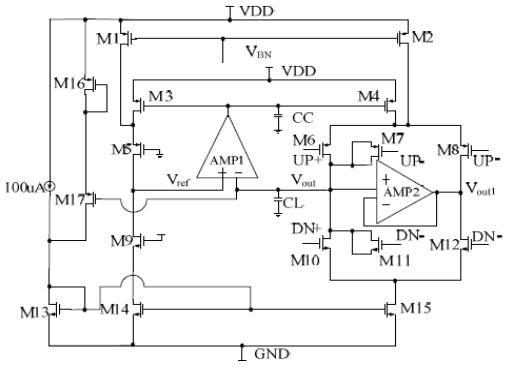

Figure 9: structure of charge pump [14]

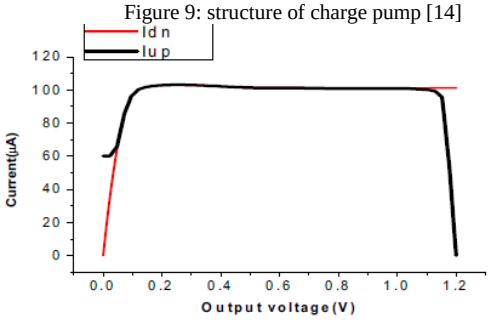

Figure 10: simulation results of charging & discharging current of charge pump [14]

Aniruddha c. Kailuke et al. shows a new charge pump that can assign the control inputs for the CTS's dynamically by adding pass transistors MN's and MP's to the NCP-1 circuit[13] . The CTS's in NCP-2 can be turned off completely when required and still can be turned on easily by the backward control as in the NCP-1 case. The Dickson charge pump circuit consists of two pumping clocks Φ1, and Φ2, which are anti-phase and have voltage amplitude of VΦ.

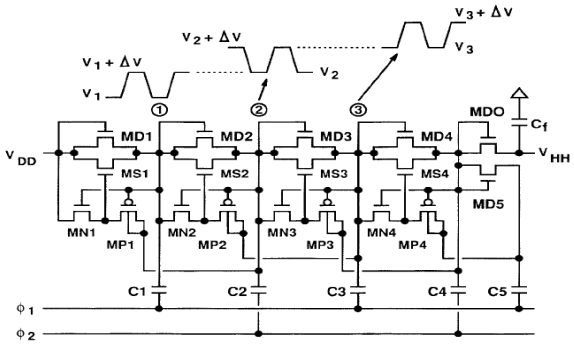

Figure 11: The Dickson Charge pump with Dynamic charge transfer switches [13]

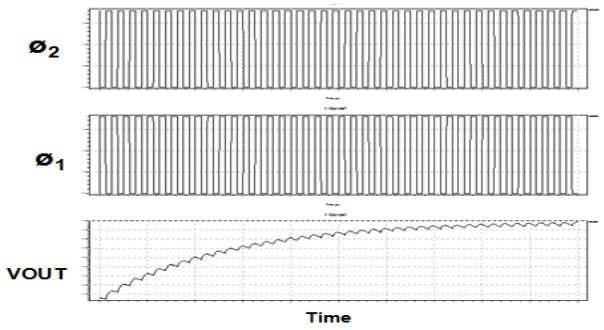

Figure 12: Output waveforms of modified Dickson Charge pump with Dynamic charge transfer switches

TABLE I
Comparison of the Previous Work

Parameter	Ref [1]	Ref [14]	Ref [15]	Ref [16]
Technology	50nm	90nm	90nm	0.18um
Power supply	1V	1.2V	1V	1.8V
Frequency	400-MHz	500-MHz	1000-MHz	NA
Power consumption	NA	1.4mW	NA	0.57mW
Output voltage	995mV to 1015mV	1.1V	1010mV	0.23V-1.723V
Up and down Current	10uA	100uA	100uA	100uA

IV.CONCLUSION

Various design analysis used for implementation of Charge Pump for PLL Application has presented in this paper. The power Consumption is comes Down, Operating voltage is reducing, and operating frequency increasing and locking time is reducing, and output voltage is also increase. CMOS process has effectively improved their Performance by using um or nm VLSI Technology. I have tried to focus on different approach taken by different research worker and their summarize prospect has presented here.

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