Design of Binary Weighted Current Steering DAC using OEM Technique

P. Karthika
Dept. of Electronics and
Communication
Engineering
PSNA College of Engineering and
Technology
Dindigul

T. Madhubala
Dept. of Electronics and
Communication
Engineering
PSNA College of Engineering and
Technology
Dindigul

T. Chelladurai
Dept. of Electronics and
Communication
Engineering
PSNA College of Engineering and
Technology
Dindigul

*Abstract-*This paper describes reduction of mismatch in binary weighted current steering DAC. The mismatch is a major problem occurred in DAC, whenever signal is converted from digital to analog. Due to this resolution and accuracy of the DAC get affected. To avoid this problem ordered element matching (OEM) technique is proposed. OEM technique used to order the elements to avoid mismatch in order to improve the performance of the DAC. The method was done by 15- bit binary weighted current steering DAC.

Keywords-Binary weighted; mismatch; ordered element.

I. INTRODUCTION

The DAC is a digital to analog converter is used to convert digital information into analog form. The current source is implemented in terms of three architectures: binary, unary, segmented. The application of binary weighted DAC is high speed applications such as all communication systems (transmitters, receivers, display systems) and medical, instrumentation applications. In this application the device matching is a major problem. Supply voltage, temperature, stress causes a matching problem in device. There are several methods to eliminate the matching error, traditional mismatch technique reduce the mismatch in certain range. The techniques are trimming, calibration circuits and switching sequence adjustments. But having some disadvantages like complicated circuitry, high cost, affects the resolution.

A new technique is differing from older methods known as ordered element matching (OEM) was developed and it is based on order statics. The main concept of this method is to eliminate random variations by grouping the ordered element components. After completing the several iterations of OEM, a unary –weighted array elements are well matched to the binary-weighted array elements generated. In this paper 15-bit binary weighted current steering DAC has been designed in a tanner tool. In this DAC has a 7-8 segmentation, the OEM is applied 7-bit unary –weighted MSB array. Finally a 7-bit unary weighted array was formed. The 8-bit LSB array is a binary weighted structure. So, 15-bit DAC has formed at the end of the operation. This paper is organized as follows. In section II describes the related works to reduce the mismatch. In Section III the operation of OEM was presented. In section IV deals the implementation of the

DAC. Experimental results are shown in section V. Section VI describes the performance estimated results and finally conclusion of this brief is presented in section VII.

II. RELATED WORKS

There are several techniques are proposed to compensates the random mismatch errors for data converters. The techniques are trimming, calibration circuits and switching sequence adjustments. Some technology described in the following paragraphs.

In this trimming method [2] it compensates the mismatch error by balance the component parameter at wafer stage. In this method it requires the careful test equipment to progressively measure the values and trimmed parameters are compared to the nominal values. There are two types in the trimming technique. The first one is the physical dimension of circuit element to change by applying the laser beams. The next type is those connects or disconnect the binary weighted array using MOS switches. Both type forms a trimming but cost wise this method is not satisfied.

Niklas U. Andersson and et al [4] proposed a technique called dynamic element matching (DEM) is increase the matching between the references. The input is in the form of digital is be a thermometer coded, these bits are assembled before entering to the 1-bit DAC. The output from the 1-bit DAC is summed and formed the desired output. The concept of this method is dynamically changing the positions of mismatched elements at different time, so the equivalent component at each position is nearly matched on a time average. In this method has advantage of linear performance can be achieved. However this method is not suitable for high resolution DAC.

Mohamed Aboudina and et al [3] proposed a mismatch shaping technique for sigma delta modulator. A proposed sigma delta modulator shapes the digital to analog converter mismatch errors. In this method the quantization noise is removed by the sigma delta modulator. The basic idea of this DAC is the modulator is formed from the second order loop by factoring out the first integration and put into the series of input of the DAC. This method helps to increase the performance of the DAC. The high speed applications it produce distortion.

III. ORDERED ELEMENT MATCHING

Random mismatch errors are important issue in the data converters, these errors are caused by matching critical circuit components and variations in the semiconductor process. This leads to unpredictable circuit performance at the output. The OEM is a technique is aimed to create the new component tree in order to reduce variations depending to their original component order.
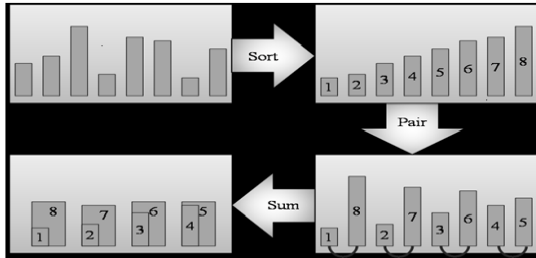

Fig. 1 OEM techniques for unary weighted array resistor has sample size 8

The OEM method consists of three steps three steps sort, pair and sum. The *Fig.1* shows the OEM technique for matching the unary weighted array resistor with sample size 8. The rectangles in the figure denote the resistance value with random variations. The first step is to order the resistance value of resistors in ascending order. The next step is pair the complimentary order resistor into group. All are grouped by (1,8),(2,7),(3,6),(4,5). Then the final step is to sum the two resistors in the group and forming a new array have a sample size of 4.so resistance variations are reduced considerably. To improve the matching activity in the array of transistors or capacitors is done by using this technique. Here rectangles are denoted the drain current and capacitor values respectively.

IV. IMPLEMENTATION OF DAC

Using the OEM technique 15-bit current steering DAC has been designed is shown in *Fig.2*. The LSB bits 0 to 7 bits are given to delay equalizer. Here bridged-T delay equalizer are used, is an electrical all pass filter.
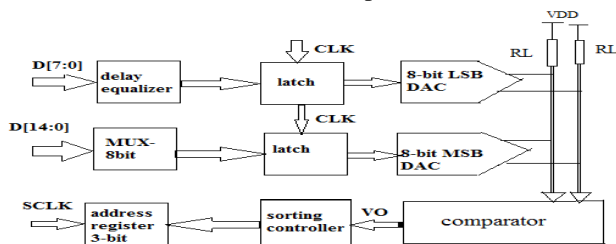

Fig. 2 15- bit binary weighted current steering DAC

The purpose of this equalizer is to insert a constant delay at all frequencies in the signal path is represented in *Fig.3*. The output from the delay equalizer is given to the latch. Latch is circuit that has two stable states and can be used to store state information shown in *Fig.4*.
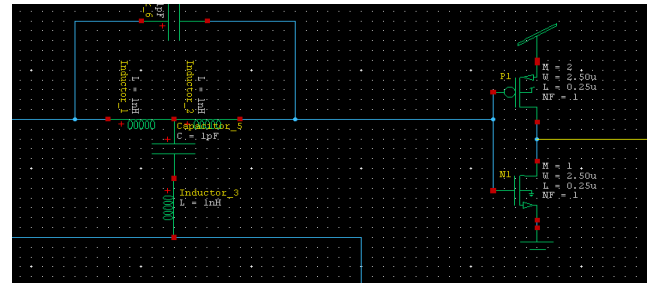

Fig. 3 Delay Equalizer

Whenever the clock is high the input is transferred to the output. The output from the latch is given to the 0 to 7 bit LSB DAC; the least bits are converted from digital to analog form. Similarly the most significant bits are given to the multiplexer. Mux is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. Multiplexers are mainly used to increase quantity of the information which will be sent over the network within a certain amount of time and bandwidth.
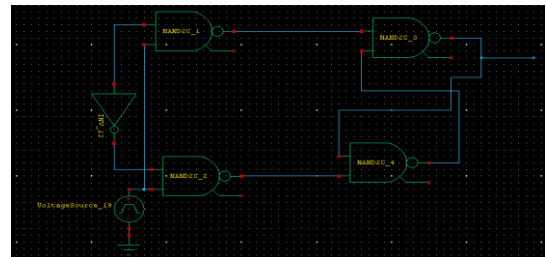

Fig. 4 latch

This also called a data selector implemented by using Boolean functions of multiple variables. The output from the mux is given to the latch, after that is given to the 8-bit MSB DAC. Here the most significant bits are converted to analog form.
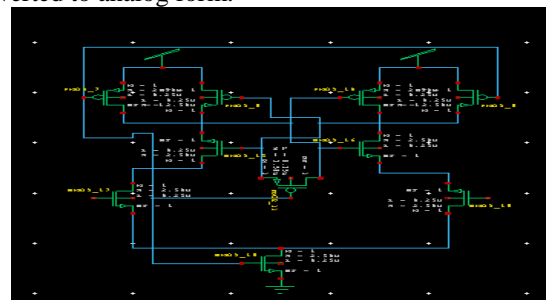

Fig.5 Comparator

The comparator is used to compare the two voltage levels represented in *Fig.5*. The sorting controller is used to arrange the unordered collection of elements into a monotonically increasing or decreasing order. The sorting controller is shown in *Fig.6*. It is an important operation including data mining, database, digital signal processing etc. To increase the storage capacity in terms of number of bits, have to use a group of flip-flop. The group of flip flop is known as address register. The n-bit register will consist of n number of flip-flop and it is capable of storing an n-bit word.
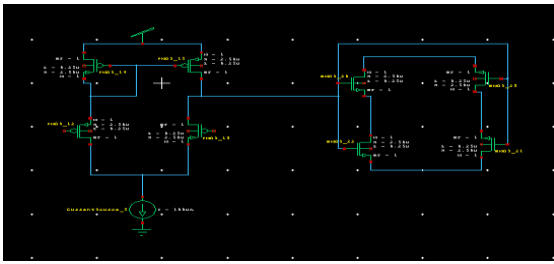
Special Issue - 2017

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
RTICCT - 2017 Conference Proceedings

Fig. 6 Sorting Controller

V.   EXPERIMENTAL RESULTS

The experiments are done on the binary weighted current steering DAC which are described in the tanner eda tool.
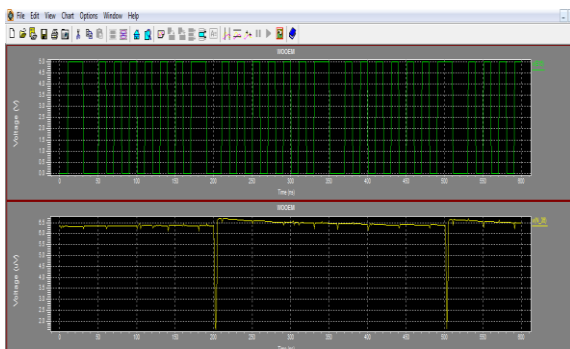

Fig. 7 Simulation results of DAC without using of OEM technique

The *Fig.7* describes the output of the DAC without OEM technique. In this figure the binary information are converted to analog but have a more glitches. The computational time of this conversion high, and also the consumption of power also increased.
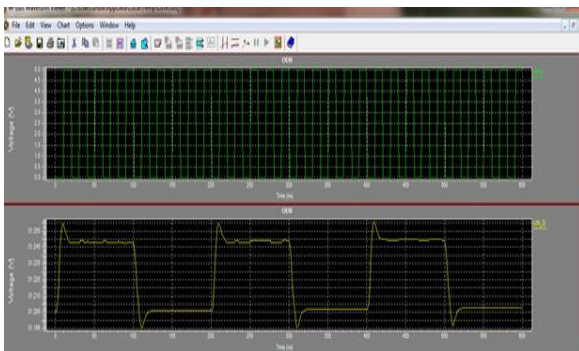

Fig. 8 Simulation results of DAC using OEM technique

The *Fig.8* shows the simulation results of binary weighted DAC using OEM technique. The input is given as binary information to the DAC. The DAC converts binary to analog form using the OEM technique getting desired output. Computational time of this conversion and power consumption also reduced.

VI.   PERFORMANCE ESTIMATED

TABLE I. PARAMETER CALCULATION BASED ON TANNER SIMULATION

SI.NO	Parameters	15-bit using OEM	15-bit using without OEM
1	Technology	0.45μm	0.45μm
2	Supply voltage	5v	5v
3	Power consumption	1.22w	3.54w
4	Computational time	5.96ns	6.18ms

The parameters are estimated as represented in Table. I. The values are calculated help of Tanner 0.45μm technology. Obtaining better results using OEM compared to normal binary weighted DAC. Power, computational time, resolution are the limitation of DAC; however using this concept we overcome these limitations.

VII.   CONCLSION

Using OEM technique a design of 15-bit binary weighted current steering DAC has proposed. The OEM technique selectively converts the unary weighted array to binary weighted array achieving system level matching without mismatch population. The new matching technique only demands the component orders, thus requires the comparator and other digital circuitry. Element mismatch are reduced in order to improve the performance of the DAC was obtained. The occurring glitches of output is lower than the without OEM technique. Less power, speed, circuit complexity, mismatches are the limitations of DAC. Overcoming these limitations my design with OEM technique was proposed. In proposed design of DAC has a less power, high resolution, less device variability, and high resolution.

REFERENCES

[1]   A. Van den Bosch, M.A.F.Borremans, M.S.J.Steyaert, and W.Sansen, "A 10-bit 1-Gsamples/s Nyquist current-steering CMOS D/A converter," *IEEE J. Solid-state Circuits*, vol. 36, no. 3, pp.315-324, Mar.2001.

[2]   Fang-Ting Chou. Chia- Min Chen. Chung- Chih Hung, "A low-glitch binary-weighted DAC with delay compensation scheme," in *springer Analog Integr Circ Sig Process,* published online: Feb 2014.

[3]   J. Huang, Y. He, Y. Liu, and H. Yang,"A 10-bit 200-MHz CMOS video DAC for HDTV applications," *Analog Integr. Circuits Signal process*, vol. 52, no. 3, pp.133-138 Sep.2007.

[4]   Niklas U. Andersson,K. Ola Andersson, Mark Vesterbacka and J Jacob Wikner, "Models and implementation of a Dynamic element matching DAC," *Analog integrated circuits and signal processing*, vol.34, issue 1, Jan 2003.

[5]   Peijun Wang and Nan Sun, "A Random DEM Technique with Minimal Element Transition Rate for High-Speed DACs" in *IEEE*, 2014.

[6]   Peiman Aliparast.,et al "A 12-bit 1-Gsamples/s Nyquist current-steering DAC in 0.35 μm CMOS for wireless transmitter," circuits and systems,2011,2,74-84.

[7]   Pelgrom, M., et al, "Matching properties of MOS transistors," *IEEE Journal of solid-state circuits*, 24(5), 1433-143, 1989.

[8]   Piyash K. Mathukar and Madan B. Mali, "CMOS 8-Bit Binary type current-steering DAC," International Journal of Embedded Systems and Applications (IJESA) Vol.2, No.3, Sep 2012.

Special Issue - 2017

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
RTICCT - 2017 Conference Proceedings

[9] Pooja J. Dani, Mr. Yash sharma, "Analysis and design of 10-bit current steering DAC in CMOS technology," vol-2 issue-3, *IJARIIE-ISSN (O)*-2395-4396.

[10] R.E. Radke, A.Eshraghi and T.S. Fiez, "A 14-bit current streeing DAC based upon rotated data weighted averaging," *IEEE J. Solid-state circuits*, vol.35,no.8,pp.1074-1084,Avg 2000.

[11] Seon, J.K, Ha, S.M., & Yoon, K.S, "An I/Q channel 12-bit 120 MS/s CMOS DAC with deglitch circuits," *Analog Integrated Circuits and Signal Processing,* 72(1), 65-74, 2012.

[12] Tao Chen, Georges G.E. Gielen, "The analysis and improvement of a current-steering DACs dynamic SFDR-1: the cell dependent delay differences," *IEEE transactions on circuits and systems-I: regular papers.* Vol.53,no.1, Jan.2006.

[13] W.-H. Tseng,J.-T. Wu, and Y.-C. Chu, "A CMOS 8-bit 1.6-GS/s DAC with digital random return-to-zero," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* Vol. 58, no. 1, p. 1-5, Jan. 2011.

[14] Y. Cong and R.L.Geiger, "A 1.5V 14-bit 100MS/s self-calibrated DAC,"*IEEE J. Solid-state circuits*, vol.38, no.12, pp.2051-2060, Dec 2003.

[15] Engel, S. Kuo, S. Rose, "A 14 b 3/6 GHz current-steering RF DAC in 0.18 μm CMOS with 66dB ACLR at 2.9GHz," *IEEE ISSCC Dig.Tech. Papers,* Feb. 2012, pp. 458-460.

[16] W. A. Lane and G. T. Wrixon, "The design of thin-film polysilicon resistors for analog IC applications," IEEE Trans. Electron Devices, vol.36, no. 4,pp. 738-744, Apr. 1989.

[17] J. B. Shyu, G. C. Temes, and F. Krummenacher, "Random error effects in matched MOS capacitors and current sources," IEEE J. Solid-state Circuits, vol. 19, no. 6, pp. 948-956, Dec. 1984.

[18] T. Zeng and D. Chen, "An order-statistics based matching strategy forcircuit components in data converters," IEEE Trans. Circuits Syst. I,Reg. Papers, vol. 60, no. 1, pp. 11 -24, Jan. 2013.

[19] J. Deveugele and M. S. J. Steyaert, "A 10-bit 250-MS/s binary-weighted current-steering DAC," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 320–329, Feb. 2006.

[20] M.-H. Shen, J.-H. Tsai, and P.-C. Huang, "Random swapping dynamic element matching technique for glitch energy minimization in current steering DAC," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 5, pp. 369–373, May 2010.