Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 05, May - 2017

Design of Array Multiplier using Mux Based Full Adder

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***Abstract*— Multiplier is one of the basic arithmetic units in digital signal processor. Multipliers play a major role in today's digital signal processing and various other applications. The first stage of multipliers involves partial products generation which is nothing but an array of AND gates. The partial products are then added to give the final results. In this paper an effort is made to design 8 bit array multiplier in 180nm technology. The array multipliers using different full adders have been designed, implemented & analyzed in standard gpdk180nm technology library using Cadence tool. And the performance parameters (area, delay and power) are compared among them.**

Keywords—Multiplier, Full adder, Partial Products, Cadence.

I. INTRODUCTION

In recent years, low power, high speed and less area are the key parameters in the design of modern VLSI circuits. In ALU multipliers plays a major role. In the design of DSP structures multipliers is a important functional unit. The array multiplier partial products are generated by anding of multiplier and multiplicand bits. In second stage full adders and half adders has been used for the reduction of generated partial products. In third stage by addition of two rows using fast carry adders.

In recent years a lot of research work has been carried out to reduce the complexity of the multiplier, a novel method is used for reduction of complexity of array multiplier in terms of number of half adders, further improvement is carried out by incorporating one more half adder to the right most columns, results in a drastic area reduction. In addition to that, Booth encoding approach along with compressor has been used to reduce the area as well as latency. Furthermore, the conventional half adder and full adder in the second stage are replaced with XOR-XNOR based 3:2, 4:2 and 5:2 compressors which bring an increase in speed of operation. An efficient approach is proposed by estimating the power of each stage of the reduction tree using probabilistic gate-level power estimator. Due to that the switching power is reduced by optimizing the transitions activity in the partial product tree. The reordering of partial products is employed in such a way so as to reduce the switching activity which leads to reduction in power. A modified full adder using 4:1 multiplexers is used in the reduction phase to reduce the power and full adder is designed using six 2:1 multiplexers. This paper mainly deals with the replacement of full adders with different designs and comparing all the parameters like delay, area and speed.

II. ARRAY MULTIPLIER

The conventional array multiplier uses carry save addition to add the products. In the carry save addition method, the first row will be either half adders or full adders .If the first row of the partial products is implemented with full adders, Cin will be considered 0.

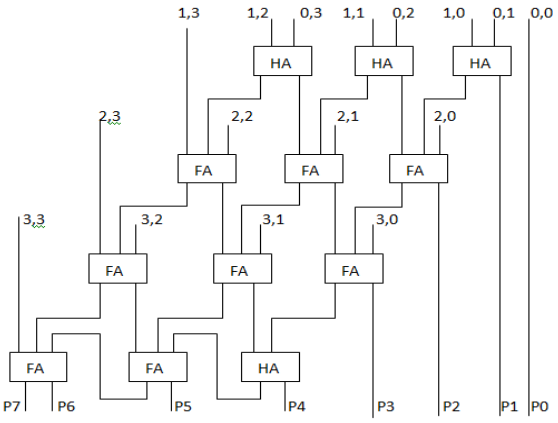

Fig .1. Array Multiplier

Then the carries of each full adder can be diagonally forwarded to the next row of the adder. The resulting multiplier is said to be carry save array multiplier as the carry bits are not immediately added but rather saved for the next stage of addition.

Array multiplier is an efficient layout of a combinational multiplier. Multiplication of two binary number can be obtained with one micro-operation by using a combinational circuit that forms the product bit all at once thus making it a fast way of multiplying two numbers since only delay is the time for the signals to propagate through the gates that forms the multiplication array. Array multiplier has regular structure, therefore layout becomes simple and it occupies less area since it has small size. It is a multiplication method in which an array of identical cells generates new partial product and accumulation of it at the same time.

A. Conventional Full Adder

A full adder can be implemented in many different ways such as with a custom transistor-level circuit or composed of other gates. If A and B are two inputs and Cin is

International Journal of Engineering Research & Technology (IJERT)
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the carry input the expressions for SUM and Carry are as follows:

SUM = A.B.Cin + A.B.Cin + A.B.Cin + A.B.Cin (1)
SUM = Cin (A.B+A.B) + Cin (A.B+A.B) (2)
=A (XOR) B (XOR) Cin (3)
CARRY = A.B + A. Cin + B. Cin (4)
CARRY = A.B + Cin (A+B) (5)

This implementation uses a 3-input XOR gate, 2 AND gates and one OR gate. A transistor level implementation uses a total of 42 transistors.

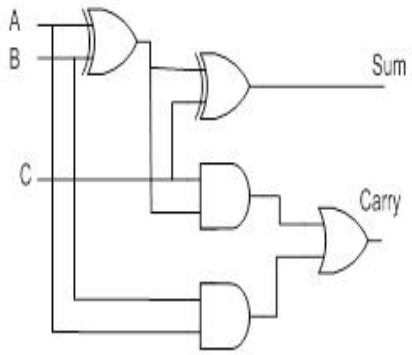


Fig . 2. Conventional Full Adder

B. Full Adder Using 6 MUX

A full adder can be implemented using six 2:1 multiplexers. A transistor level implementation uses a total of 22 transistors which reduces area compared to conventional approach.

C. Full Adder Using 4:1 MUX

The conventional full adder in array multiplier can be replaced with a MUX based full adder. In MUX based full adder the full adder is implemented using 4:1 multiplexers. This implementation uses a two 4:1 MUX and one NOT gate. A transistor level implementation uses a total of 20 transistors which reduces area compared to conventional approach.

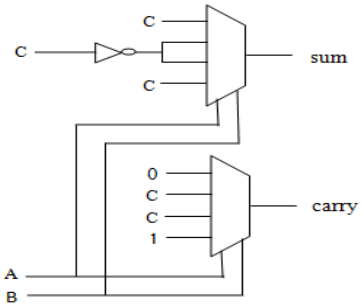


Fig .3 Full Adder using 4:1 MUX

D. *Full Adder Using 2:1 MUX*

In MUX based full adder can also be implemented using 2:1 multiplexers and one XOR gate. A transistor level implementation uses a total of 22 transistors which reduces area compared to conventional approach.

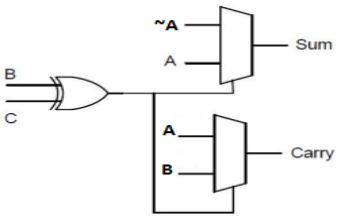


Fig .4 Full Adder using 2:1 MUX

III.IMPLEMENTATION & RESULTS

In this chapter implementation and results of 8 bit array multiplier in 180nm technology using Cadence tool are discussed. The array multiplier using different full adders have been designed, implemented & analyzed along with their performance parameters.

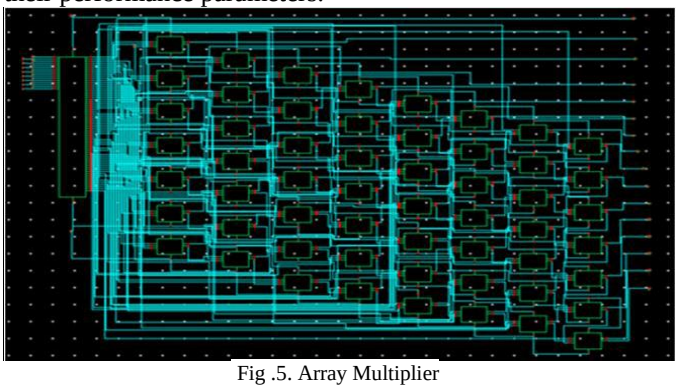


Fig .5. Array Multiplier

The above Fig.5 depicts the schematic of Array Multiplier (using Cadence Virtuoso tool) which is used for multiplying two 8 bit binary numbers.

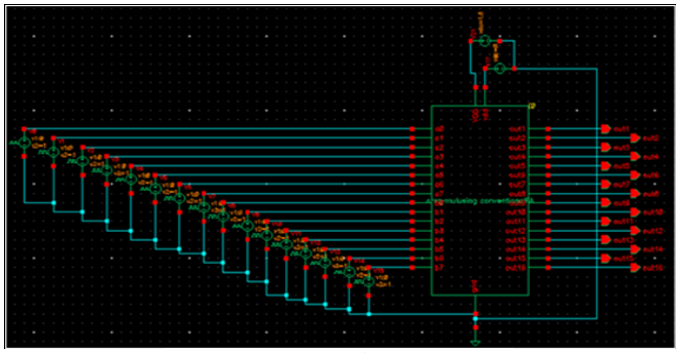


Fig.6 Test Schematic of Array Multiplier

The above Fig.6 depicts the test schematic of Array Multiplier which is used for multiplying two 8 bit binary numbers.

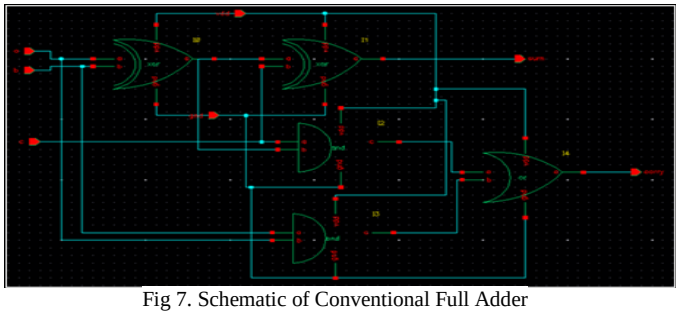


Fig 7. Schematic of Conventional Full Adder

The above Fig.7 depicts the schematic of Full adder(Conventional).

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 05, May - 2017

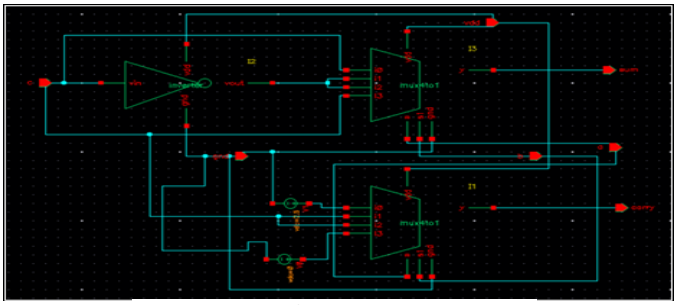


Fig 8 .Schematic of Full Adder using 4:1 MUX

The above Fig.8 depicts the schematic of Full adder using 4:1 MUX.

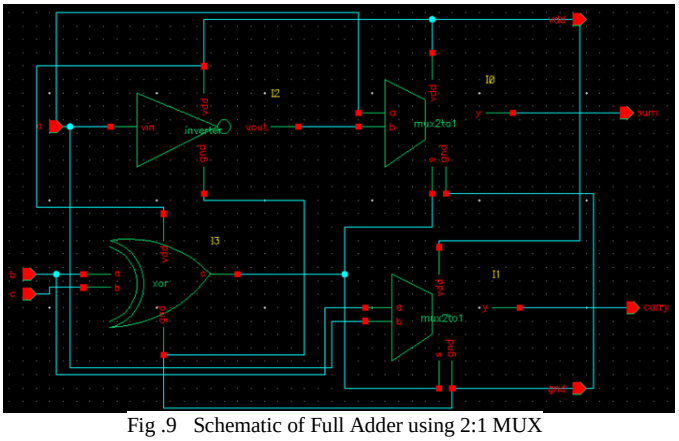
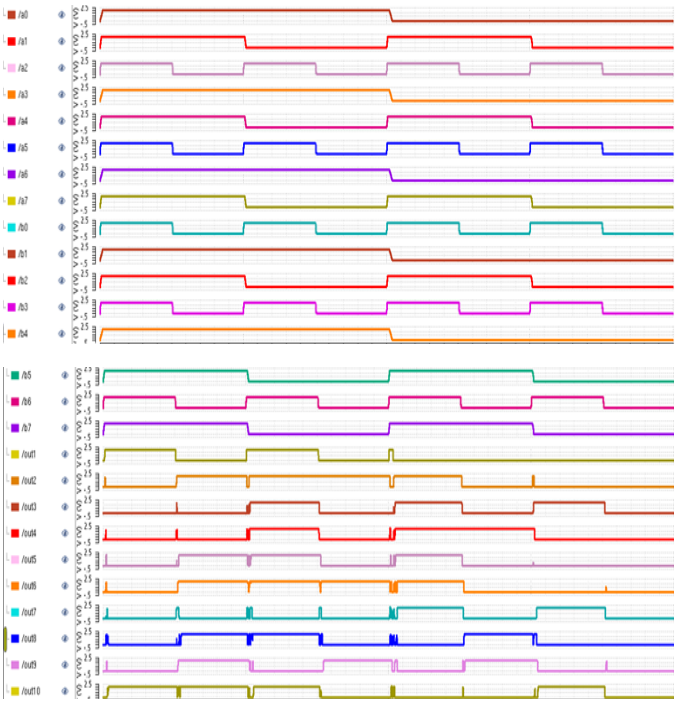


Fig .9 Schematic of Full Adder using 2:1 MUX

The above Fig.9.depicts the schematic of Full adder using 2:1 MUX.



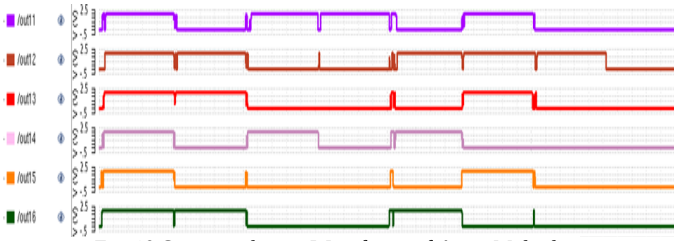


Fig .10 Output and input Waveforms of Array Multiplier

The Fig .10 depicts simulation results of 8 bit Array Multiplier.

A. *Comparison of Delay, Area & Power for Different Full Adders*

TABLE1

	CONVENTIONAL FULL ADDER	FULL ADDER USING 4:1 MUX	FULL ADDER USING 2:1 MUX
DELAY (ns)	45.16	40.53	20.32
AREA (no.of transistors)	42	20	22
POWER (uW)	442.1	62.44	96.67

B. *Comparison Of Delay, Area & Power For Array Multipliers Using Different Full Adders*

TABLE 2

	ARRAY MULTIPLIER USING CONVENTIONAL FULL ADDER	ARRAY MULTIPLIER USING FULL ADDER USING 4:1 MUX	ARRAY MULTIPLIER USING FULL ADDER USING 2:1 MUX
DELAY (ns)	49.98	49.09	49.57
AREA (no.of transistors)	2944	1536	1664
POWER (mW)	2.197	5.592	1.218

CONCLUSION

The proposed and the existing multiplier designs are developed using Verilog HDL for 8 and 16 bits, respectively. The schematics are designed for 8 bit array multiplier using CADENCE tool in 180nm technology. The schematic for conventional full adder, full adder using six 2:1 mux ,full adder using 4:1 mux and full adder using 2:1 mux ,is designed. The performance parameters are compared by implementing array multipliers using different full adders. The proposed work is operated with analog input voltage of 0 to 1v, supply voltage 1.8v. As the proposed designs have proven to work efficiently in terms of various performance parameters thus; the more effective results are expected to be obtained while incorporating these circuits to implement other complex systems in the field of low power VLSI design. In the future, the 8 bit array multiplier using 10T GDI based full adder can be optimized for low power applications. Further, the improved multiplier can also be used for designing the low power DSP applications.

International Journal of Engineering Research & Technology (IJERT)
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