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Design of an Efficient Phase Frequency Detector for a Digital Phase Locked Loop

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***Abstract*— This paper outlines the design and analysis of the digital phase locked loop (DPLL). It also demonstrates the feasibility of the DPLL in the various applications. The proposed phase frequency detector (PFD) uses 26 transistors analogous to the conventional PFD which uses 54 transistors. It has been observed that the lock in time of the DPLL is very less. In addition to these, an overview on the designing of the charge pump and loop filter is also discussed. Prototype has been designed in Cadence virtuoso environment and implemented using GPDK180 library of 180 nm technology with a supply voltage of 1.8 V.**

Keywords*— Candence, Charge Pump , Clock Recovery Circuit, DPLL, Frequency Divider, Frequency Synthesizer, PFD, TSPC, VCO.

I. INTRODUCTION

The Phase Locked Loop has many applications in various fields. In communication system the PLL is used for clock and data recovery at the receiver side and also in many modulation techniques. In digital IC's PLL is used for synchronization, to reduce clock skew and clock generation. In SoC, PLL occupies 50 to 60% area so there is necessity of designing an efficient PLL which occupies less area, high lock range with less lock time..

The PLL is a negative feedback circuit. PLL circuit consists of a phase detector, charge pump, loop filter and voltage controlled oscillator (VCO). The PLL is classified into three types based on the implementation of the different blocks in it.

- Analog PLL

The PLL introduced in 1930's was an analog PLL in which all the blocks are implemented in analog. The multiplier is used as the phase detector in the analog PLL. The analog PLL finds applications in the frequency modulation and demodulation techniques.

- Digital PLL (DPLL)

The phase detector is implemented in the digital class and the rest of the blocks are implemented in the analog class. The two D flip flops connected to each other with the reset path, which is known as phase frequency detector and XOR gate, RS latch can also be used as phase detectors in the digital PLL. Depending on the type of application the phase detectors are chosen in the digital PLL. For the clock and data recovery, XOR gate is used as the phase detector. For frequency synthesis and clock synchronization, phase frequency detector (PFD) is used as the phase detector in the digital PLL [1-2]. RS latch is used as the phase detector in digital PLL for the de-skewing purpose.

To use DPLL as the frequency synthesizer connect the divider circuit in the feedback path. The output of the VCO is given as the input to the divider circuit which is in the feedback path and the output of the divider circuit is given as one of the input of the phase detector.

- ALL DIGITAL PLL (ADPLL)

The ADPLL consists of all the blocks in the digital class. The loop filter is replaced with the digital filter and VCO with the numerically controlled oscillator (NCO).

II. OPERATION OF DPLL

The block diagram of the DPLL is shown in the Fig. 1. The reference clock is given as one of the inputs to the PFD which generates two output signals UP and DOWN. These are given as the inputs to the charge pump. The output of the charge pump is given to the loop filter which generates the required voltage which is fed to the VCO. The output of the VCO is given as another input to the PFD. When the input signal and VCO out signal are having same phase and frequency the PLL locks the signal.

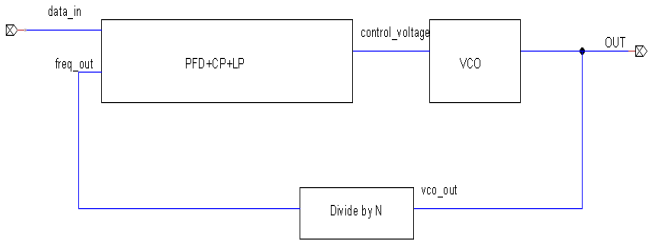

Fig. 1. Block diagram of DPLL.

Desired PLL is expected with higher lock range, less lock time and tolerable phase noise [2-4]. The PLL enters into lock mode when the input frequency and the output frequency is same and it is known as lock in range.

$$Lock\ in\ range = 2\varsigma\omega_n \quad (1)$$

Where, ς is damping factor

ω_n is the natural frequency

The stability of the PLL depends on the damping factor and the bandwidth of the PLL depends on the natural frequency. The desirable value of the damping factor ranges between 0.45 to 1. Sometimes PLL may not enter into lock mode this is due to the output of the divider circuit with glitches which misleads the PFD.

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To design an efficient PLL each block has to be designed with care. The designing of each block is described in the following sections.

III. PHASE FREQUENCY DETECTOR

The PFD detects the phase and frequency difference between the two inputs given to it. The first input is the reference clock signal and the second input is the VCO output. The PFD generates two outputs, namely UP and DOWN. The UP signal is generated when the rising edge of the reference clock is leading the other feedback signal. The DOWN signal is generated when the feedback signal rising edge is leading the rising edge of the reference clock.

When the UP signal is generated this specifies that the VCO out signal is slower than the clock so the input of the VCO is tuned in such a way that it generates the high frequency output. After many of the analogous iterations the two signals are matched and PLL enters into lock mode.

Similarly, when the DOWN signal is generated this implies that the VCO out is faster than the clock and it should be slowed down. This can be done by properly tuning the VCO.

The efficient PFD should be capable of detecting the smallest phase errors [5]. The small phase error is known as the blind zone or dead zone. The conventional PFD uses 54 transistors. The power consumption is more while operating at the higher frequencies.

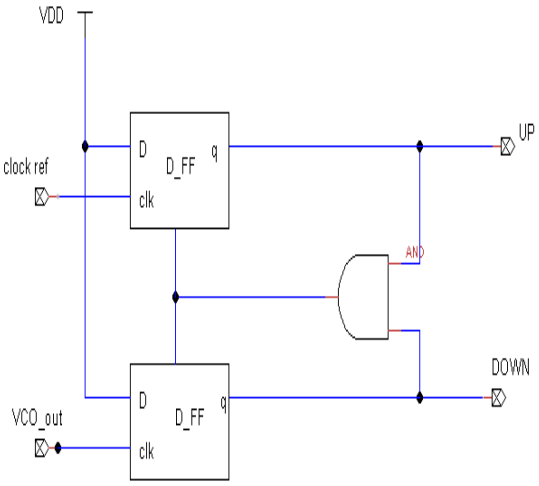

Fig. 2. Phase frequency detector (PFD).

The Fig. 2 shows the block diagram of the PFD. The conventional PFD uses 54 transistors. The proposed design uses only 22 transistors. The D flip flop is implemented using true single phase clocking (TSPC) logic.

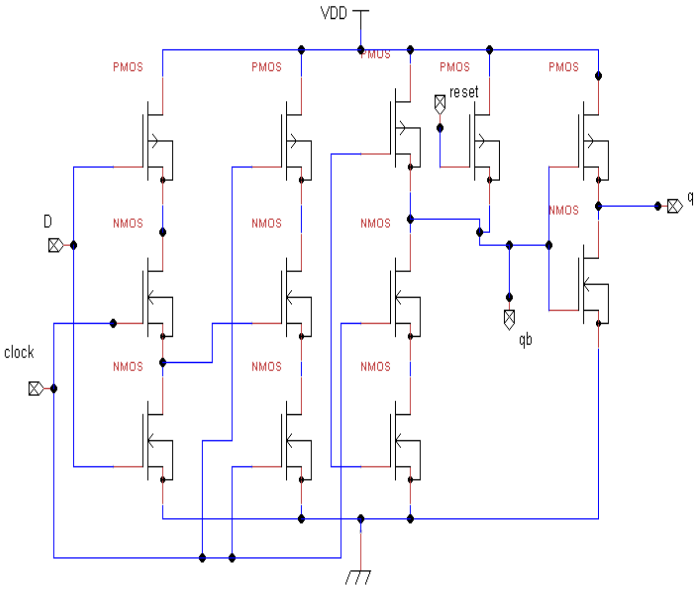

Fig. 3. D flip flop using TSPC logic.

The implementation of the D flip flop in true single phase clocking (TSPC) logic is shown in the Fig. 3. The reset path is designed using AND gate in pass transistor logic.

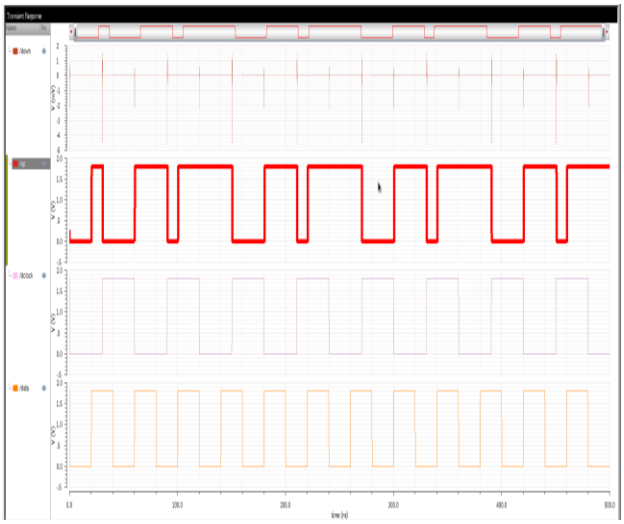

Fig. 4. Simulated result of the proposed PFD.

The simulation output of the PFD is shown in the Fig. 4. In the graph, the rising edge of the clock reference is leading the feedback signal so, UP signal is generated. The pulse is generated when there is a phase or frequency difference between the two signals.

IV. CHARGE PUMP

The two outputs of the PFD are given as the input to the charge pump which gives a single output and fed as the input to the loop filter. There are two methods to obtain the single output. In the first method UP signal output is given to the inverter and the output of the inverter is given as the input to the PMOS. The DOWN signal is directly fed to the NMOS transistor. When UP and DOWN are low the two transistors are turned off. If the UP IS high then PMOS is turned ON and vice versa. This method is known as tri state

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output. The drawback of tri state output method is, the PMOS transistor output gets affected by varying power supply. The output of the PFD using tri state method is,

$$V_{PDtri} = K_{PDtri} \times \Delta\emptyset \quad (2)$$

Where, K_{PDtri} is the gain and $\Delta\varphi$ is the phase difference

$$K_{PDtri} = \frac{V_{DD}}{2} \ (volts/radians) \quad (3)$$

The second method is known as the charge pump. The PFD output using charge pump configuration is independent of the supply voltage. The current sources are connected to the PMOS and NMOS because current sources can be made insensitive to the supply voltage variations. The Fig. 5 shows the charge pump along with loop filter. The output of the PFD for the charge pump configuration is,

$$I_{PDI} = K_{PDI} \times \Delta\emptyset \quad (4)$$

Where ,

$$K_{PDI} = \frac{I_{pump}}{2\pi} \ (amps/radians) \quad (5)$$

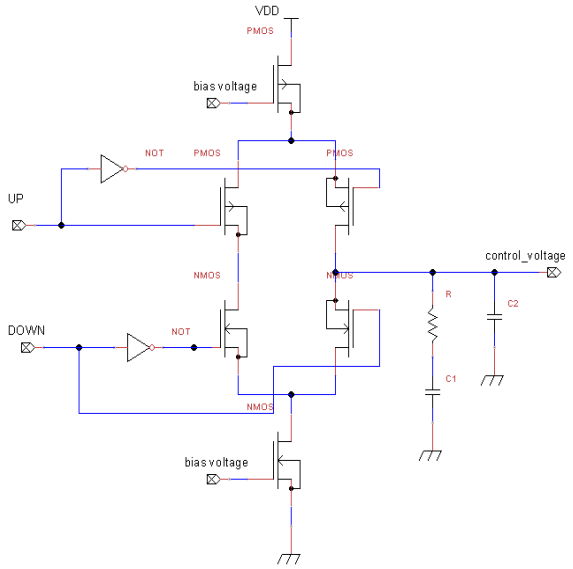

Fig. 5. Charge pump implementation along with loop filter.

The output of the above mentioned configurations should be independent of the supply voltage otherwise the control voltage generated by the loop filter gets affected and unable to tune the VCO.

V. LOOP FILTER

In tri state output configurations the simple RC passive loop filter is used. The zero is added in the path to make the passive filter as the passive lag filter. Because of the addition of the zero the pole of the loop filter is made small which in turn increases the VCO gain and desired damping factor can be achieved.

For the fast variations the loop filter acts like resistive divider. This allows the loop filter to track fast variations between the rising edges of the signals. The loop filter for the tri state configuration is shown in the Fig. 6.

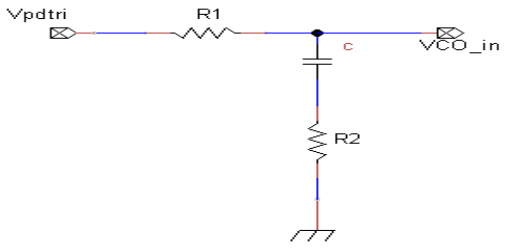

Fig. 6. Loop filter for tri sate configuration.

$$R_2C = 2\varsigma\,\omega_n \quad (6)$$

$$2\varsigma\omega_n = K_{PDtri}K_{VCO}R_2C \div N(R_1 + R_2)C \quad (7)$$

Where K_{vco} is the gain of the VCO

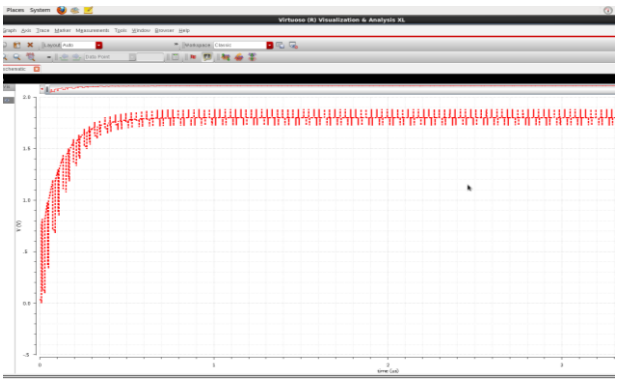

Fig. 7. Simulated result of the tri state.

The Fig. 7 shows the output of the loop filter with tri state configuration. The true state configuration is not preferable because the it varies with the voltage variations and take long time to attain the steady state. When the loop filter attains the steady state then only the PLL enters into the lock mode.

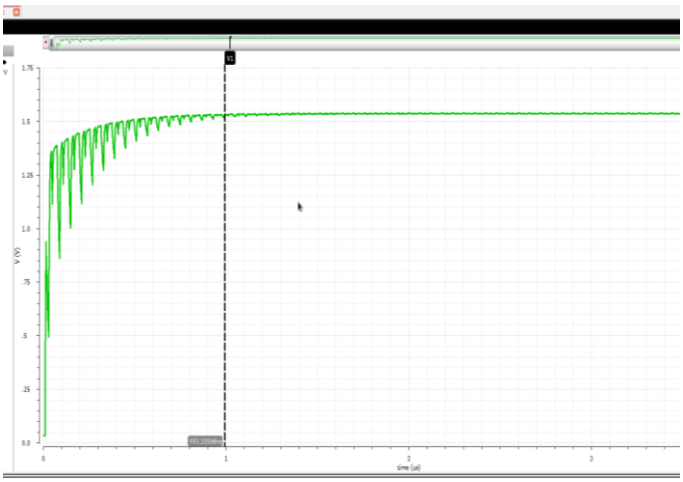

Fig. 8. Simulated output of the charge pump.

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The Fig. 8 shows the output of the loop filter with the charge pump configuration.In the Fig. 4 the loop filter for charge pump configuration is shown. The charge pump is preferred over tri state configuration the because the output of the charge pump is independent of the supply variations. The output of the loop filter attains the steady state in less time, which means that the PLL lock in time is very less compared to the tri state configuration.

The equations of the loop filter for the charge pump configuration are,

$$C_1 = {K_{PDI} K_{VCO}}/{N \omega_n^2} \quad (8)$$

$$C_2 = {C_1}/{10} \quad (9)$$

$$R = {2\varsigma}/{\omega_n C_1} \quad (10)$$

VI. VOLTAGE CONTROLLED OSCILLATOR

The current starved VCO is used in the designing of the DPLL. The current starved VCO is shown in the Fig. 9. For odd number of the inverter stages the VCO output is obtained. The input given to the VCO is the output from the loop filter. The characteristic of the VCO is the output frequency is linearly proportional to the input frequency.

The small load capacitance should be attached to the VCO otherwise large load capacitance can kill the oscillations at the output. The loop filter should generate the controlled voltage according to the requirement.

If the UP signal is generated by the PFD with the charge pump configuration, then the loop filter generates the increasing control voltage which in turn leads to the higher frequency VCO output signal. Because of the high frequency VCO output the feedback signal is made faster and matched with the reference clock. When both are same, PLL enters into lock mode.

If the DOWN signal is generated by the PFD with charge pump, then the loop filter output generates decreasing control voltage. The VCO generates the low frequency output signal that means the feedback signal is slowed down and matched with the reference clock.

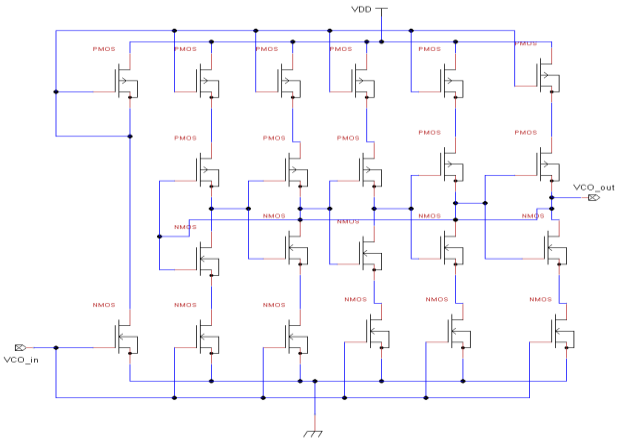

Fig. 9. Current starved VCO.

The input to the VCO is known as the control voltage

$$VCO_{in} = K_F \times I_{PDI} \quad (11)$$

Where,

K_F is gain of the loop filter

I_{PDI} is the output of the PFD with charge pump.

The gain of the VCO is,

$$K_{VCO} = {Freq_{max} - Freq_{min}}/{V_{max} - V_{min}} \quad (12)$$

Where,

$V_{max} = V_{DD}$ at maximum frequency

$VCO_{in} = V_{THN}$ when $Freq_{min} = 0$

The $Freq_{max}$ is determined from the drain current when

$$VCO_{in} = V_{DD} \quad (13)$$

The oscillation frequency of the VCO depends on the input of the VCO

$$freq_{oscillation} = \frac{1}{N \times C_{total} \times V_{DD}} \quad (14)$$

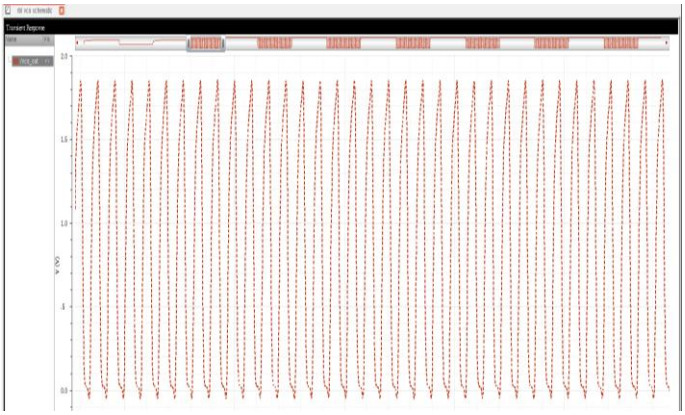

Fig. 10. Simulated result of the current starved VCO.

The output of the current starved VCO with 5 inverter stages is shown in the Fig. 10.

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VII. SIMULATION RESULTS OF DPLL

The output of the DPLL is shown in the Fig. 11. When the loop filter output reaches the steady state that specifies the input signals are in the same phase and frequency and the DPLL enters the lock mode.

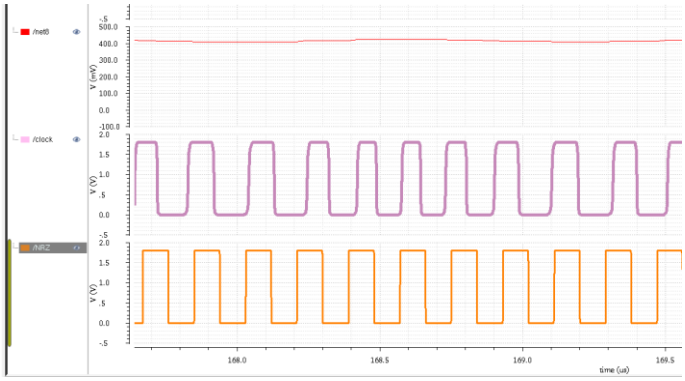

Fig. 11. Simulated result of DPLL.

The lock time of the DPLL achieved is 998.9ns and the average power estimation is 2.272mW.

VIII. APPLICATIONS

The above designed DPLL is implemented in the two applications. The DPLL is used to design the clock recovery circuit at the receiver side. The clock is generated from the data using clock recovery circuit [6-9]. The clock recovery circuit consists of the edge detector and the DPLL. The edge detector circuit is used to in clock recovery circuit.

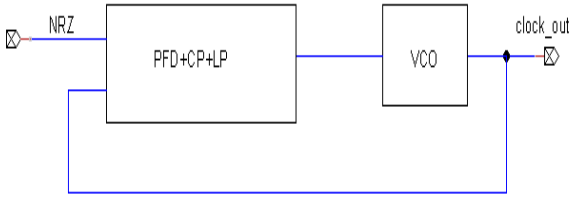

Fig. 12. Block diagram of the clock recvovery circuit.

The block diagram of the clock recovery circuit is shown in the Fig. 12. In this design the clock recovery circuit is designed without using an edge detector because DPLL with PFD generates the pulse at the rising edge of the leading signal unlike XOR as phase detector. The DPLL generates the clock when the input signal and feedback signal are same in phase.

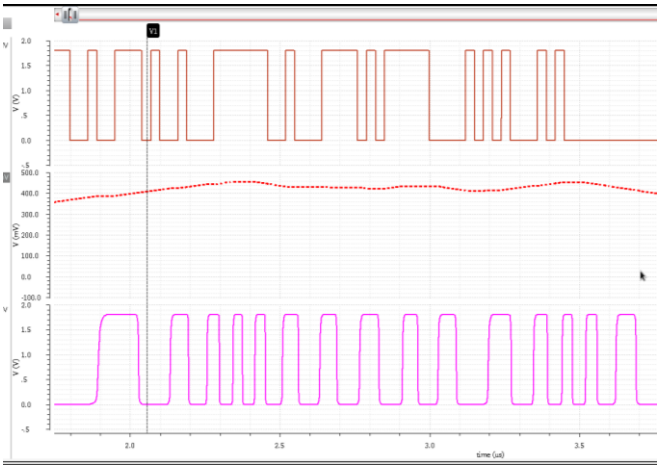

Fig. 13. Output of the clock recovery circuit for NRZ.

The Fig. 13. Shows the simulation result of the clock recovery circuit. The non return to zero (NRZ) is given as the input bit pattern to the clock recovery circuit. From the NRZ bit pattern the clock is generated.

The most popular application of the DPLL is a frequency synthesizer [10-12]. The block diagram of the frequency synthesizer is shown in the Fig. 14. To achieve the output frequency double that of the input frequency, use the divide by 2 circuit in the feedback path. The VCO output is given as the input to the divider circuit which divides the frequency by 2 and this is fed as the input to the PFD which performs iterations to match the two signals. When the two signals are same in phase and frequency, DPLL enters into the lock mode and the output frequency is twice that of the input frequency.

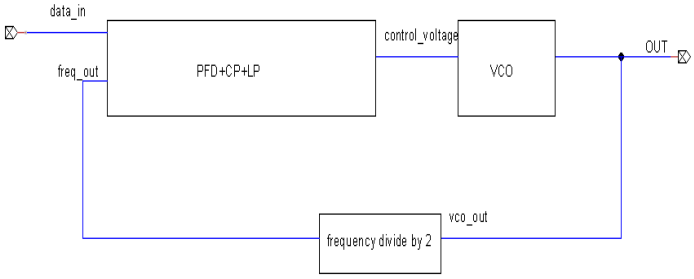

Fig. 14. Block diagram of frequency synthesizer.

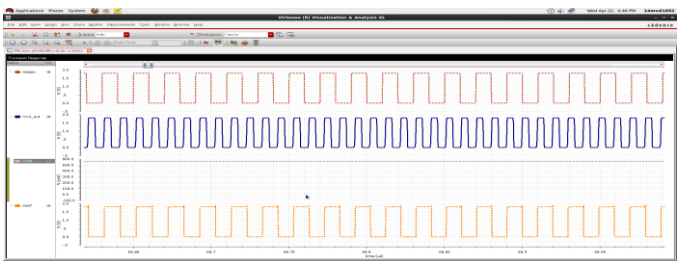

Fig. 15. Simulated result of frequency synthesizer.

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The Fig. 15 shows the simulation result of the frequency synthesizer. The output frequency of the VCO is divided by 2 and fed to the PFD. To error signal is given to the loop filter which generates the required control voltage and given to the VCO. Therefore, the output of the DPLL is twice that of the input frequency. In the divider circuit, D flip flop is implemented in TSPC logic.

IX. CONCLUSION

The comparison of conventional and proposed PFD is shown in the table.1. Lock in time of the DPLL is 998.9ns which is far better than the conventional DPLL. The average power estimation of the proposed PFD is 28.65uW which is 40% lesser than the conventional PFD. The DPLL with proposed PFD is used in the designing of the clock recovery circuit and the frequency synthesizer.

Factor	Conventional PFD	Proposed PFD
Number of transistors used	54	26
Power	40.2 μW	28.65 μW

Table1. Comparison of conventional and proposed PFD

X. FUTURE WORK

To design a VCO by proper transistor sizing, the transistor sizing can be achieved by using optimization techniques.

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