Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 11 Issue 05, May-2022

Design of an 8*8 SRAM Array in 18nm FINFET Technology in Cadence Virtuoso

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***Abstract*— Static Random-Access Memory has become a common component of any ASIC, System-On-Chip (SoC), or other micro-architecture. SRAM is utilized as a CPU interface, and it exchanges DRAM from the system since it uses relatively low power. Low-power SRAM is critical. since it consumes less power and takes up less space. SRAM is used in numerous applications to improve throughput. This paper aims to design an 8 by 8 SRAM array cell using FinFET sub-18nm technology as SRAM is made using CMOS but with FinFET, we have advantages such as low power consumption, operation at low voltage, and higher operating speed. In this paper parameters such as leakage current, power consumption, and access time are compared, in this paper many components, including sensing amplifiers, decoders, precharge, write circuits, and 8x 8 cells, have been developed, constructed, and evaluated using Cadence Virtuoso.**

Keywords*— SRAM, CMOS, FinFET, read, write, leakage current, leakage power.

I. INTRODUCTION

Handheld wireless computers and consumer gadgets are becoming more common as current communications and signal processing technologies advance. SOC designs have allowed for significant cost and form factor savings, in part because they combine critical memory components with digital computation and signal processing circuitry on a single chip that takes approximately 70% of the area. SRAM is a key component that makes up a bigger portion of the chip die, and for SOC designs, digital circuit requirements influence technology and system design decisions.

With the widespread usage of SRAM in mobile's, SOC's, and VLSI circuits, demand for SRAM is rising. SRAM is an important component for cache memory, which is a type of memory that sits between the main memory (typically DRAM – Dynamic Random Access Memory) and the processor in the memory hierarchy. They're made to run at the same or very near to the same CPU frequency. Due to its fast speed and less consumption of power, it is also used in computers, engineering workstations, and memory in electronic devices such as smartphones. SRAMs must be not only quick but also reliable, i.e., stable and resilient, for the system to function effectively.

Although it does not need to be updated as regularly as DRAM, SRAM requires continual power to hold data.

In SRAM, rather than being a capacitor storing the charge, the transistor acts as a switch, with one position indicating 1 and the other representing 0. Static RAM, in contrast to dynamic RAM, which requires just one transistor per bit, requires several transistors to keep one bit of data. As a result, SRAM chips are larger and cost more than DRAM chips of equal capacity.

SRAM, on the other side, is far faster than DRAM and uses significantly less power. Static RAM is usually used as cache memory within a computer's CPU due to price and speed differences.

The basic 8T SRAM cell is used to build the SRAM array. The goal of this study is to use Schematic Editor Virtuoso to suggest a design for 64-bit memory. Row Decoder, Pre-charge Circuit, Driver Circuit, Bit Cell, and Sense Amplifier are examples of peripheral circuits that must be developed and implemented. The project's goal is to develop the memory and show that it can write and read data successfully.

Using the cadence virtuoso tool to create an 8*8 array. It's a set of tools for designing fully-custom integrated circuits that include schematic entry, behavioral modeling, circuit simulation, custom layout, physical verification, extraction, and back-annotation. The most popular designs are analogue, mixed-signal, RF, and standard-cell, but memory and FPGA designs are also prevalent.

II. ARRAY LOGIC

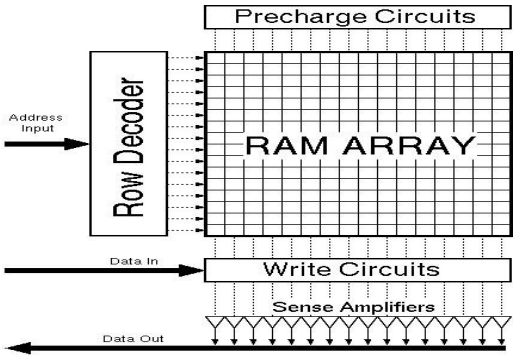

Fig 1. Block diagram

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 11 Issue 05, May-2022

The above fig of the SRAM array consists of SRAM Cell, Precharge circuit, Write Driver Circuitry Sense Amplifier Decoders Every block can be described as follows:

III. PROPOSED 8T SRAM CELL IN FINFET 18NM

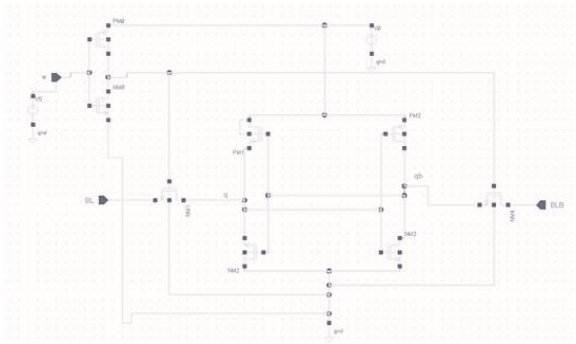

Fig 2. proposed 8T SRAM cell

As seen in Fig 2, the proposed design consists of eight transistors, five of which are n-type and three of which are p-type, N_1-N_5 is N1HVT and P_1-P_ 3 are P1HVT, P_1-P_2 and N_1-N_2 form a latch to store one bit of data, N_3-N_4 are access transistors that connect the cell inner nodes q and q b and also connects to bit lines and the node voltage
C 1 is controlled by this inverter circuit P_3 and N_5, and the gates of P_3 and N_5 establish a word line used to activate the cell, P_1 and P_2 are linked to a dynamic cell source(c_s) that is increased to a greater value during read, resulting in a high noise margin.

A. Read Operation

The read operation is nothing more than reading the value stored in the latch, which is nothing more than a circuit made up of N_1 and N_2 as well as P_1 and P_2 transistors. Cell Source is raised from VDD_1 to VDD_2 to begin the read procedure. To enhance the cell's noise margin during read operations, VDD_2 should be higher than VDD_1. Simultaneously, the word line is pushed low, because it is connected to the inverter circuit, this makes to drives node C to VDD_1, which activates access transistors N_3 and N_4 transistors. After turning on N_3 and N_4 transistors used to read the cell data through bit_lines, the circuit operates similarly to a standard 6T SRAM.

B. Write Operation

The write operation is nothing more than writing the value stored in the latch, At the beginning of a write cycle, the logic to be written is kept on the bit_lines. To place a value 0 on the bit_line, set 0 and on the bit_linebar to 1, and to place a value 1 on the bit_line, set 1 and on the bit_linebar to 0.
The write operation in the recommended architecture is relatively easier than the read process. The C_S line is asserted to VDD_1 to start the write operation while the Word line is pushed down. Meanwhile, the one-bit line is pulled to the gnd, while the other is retained at VDD_1. When node C is linked to VDD_1, both N_1 and N_2 turn on, and input data is written into memory in the same manner as standard 6T SRAM.

IV. PRECHARGE CIRCUIT

Well within SRAM cell, the pre-charge circuit is among the most important components that is regularly used. The bit_line and bit_line bars are charged to Vdd=1v via the pre-charge.

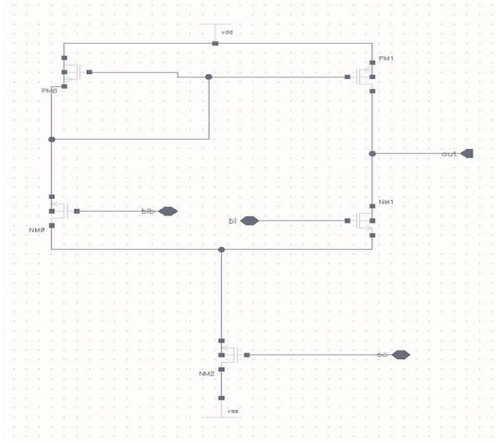

Fig 3. Schematic of Pre-Charge

The precharge circuit is by far the most important component in the array. It is made up of 3 PMOS transistors. For revitalization, two larger transistors are used, and for balanced, the smallest single transistor is used. The precharge circuit's primary function is to charge both bit lines to VDD_1 = 1 V before read and write operations. When both write and read operations are not in progress, the pre-charge circuit is utilized to charge the bit_lines. When "Pre" is logic "0," "VDD_1" charges both bit_lines, bit_line, and bit_linebar to high. Here, pin “Pre” controls the charging of bit lines, Because of the read and write operations, the precharge circuit allows the bit _lines to be stimulated and lifted at each occurrence.

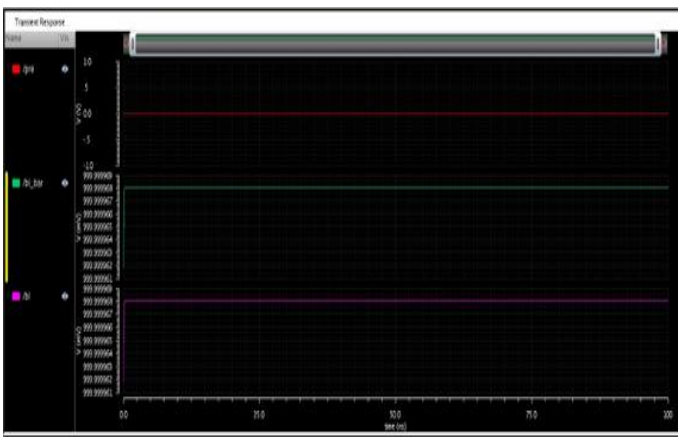

Fig 4. Waveform for Pre-Charge

It is used to charge the bit lines while both write and read operations are not in process. Fig 4 illustrates this. When "Pre" is set to logic "0," "Vdd" charges both the bit lines bit_line and bit line_bar to high levels.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 11 Issue 05, May-2022

V. SENSE AMPLIFIER

The sense amplifier must detect the bit_line and bit_line bar to perform correct monitoring. It boosts the memory cell's read and writes speeds. It also has the responsibility of lowering the amount of electricity required for the operation. The fundamental function of the sense amplifier is to amplify the voltage difference produced on the bit_line and bit line_bar during read and write operation.

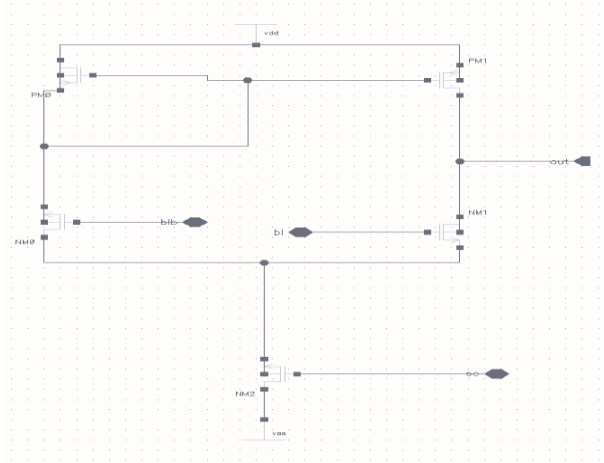

Fig 5. Schematic of the Sense amplifier

When SE equals To read "1," which consists of bit_line=1 and bit_linebar=0, go here. The transistors N_0 and N_2 are then turned on, while N_1 is turned off, leading to the activation of P_0 and P_1. As a result, VDD may be used to get high at the output logic. When bit_line=0 and bit_linebar=1 are used to read the logic "0," transistors N_1 and N_2 are turned on, whereas N_0 is turned off, resulting in the deactivation of P_0 and P_1. As a result, there is no route between VDD and the output, and logic "0" is displayed at the output. The waveform shows that when SE is strong for a certain period, whatever data is there in the bit _line is stored out.

VI. WRITE DRIVER CIRCUIT

The Write Driver is in charge of writing a certain value into the cell. The driver's role is to bring the bit_line and bit_line bar to the gnd so that the next job may begin. The role of Word enable is to grant or deny the Write Driver access to the bit lines.

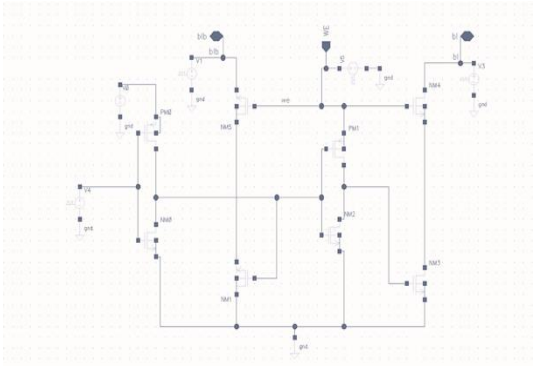

Fig 6. Schematic of driver circuit

The word enable(we), which is in the upper section of the circuit, is used to permit the driver. It consists of two NMOS transistors coupled fascinatingly one after the other. In the upper portion, there are also two inverters. First, two logics are assigned to the two positions of the most junction, namely 0 and 1. The bit_line closest to the 0 logic is discharged first, followed by its logic being inverted. The bit_line and bitline_ bar are released to the gnd in this manner. Its primary function is to create a low-impedance route to the gnd. As a result, the voltage differential between the bit line and gnd, as well as the bit line_bar and gnd, is zero.

VII. DECODER

Different varieties of Decoders are widely available, such as 2-to-4-line decoders and 3-to-8-line decoders, where 2, 3, and 4 are the number of inputs and 4, 8, and 16 are the number of outputs. It's just a circuit that translates binary data from n lines of input to up to 2n distinct outputs. The binary input conversion becomes easier as a result of this operation, and we require the required output from this type of output, which we may use for a variety of tasks such as data and memory cell word line selection.

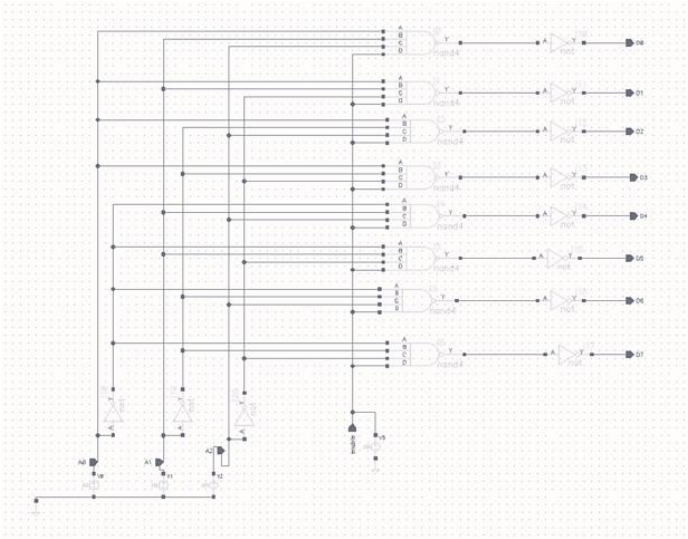

Fig 7. Schematic of decoder

8*8 ARRAY LOGIC

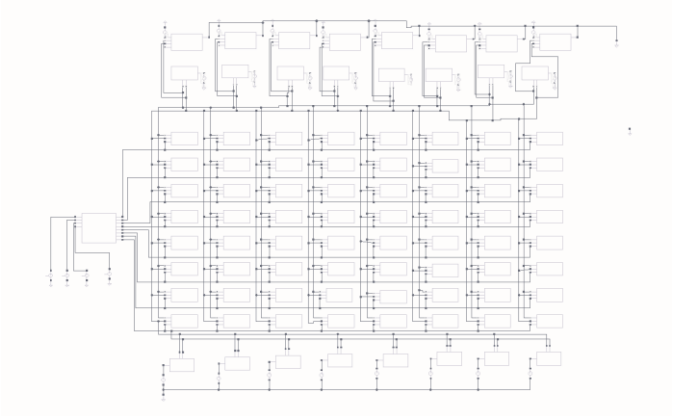

Fig 8. Schematic of 8x8 array

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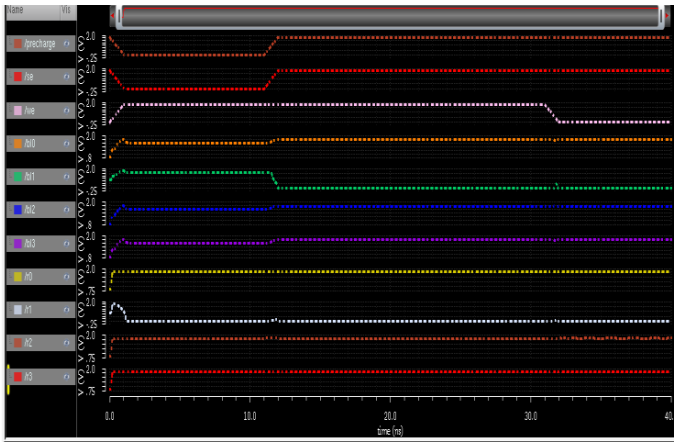

Fig 9. Transient Response for 64-bit SRAM Memory Array

Except for the voltage levels that are employed, the SRAM Array is designed utilizing FinFET 18nm technology. The basic 8X8 Memory Array is seen above, which can store 64 bits of data. Each column has eight pre-charge circuits, eight write drivers, and eight sensing amplifiers. From these 8 rows and columns, a 3:8 Row decoder is used to choose a specific row, and a 3:8 Column decoder is used to select a specific column.

Thus, at a moment just one cell is active where we may do read and write operations

VIII. SIMULATION RESULTS

The time delays and leakage powers of the new SRAM are compared to those of the current CMOS 45nm SRAM. In comparison to CMOS 45nm technology, Table 1 shows that power leakage for 8T SRAM in 18nm technology is significantly lower. When compared to 45nm technology, FinFET has the least leakage power and also has read and write latency. When compared to CMOS 45nm technology, FinFET-based SRAM offers superior values.

Table 2: Performance Comparison between CMOS 45nm SRAM cells and 8T SRAM Cell with FinFET18nm technology

Parameter	***CMOS 45 nm***	***FinFET 18nm (This work)***
Leakage Power	62 µW	2.062 µW
Read Delay	29.3ps	7.6 ps
Write Delay	714.21ps	69.13 ps

IX. CONCLUSION

After simulation and analysis, it was discovered that the suggested SRAM has much lower leakage power and delay durations than SRAMs built-in CMOS 45nm technology.

Individual circuits, such as the sense amplifier, pre-circuit, write driver circuit, and decoder, are constructed and tested using transient analysis, as previously stated.

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