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Design of A Three Phase Reduced Switch Multilevel Inverter Based on Different SPWM Techniques

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***Abstract*—In recent days variable voltage speed drives play an important role in many industries. Basically three phase multilevel inverters are used in various industrial applications and the scheme called Pulse Width Modulation scheme is the most commonly used scheme on the inverters to generate variable voltage & frequency. In this paper a three phase multilevel inverter with reduced number of switches has been designed using MATLAB/SIMULINK environment based on three different sinusoidal pulse width modulation techniques (PD, APOD & POD).**

Keywords—SPWM, Three Phase Multilevel Inverter, THD, MATLAB/SIMULINK, PDPWM, APODPWM, PODPWM.

I. INTRODUCTION

In SPWM scheme a reference signal waveform which is usually a pure sinusoidal waveform & a carrier signal waveform are compared and the intersections between two provides the 'ON' & 'OFF' instances of the switches used in the multilevel inverter. Multilevel inverters play a great role in improving the power quality of various industrial drives. By increasing level of the inverter overall THD can be reduced & consequently the power quality is improved.
In this paper a topology of a reduced switch multilevel inverter which reduces the overall cost of the inverter is explained using PDPWM, APODPWM & PODPWM methods and the variation of THD with the variation in Modulation Index (MI) & level of inverter is shown.

II. LITERATURE REVIEW

1. Biswamoy Pal, Reetam Mondal proposed a new multilevel inverter topology with reduced numbers of switches than that of a conventional multilevel inverter. This paper also described a method for generating PDPWM signal in order to generate sinusoidal output voltage with fewer harmonic. The variation in overall THD of inverter output voltage is also shown in this paper with the variation in levels of MLI at different carrier frequencies.

2. B. Pal, B. Dey, C. Debnath, S. Banerjee proposed a new multilevel inverter topology which described with reduced number of switches. Different Sinusoidal PWM schemes (PD, POD, APOD) has been employed to the reduced switch inverter and a comparative performance is analyzed of the inverter in terms of Total Harmonic Distortion. The reduced switch multilevel inverter has been designed and different SPWM schemes have been developed in MATLAB SIMULINK environment.

3. Biswamoy Pal, Aniruddha Mukherjee proposed a method in which comparative performance analysis of MOSFET based& IGBT based single phase inverter has been evaluated. The method compares overall THD of output voltage of these two proposed inverters. Here sinusoidal PWM scheme has been used which compares a sinusoidal reference voltage with a carrier based modulating signal to generate gating pulse for inverter circuit. Power quality of inverter output voltage has a great importance now a days which depends on overall THD. This method describes how THD of inverter output voltage can be controlled by varying frequency of carrier signal frequency.

4. T.Sengolrajan, B.Shanthi, S.P.Natarajan introduced a topology which investigates the performance analysis of various Multicarrier Pulse Width Modulation strategies with Sinusoidal reference for single phase seven level diode clamped Z-source inverter designed with two intermediate Z-source networks connected between the input source and inverter circuit. The diode clamped Z-source based MLI strategy enhances the fundamental output voltage and reduces the Total Harmonic Distortion (THD). Performance factors such as %THD, Vrms where measured and CF, DF of output voltage are calculated for different modulation indices 0.8-1. The results are compared. The simulation results indicate that the use of Z-Source in DCMLI boost 60% of the total output voltage. PODPWM strategy provides low THD and COPWM strategy is found to perform better since it provides relatively higher fundamental RMS output voltage.

III. PRINCIPLE OF PROPOSED REDUCED SWITCH THREE PHASE MULTILEVEL INVERTER

The topology of a three phase 15-level reduced switch inverter is shown in Fig. 1. The proposed structure contains four diagonal switches- S1, S2, S3 & S4. Switches S1&S2 function as opposite to the switches S3&S4. That means output voltage is positive if S1&S3 are ON and S4&S5 are OFF but the voltage is negative for the reverse case.

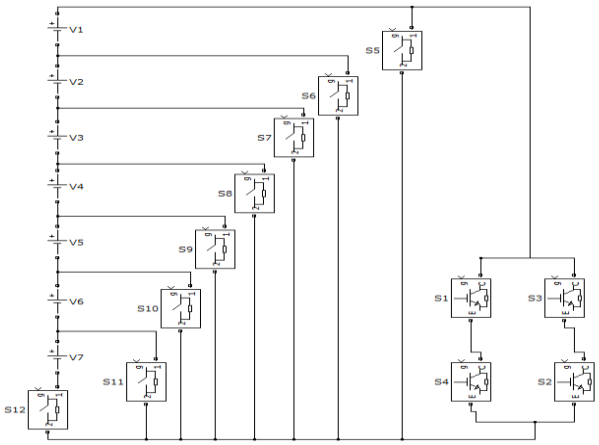

Fig.1. Topology of a 15-level inverter

The other switches are used to determine the level of the output voltage. If S5 in ON output voltage is 0, if S6 is on output voltage is $+V_{dc}$, if S7 is ON output voltage is $+2V_{dc}$ & so on.

A multilevel inverter structure of any level can be developed by using the following formulas:

Let the total number of switches required= N_{sw}

Number of levels= N_{level}

Number of voltage source required= S

Then,

$N_{sw}= (N_{level}+9)/2$ ..... (1)

& $N_{level}= 2S+1$ ..... (2)

From equation (1) & (2) the following equation can be derived,

$N_{sw}= S+5$ ..... (3)

The number of switches & the number of voltage source required for different levels of a multilevel inverter are shown in the following table:

Level (N_{level})	**NO. of Voltage Sources (S)**	**NO. of Switches (N_{sw})**
$N_{level}= 2S+1$	**$S= (N_{level}-1)/2$**	**$N_{sw}= S+5$ $= (N_{level}+9)/2$**
5	2	7
7	3	8
9	4	9
11	5	10
13	6	11
15	7	12

Table 1: Calculation of number of switches for the different levels of the inverter

IV. DIFFERENT SPWM TECHNIQUES FOR A MULTILEVEL INVERTER

There are three SPWM techniques for a multilevel inverter- a) Phase Disposition PWM (PDPWM), b) Phase Opposition Disposition PWM (PODPWM) & c) Alternate Phase Opposition Disposition PWM (APODPWM). The power quality of the inverter can be varied by varying the Modulation Index (MI) of the inverter. The MI of the multilevel inverter can be calculated as follows:

$$MI= A_r/(N_{level}-1)A_c$$

Where,

A_r= Amplitude of reference signal (sine wave)

$(N_{level}-1)$= Number of carrier signals used

A_c= Amplitude of carrier signal (triangular wave)

PDPWM technique:

In phase disposition scheme all the carriers are in phase & they occupy the adjoining bands. The following figure shows the strategy for a PDPWM signal generation in case of a five level inverter in which four carrier waveforms c_1, c_2, c_3 & c_4 are used which are in phase with each other.

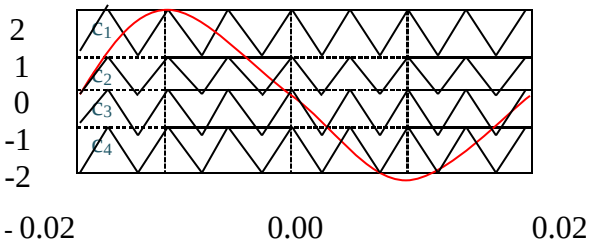

Fig.2. PDPWM Strategy

PODPWM technique:

In phase opposition disposition the carrier waveforms above the zero level are in phase with each other & the carrier waveforms below the zero level are also in phase with each other but they are shifted by 180 degree from the carrier waveforms which are above the zero level. The following figure shows the strategy for a PODPWM signal generation for a five level inverter in which c_1&c_2 are in phase with each other and c_3&c_4 are in phase with each other as well but they are shifted by 180 degree from c_1&c_2.

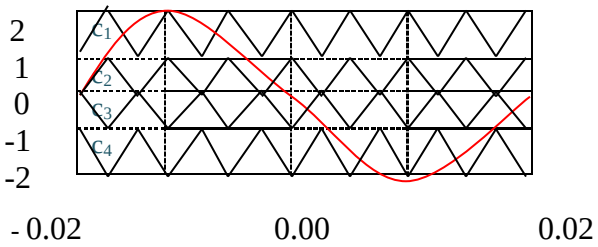

Fig.3. PODPWM Strategy

APODPWM technique:

In alternate phase opposition disposition all the carrier waveforms used are phase shifted with each other alternately by 180 degree. The following figure shows the strategy for a APODPWM signal generation for a five level inverter in

which c_1, c_2, c_3 & c_4 are alternately phase shifted from each other.

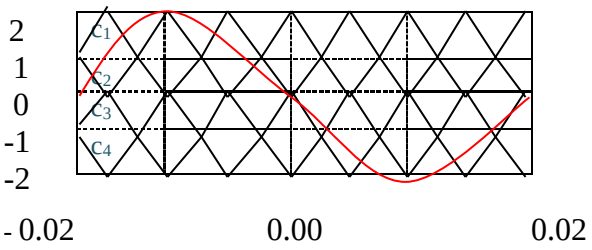

Fig.4. APODPWM Strategy

V. IMPLEMENTATION OF THREE PHASE REDUCED SWITCH MULTILEVEL INVERTER IN MATLAB/SIMULINK

Using PDPWM technique (for five level):

Step1:
In PDPWM scheme all the carrier waves are in same phase with each other. So for a five level inverter four carrier waves (two for positive half cycle, two for negative half cycle) are compared with three sine waves (for a three phase multilevel inverter). Another carrier wave resides on the zero level.

Step2:
Then some logical operations (AND, OR, NOR, NOT) are performed on the compared signal outputs to enable the signals triggering the switches of the inverter.

Step3:
Then the resulting outputs trigger the switches and consequently pulses are generated.

Step4:
Variation of THD according to the change in modulation index is shown.

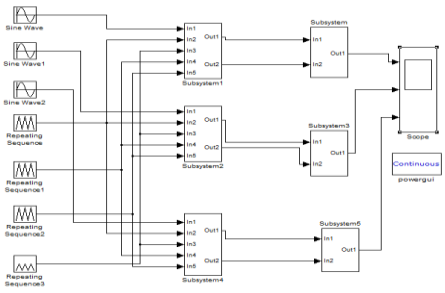

Fig.5. SIMULINK model of three phase five level inverter using PDPWM technique

Using APODPWM technique (for five level):

Step1:
In APODPWM technique alternate carrier waves are out of phase with each other. So, four carrier waves (two for positive half cycle, two for negative half cycle) which are alternatively out of phase with each other are compared with three sine waves (for a three phase multilevel inverter). Another carrier wave resides on zero level.

Step2, step3 & step4 are similar to the PDPWM technique.

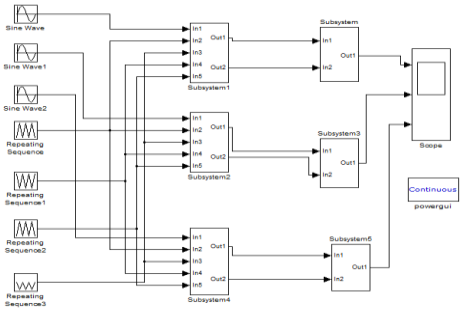

Fig.6. SIMULINK model of three phase seven level inverter using APODPWM technique

Using PODPWM technique (for five level):

Step1:
In PODPWM method the carrier waveforms above the zero reference value are in phase. The carrier waveforms below zero are also in phase but are 180 degrees phase shifted from those above zero. Therefore, four carrier waves (two for positive half cycle, two for negative half cycle) among which two are in same phase above zero level and other two reside below the zero level with the opposite phase are compared with three sine waves (for a three phase multilevel inverter). Another carrier wave resides on the zero level.

Step3, step4 & step5 are similar to the other two schemes.

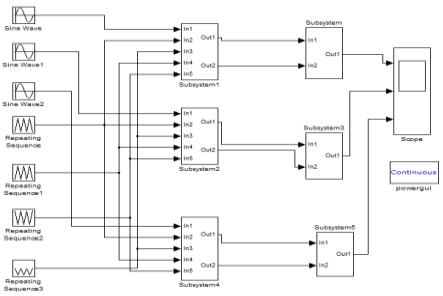

Fig.7. SIMULINK model of three phase five level inverter using PODPWM technique

The implementation of seven, eleven, thirteen & fifteen level inverters are similar to the five level inverter except the number of carrier waves increase with the increase in level i.e.; 6 carriers for 7 level, 8 carriers for 9 level, 10 carriers for 11 level, 12 carriers for 13 level & 14 carriers for 15 level are required. In each of the seven, eleven, thirteen & fifteen level one carrier resides on the zero level.

VI. RESULTS

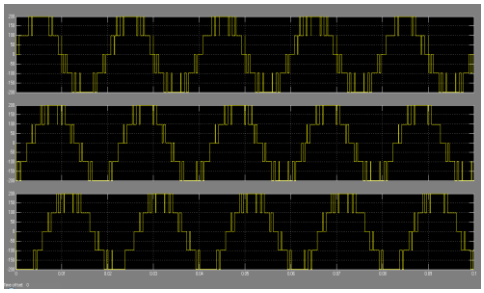

Fig.8. Inverter output for five level using PDPWM Technique

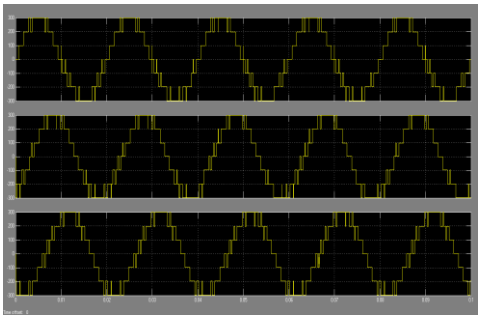

Fig.9. Inverter output for seven level using PDPWM Technique

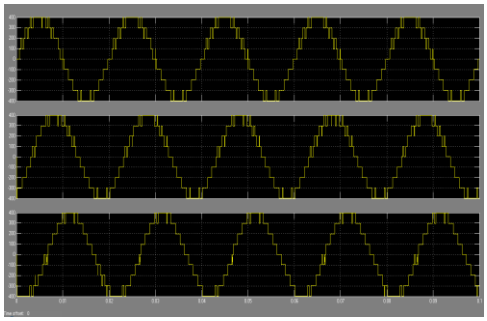

Fig.10. Inverter output for nine level using PDPWM Technique

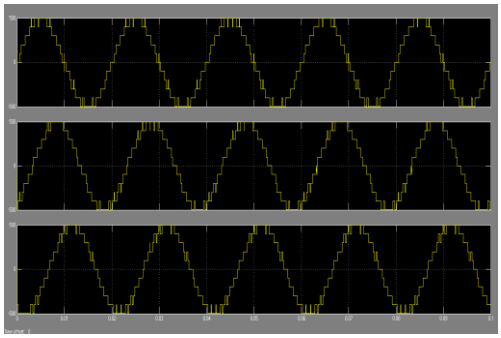

Fig.11. Inverter output for eleven level using PDPWM Technique

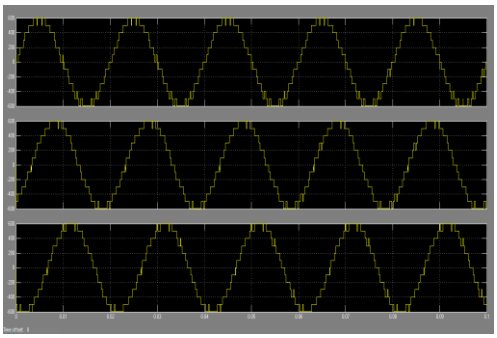

Fig.12. Inverter output for thirteen level using PDPWM Technique

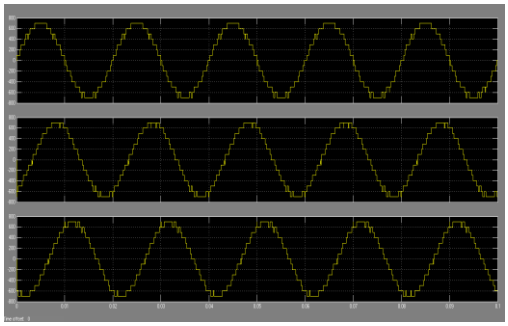

Fig.13.Inverter output for fifteen level using PDPWM Technique

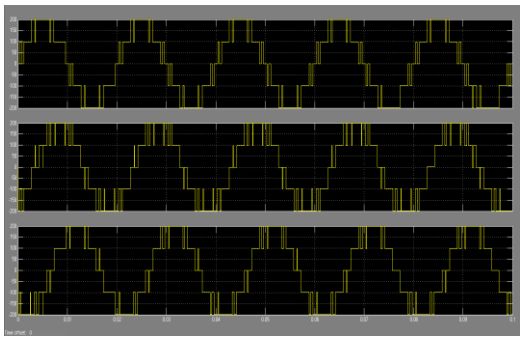

Fig.14.Inverter output for five level using APODPWM Technique

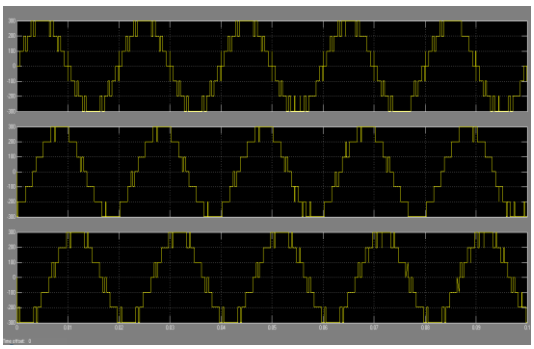

Fig.15.Inverter output for seven level using APODPWM Technique

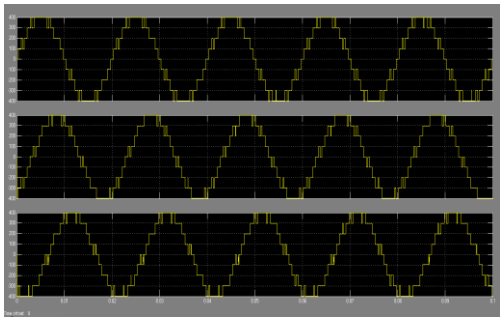

Fig.16.Inverter output for nine level using APODPWM Technique

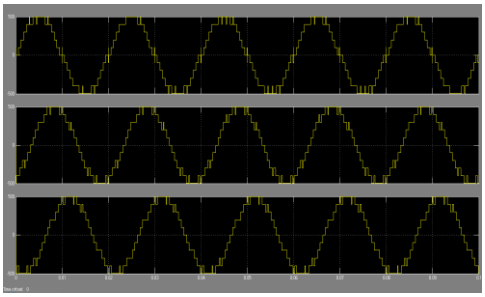

Fig.17.Inverter output for eleven level using APODPWM Technique

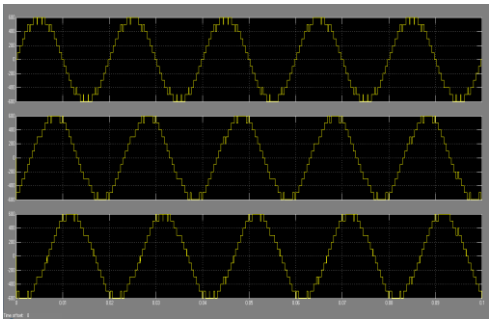

Fig.18.Inverter output for thirteen level using APODPWM Technique

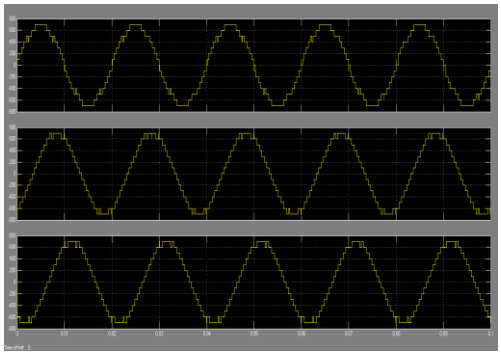

Fig.19.Inverter output for fifteen level using APODPWM Technique

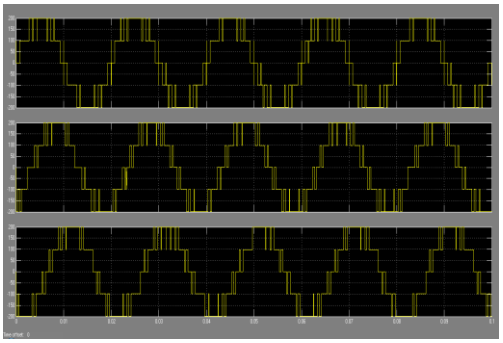

Fig.20.Inverter output for five level using PODPWM Technique

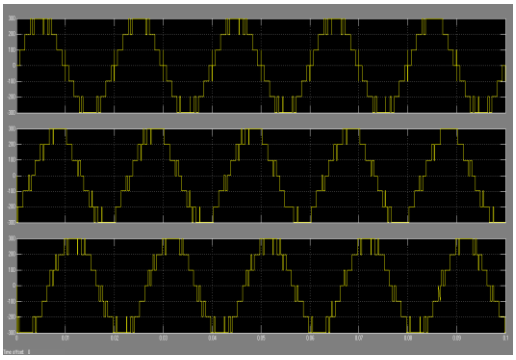

Fig.21.Inverter output for seven level using PODPWM Technique

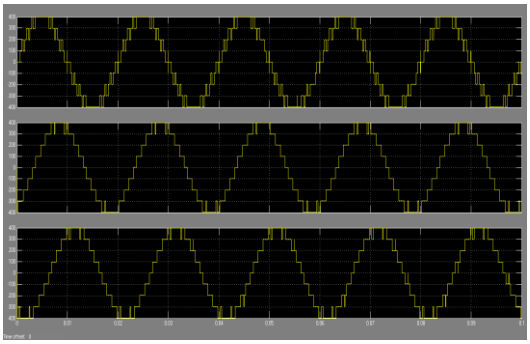

Fig.22.Inverter output for nine level using PODPWM Technique

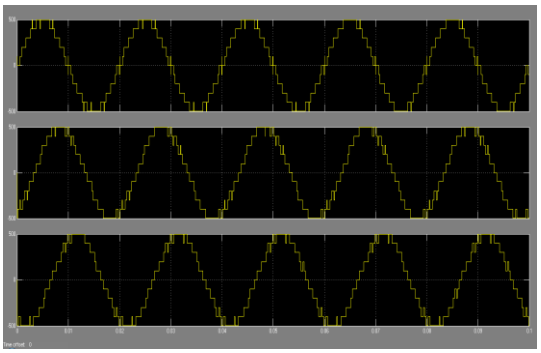

Fig.23.Inverter output for eleven level using PODPWM Technique

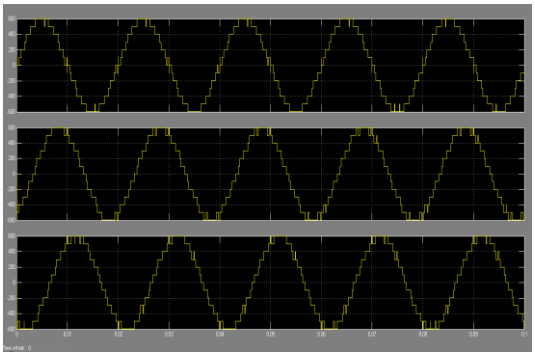

Fig.24.Inverter output for thirteen level using PODPWM Technique

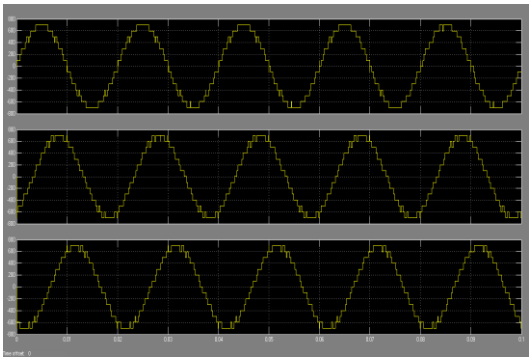

Fig.25.Inverter output for fifteen level using PODPWM Technique

THD Analysis:

The following table shows variation of three phase inverter performance in terms of THD of output voltage for different levels at different modulation index using different level shifted PWM techniques.

Level of MLI	Modulation Index	% THD of inverter output voltage		
		PDPWM	APODPWM	PODPWM
5 Level	1	24.22	24.71	23.36
	0.8	38.38	38.57	37.94
	0.5	48.62	45.97	44.46
7 Level	1	17.01	18.06	15.64
	0.8	23.44	20.82	21.77
	0.5	39.51	35.39	40.45
9 Level	1	13.75	13.08	15.94
	0.8	15.14	14.51	14.36
	0.5	23.98	24.25	23.19
11 Level	1	10.31	9.99	10.20
	0.8	13.64	12.73	15.91
	0.5	23.58	21.69	22.33
13 Level	1	9.55	8.74	8.70
	0.8	12.57	12.79	11.17
	0.5	17.16	15.45	15.78
15 Level	1	7.94	8.79	7.60
	0.8	10.19	10.31	10.76
	0.5	15.69	15.53	16.04

Table 2: Variation in %THD for different levels

Performance Analysis:

Variation in % THD of output voltage for different levels of MLI with Modulation Index = 1 for PDPWM is shown below,

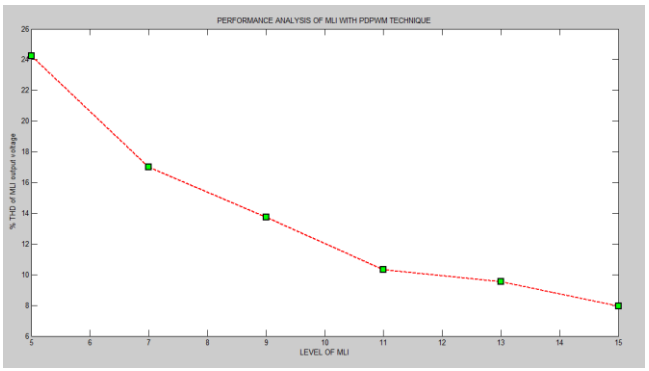

Fig 26: Performance analysis of MLI with PDPWM technique

Variation in % THD of output voltage for different levels of MLI with Modulation Index = 1 for APODPWM is shown below,

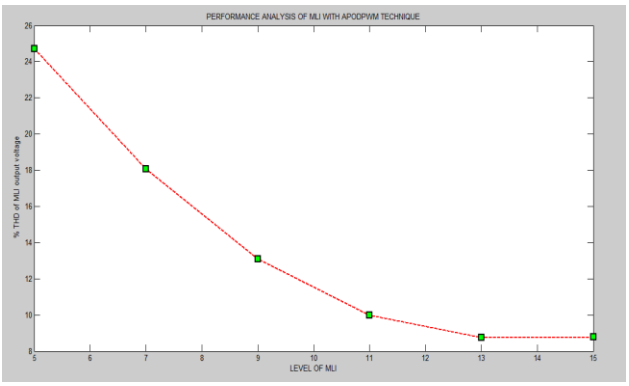

Fig 27: Performance analysis of MLI with APODPWM technique

Variation in % THD of output voltage for different levels of MLI with Modulation Index = 1 for PODPWM is shown below,

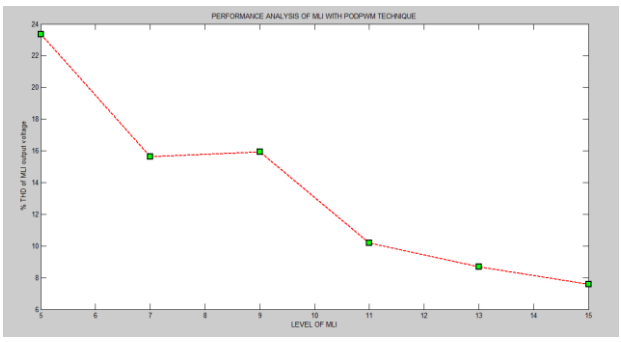

Fig 28: Performance analysis of MLI with PODPWM technique

VII. CONCLUSION

In this paper the concept of three phase multilevel inverter with reduced number of switches using different SPWM techniques has been explained in MATLAB/SIMULINK environment. It has been shown in this paper that overall THD is reduced with the increase in level of inverter & consequently the inverter performance is also increased.

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