Design of a High Speed LVDS Bus Interface Using FPGA

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Abstract

Electronics circuits and systems have increased in complexity in recent years so we have to develop more sophisticated and low cost automatic test equipment. In automated testing system, there are several types of interface systems that can be used to connect to testing instruments. In order to attain high-speed transmission of binary data a low voltage differential signalling method is used to send and receive data between the communication card and pin electronics in an ATE. *Data rates of more than 455 Gbits/s in-chips can be achieved using LVDS interface technique. As Integrated Circuit's communication speeds has increased differential signalling is used to handle high speed. Design of high speed LVDS (Low Voltage Differential Signalling) bus interface controller using FPGA is presented. Source-synchronous clocking is used to achieve this high speed data transfer. The de- formatted packet data is transmitted through FIFO to 16B/20B encoder where it is encoded and transmitted serially using a serializer. The receiver module receives the data serially by the deserializer and then decodes to verify the transmitted data. The SerDes architecture is considered.*

1. Introduction

In electronic engineering, test and measurement is a key area, where test technology is been used throughout the life of electronic products which includes from its initial development, through verification of the product and manufacture, to maintenance and repair during its service life. According to which there are various test techniques, test equipment and test technology. Automated Test Equipment (ATE) is computer-controlled equipment that tests electronic devices for functionality and performance. In semi-conductor industries ATE is mainly for testing of semiconductor devices and systems which form simple components like resistors, capacitors and inductors to integrated circuits (ICs), Printed Circuit Boards (PCBs) and also complex, assembled electronic systems. ATE systems are designed to reduce the amount of test time needed to verify whether a particular device works inorder to quickly find its faults before it is used in a final quality. To reduce manufacturing costs and improve yield, semiconductor devices should be tested after being fabricated to prevent even a small number of defective devices. In addition to the semiconductor industry, ATE is also used in the automotive, medical equipment, airplane, and other manufacturing industries. The first ATE systems were introduced in 1960's replacing the numerous separate instruments, manually wired connections and paper test procedure. Thus these systems, automated the test procedures by using computers and digital test resources that can be programmed and switched to a device under test (DUT), which enables the test results to be captured automatically.

ATE usually includes a personal computer, communication card and pin electronics card. The device under test is connected to the pin electronics and the tester data is applied to the device under test to study the functionality and performance of the device. The response from device is analyzed and the result is collected by computer. In brief testing typically consists of applying set of test stimuli to inputs of circuit under test, and analyzing the output responses. A simpler test system for the complete functional testing of VLSI devices with large pin count can be developed. The architecture of main test system which is to develop a scalable low cost test system for high pin count VLSI devices has the following parts. The main parts are: - PC controller mainly controls the whole testing which is used to input the data vectors in the required format to the controller and also take the resultant vectors from the controller. It compares the values obtained from the Device Under Test with a set of expected values already present. Then it gives the functional PASS or FAIL for the test which was conducted. Then it decodes the data vectors and selects the module and writes to that module. At the end of test it sends back the captured data from the module to the PC. Pin Electronics drives the desired waveform at the pins at the desired times at the proper voltage level and also capture the response from the IC pin. The design includes formatting of the tester data received from PC and sending it to Pin Electronics using LVDS. The data packet to be sent should include header and data. The header includes many control fields. The interface between communication card and PE is done using Low Voltage Differential Signaling interface to attain high speed

data transfer. LVDS is chosen to drive these high speed transmission lines due to its speed, low power consumption, noise control and cost advantageous for data communications. LVDS is currently one of the best point to point interfaces suitable for gigabit per second data rates. Encoding scheme is also applied on the data for security and reliability

2. Design of Bus Interface Controller

In automated testing, there are several types of interface systems that can be used to connect computers to testing instruments. Here, design of a high speed LVDS data bus interface controller for data communication between communication card and pin electronics card in test system is been developed. A LVDS source synchronous Serialization and Deserialization data transmission is proposed. The goal is to transmit de-formatted tester data stored in FIFO from the Communication Card using a Low Voltage Differential Signalling (LVDS) interface to a Pin Electronics circuit. Source-synchronous clocking is used to achieve high speed data transfer. The design of bus interface architecture includes the following blocks as shown in Figure 1:-

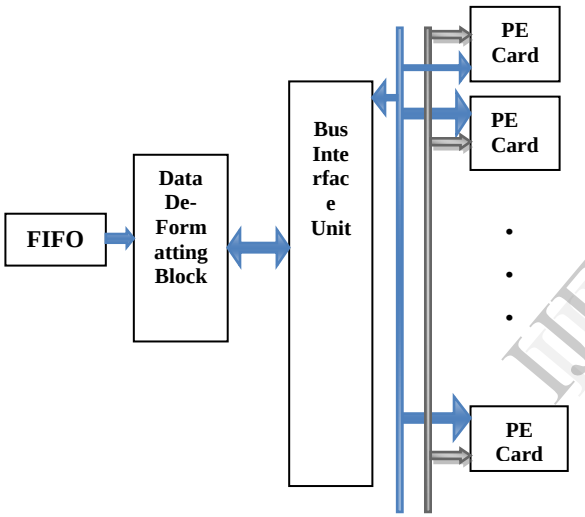

Figure1. Block diagram of architecture

FIFO is a memory queue with control logic that manages the read and writes operations and also generates status flags such as empty and full for interfacing with the user logic. A synchronous FIFO is designed for the bus controller. A synchronous FIFO refers to a FIFO design where data values are written sequentially into a memory array using a clock signal, and the data values are sequentially read out from the memory array using the same clock signal. The designed FIFO has a depth of 20 and width of 16. The packet format received from fifo has a header and data part. The format of header block is shown in the Figure 2. In data de-formatting block the first value from FIFO is read and then it is checked whether the value equals the constant sync value for synchronization, such that a sync_detect signal indicates that it is synchronized and it determines the start of a packet. Therefore, only if the sync_detect signal is high we read the next values from FIFO block and then the next value read decodes or selects the PE card number and thus enables us to identify out of 9 to which PE card the data send will be received. The other blocks are described below.

Sync Sequence
PE card number
Type of data (timing/waveform/vector/channel)
Sub-packet number for vector data
No. of bytes in data block

Figure2. Format of header block

3. Bus Interface Unit

Bus Interface Unit has a transmitter section which includes an encoder, a serializer and OBUFDS. The tester data fields of 16 bits each are encoded and transmitted serially over LVDS to the PE Card. The encoding scheme chosen for my work is 16B/20B encoding and OSERDES is the serializer.

3.1. LVDS transmitter unit

The transmitter module takes 16 bit data on the parallel side encodes it and performs serialization for each LVDS channel and the given to OBUFDS to obtain the differential signals. The deformatted data from FIFO is encoded using 16B/20B block encoding scheme where the 16 bit input is encoded to 20-bit value and the 20 bit parallel data is converted to serial form using a serializer.16B/20B protocol is used to encode a 16 bit word to 20 bit codes that will result in a dc balance serial stream. The serialization is done by OSERDES block.

A 16B/20B transmission scheme incorporates the ides of the 8B/10B transmission code by combining two 8b/10b modules. The input data is provided to both the 8B/10B encoder. In 8B/10B encoding the 8 bit input is divided into two blocks of MSB 3 bit and LSB 5 bit which is converted to 4 bit and 6 bit respectively. The extra bits that are added for encoding depends on the disparity of each blocks of input data disparity of a binary digit is the difference between the number of 1's and number of 0's. The detailed steps in code construction are described in [4].The encoded 20 bit data is given to the serializer block. The OSERDES consists of parallel in serial out block. A single OSERDES primitive can only perform a 6:1 serialization, but it is possible to concatenate two OSERDES blocks in a master/slave model to serialize up to 8 bits. There are shiftin and shiftout ports available for the concatenation. The 20 bit encoded value is stuffed with zero to get a 24 bit value and the serializer takes parallel data, converts it into a serial stream, where we get the 24 bit serial value in 8 divide by clock which is given to Differential Signaling Output Buffer (OBUFDS) for transmission. OBUFDS is a single output buffer that supports low-voltage, differential signaling. Its output is represented as

two distinct ports, where one output is the opposite phases of the same logical signal

4. Pin Electronics

Pin electronics deliver signals, power, or precise voltages and currents, and can measure the pin's response, drive data, and electrical characteristics. Its function is to drive the desired waveform at the pins at the desired times at the proper voltage level like TTL, CMOS, ECL etc The PE should capture the response from the IC pins at the proper time and store it for further analysis.

4.1. LVDS receiver unit

The receiver in PE card receives the differential signal which is given to Differential Signaling Input Buffer (IBUFDS), which generates the serial data and then performs deserialization and decoding. ISERDES is used for deserialization in the thesis. After deserialization we get 24 bit data where the last 4 bits are zeros. The zero bits are removed and then the 20 bit is decoded to get the 16 bit data that is transmitted. The receiver block includes IBUFDS, ISERDES and decoder. The differential signals are given to IBUFDS, an input buffer that supports low-voltage, differential signaling. In IBUFDS design, its input is represented as two distinct ports and serial output is obtained. The deserializer is done using ISERDES block. The Input Serial-to-Parallel Logic Resources (ISERDES) in Virtex-5 FPGAs is a dedicated serial-to-parallel converter with specific clocking and logic features designed to facilitate the implementation of high-speed source synchronous applications. The ISERDES avoids the additional timing complexities encountered when designing deserializer in the FPGA fabric. A single ISERDES component can only deserialize 6 bits. Therefore two ISERDES components are used to deserialize up to 8bits in SDR mode. Decoding is the reverse process of encoding, it restores 20-bit code groups from the input 16-bit code group according to the original code table. A 10B/8B decoder block is used for each upper and lower byte of incoming data. Decoding of data can be done by the examination of just 6 and 5 bits. The required bit translation for decoding can be extracted from table provided in [5].

5. Results and Discussions

The transmitter and receiver sections along with the components specified in the design are coded in VHDL and synthesisedusing Xilinx ISE 13.2 for Virtex5 FPGA board.

Figure 3. FIFO and data de-formatting block

Each 16 bit data is read from FIFO and send the data to encoder. When first value is read it is compared with the sync sequence. Sync sequence. selected is:-1010101010101011.If the sync sequence is identified the next value is read which selects (out of 9) to which pin electronics card the data has to be send. The other fields are encoded and transmitted through differential signals. The read and write cycles of FIFO are shown in Figure 3.

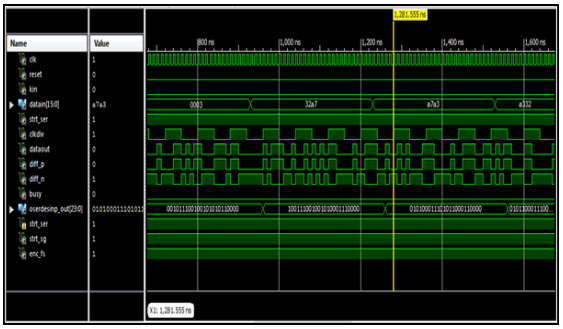

Figure 4. Simulated waveform of transmitter

The data from data de-formatting block is given to encoder where the 16 bit input is encoded to 20 bit value which increases the redundancy and also security. When the reset pin is low the input given at input pin is encoded and then after 3 clock cycles the encoded value is obtained at output pin. This encoded value is given to the serializer, OSERDES. Four 0's are concatenated to the encoded bits to get 24 bit value. OSERDES has clkin and clkdiv pins where clkin is the input clock and clkdiv is divide Then after a delay of 6 clock cycles the parallel data is converted to serial data and obtained. In transmitter all the above blocks along with OBUFDS are interfaced to get the transmitted signal which has to be sent to receiver of pin electronics card.

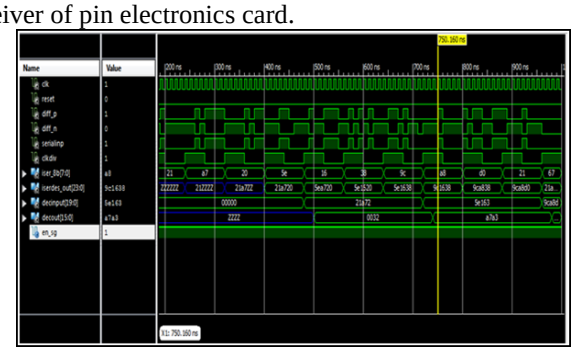

Figure 5. Simulated waveform of receiver

The differential signals are received and converted to serial signal using IBUFDS. The serial data is given as input to ISERDES. This serial data is converted to parallel output after a delay of 2 clkdiv cycles. The last four 0's are removed and given to the decoder. The decoder decodes the 20 bit data to receive the 16 bit data. On integrating the IBUFDS, ISERDES and

decoder blocks we get the tester data that is sent.

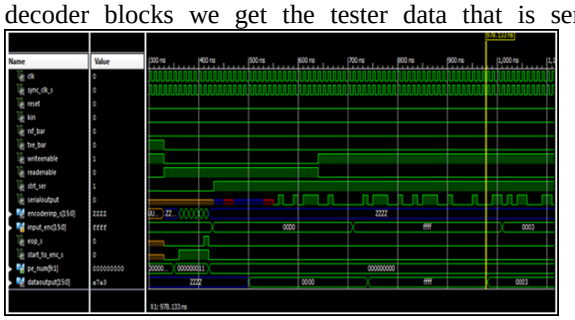

Figure 6. Simulated waveform of top module

The top module integrates both the transmitter and receiver blocks so that the received signal can be verified with the transmitted signal such that both signals are equal. Thus, the transmitted and received values are verified equal.

6. Conclusions

The system is designed for high-speed data transmission, with low cost and power. A high speed LVDS data bus interface controller applicable in an ATE system for data transmission and reception is been coded in VHDL and has been synthesised for the Virtex5 FPGA board using XILINX ISE13.2. LVDS technology solutions eliminate the trade-offs in speed, power, noise, and cost for high-performance data transmission applications. LVDS not only achieves great benefits in existing applications, but opens the door to many new ones. The testing of LVDS systems involves understanding of the requirements and standards, selecting of measurement devices, compensating for the impact of measurement devices, minimizing external influences, and planning to deal with systems that fail the requirements.LVDS applications will be able to quickly adapt and scale with the new innovations in technology, such as improved processes and lower supply voltages. This quick adaptation will surely help the longevity of the LVDS solution in the foreseeable future.

7. References

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