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Design of a 2.4 GHz Common Source LNA with Inductive Degeneration for RF-IC

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***Abstract*— This paper illustrates a 2.4 GHz low noise amplifier (LNA) designed for use in RF receiver system for radio frequency integrated circuit (RFIC). The design has been made in 90 nm technology using CMOS. The proposed LNA design uses common source configuration with inductive degeneration technique. This technique provide high linearity The simulation result shows that total power consumed is 15.6mW only at low supply voltage of 1.5 V. This amplifier provides a forward gain of with a low noise figure of 0.58dB. The input return loss (S11) is -9.6dB and output return loss (S22) is -2.2dBrespectively. This amplifier provides a forward gain of 11dB at 2.4 GHz.**

Keywords*— Low noise amplifier(LNA), Noise Figure (NF), Gain, RF

I. INTRODUCTION

Wireless sensor network is emerging as a popular recent trend in new markets. Radio frequency (RF) is an electromagnetic wave frequency whose range is around 3KHz to 300GHz. As shown in block diagram of RF receiver system signal coming from antenna is RF signal. RF receiver is used in two way devices such as radios and mobile phones etc. Wireless local area network (WLAN) at 2.4 GHz is emerging very rapidly. CMOS is having advantage of ease of integration. It can be scaled to any technology and hence due to higher level of integration, it reduces cost of wireless communication systems[2]. RF receiver is battery powered [1]. Power consumption can be reduced by adequate receiver sensitivity. This can be done using low noise amplifier (LNA). LNA is a first building block of wireless network. It affects the performa-nce of receiver of RF receiver system. It consumes less chip area because it uses MOS devices which is active component when implemented on chip uses less area as compared to lumped components (R,L,C). It also consumes less power, less noise, high linearity and adequate gain [2]. The basic block diagram of RF-receiver is shown in fig (1). The overall performance of the RF receiver system depends on the LNA gain and noise figure(NF). The LNA design faces several challenge Such as such as sufficient gain to suppress noise, low power, high linearity low noise figure and impedance matching because every communication systems implementation with with the standard, which includes low power and low data rate. So, the design of LNA is aimed at lower power consumption We try to make LNA such that it provide a minimum noise figure while providing sufficient linearity with gain and a stable 50Ω resistance for the impedance matching. Impedance matching play significant role and it is critical when a preselect filter such a BPF precedes the LNA in RF receiver system.

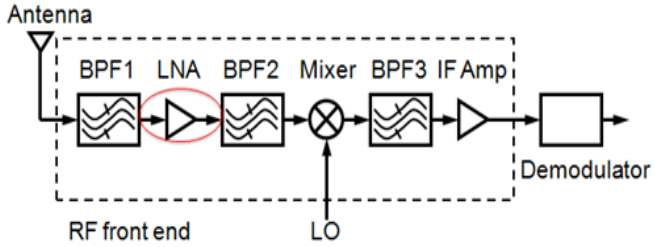

Fig (1). Block diagram of RF receiver system

This paper includes the design and implementation of Low Noise Amplifier in 90nm technology. This paper is organized in following manner; Section II gives proposed LNA design. Section III gives simulation result and section IV is the conclusion of our paper.

II. LNA CIRCUIT DESIGN

A. Topologies Used In Lna Design

LNA circuit should be simplified as much as possible because if it is complicated then parasitic effects are introduced. So different topologies are introduced for single ended narrow band low power, low voltage design, low noise figure such as common source with resistor, common gate, common source with shunt series feedback, cascode inductive degeneration source and inductive degeneration common source respectively and these types of topologies are shown in Fig (2). But in proposed design of LNA we have used common source with inductive degeneration type of topology is shown in Fig (3).

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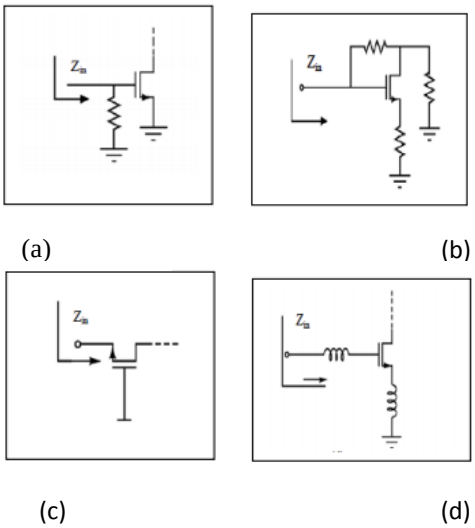

Fig.2. LNA Architectures (a) Resistance Match (b) Feedback Structure (c) Common Gate Structure (d) Inductive Degeneration

This LNA design approach uses common source with inductive degeneration type of topology to provide high linearity [5]. This LNA operates at 1.5 V of power supply. The matching provided at input and output port is 50Ω. Matching network consist C1 and C2 and small inductor. Thumb rule says that if I_{bias}= 1mA than the value of g_m will be 10 to 20 times the value of I_{bias}. For this circuit value of I_{bias} is 10mA, if this device works in weak inversion region than to maintain linearity it is quite difficult so the device should operate in saturation region. According to the rule if the device is operated at certain current of any value than you should maintain the overdrive voltage V_{dsat} at 200mV. It means the device is working in strong inversion, if V_{dsat} goes below than g_m goes high for same I_{bias}. The relation between V_{dsat} and $\frac{W}{L}$ is given by formula which is define below. The total capacitance offered by gate and drain terminal is given as:

$$I_d = \mu_n C_{ox} \frac{W}{2L} (V_{gs} - V_t)^2 \quad (1)$$

$$V_{dsat}^2 = \frac{2I}{k_n'(\frac{W}{L})} \quad (2)$$

$$C_{gs} = C_{ox} \times w \times l \quad (3)$$

$$C_{ex} = C_{gs} + 2C_{ds} \quad (4)$$

$$Z = g_m \times \frac{L_s}{C} \quad (5)$$

$$F_0 = \frac{1}{2\pi(L_g + L_s)C_{ex}} \quad (6)$$

Value of C_{gs}, C_{ex}, Ls, F_0 is calculated by given equations,and gain(A_v) is calculated by the formula given below:

$$A_v = \frac{\sqrt{L/C}}{R} \quad (7)$$

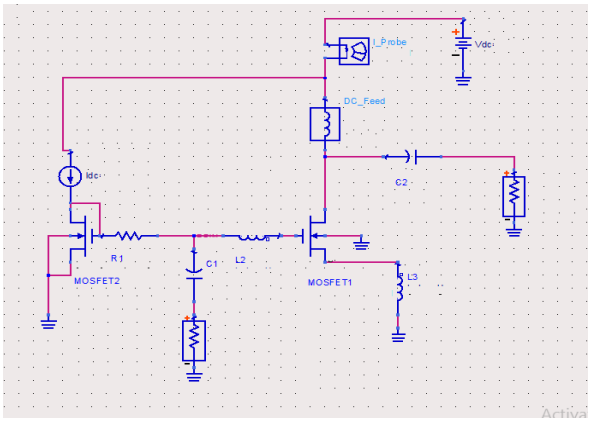

Fig 3 Circuit layout of proposed design

III. DESIGN SPECIFICATION

The sensitivity of communications system is limited by noise. The noise factor (F) of a system is defined as:

$$F = \frac{(SNR)i}{(SNR)o} = 1 + \frac{Na}{Ni} \quad (8)$$

Where: $(SNR)_I$ and $(SNR)_o$ are the signal to noise ratios in the input and output ports respectively. The N_i is the noise present at input source and the N_a is the overall noise due to circuit. The Noise Factor of a series system is given as:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots\ldots\ldots\ldots \quad (9)$$

where F_1, F_2, F_3, G_1, G_2, G_3 are the noise factors and power gains at each stage of the design.

Eqn.(9) Shows that if the power gain of the first stage is large then the total noise factor will be dominated by the first stage of the design. Since LNA is the first basic block in the receiver path, so LNA should provide enough gain and generate noise as less as possible.

IV. SIMULATION RESULTS

This section describes simulated results of common source with inductive degeneration technique operated at 2.4 GHz. The design was simulated using 90nm technology. These are the figures (4-7) represents the S-parameter curves, from the simulation results it is shown that input signal frequency varying from 1GHz. This shows that S11 (input reflection coefficient), S12 (reverse gain coefficient), S21 (forward gain coefficient), S22 (output reflection coefficient) respectively.

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With the help of S-parameter we can calculate the insertion and return losses. The input return loss (S11) is -9.6dB and the output return loss (S22) is -2.2dB. The maximum power gain (S21) is 11dB at 2.4GHz. The S12 is -16dB. The circuit is designed to achieve the target 2.4 GHz.

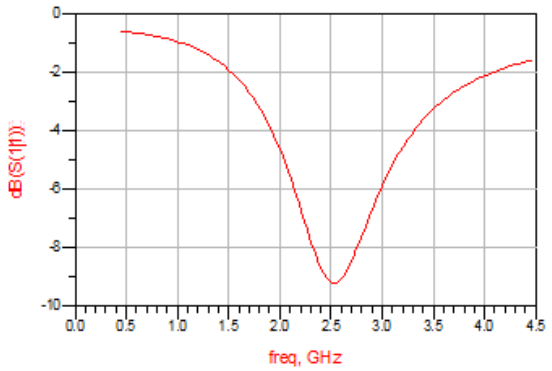


Fig 4 Simulation result of Input reflection coefficient S11

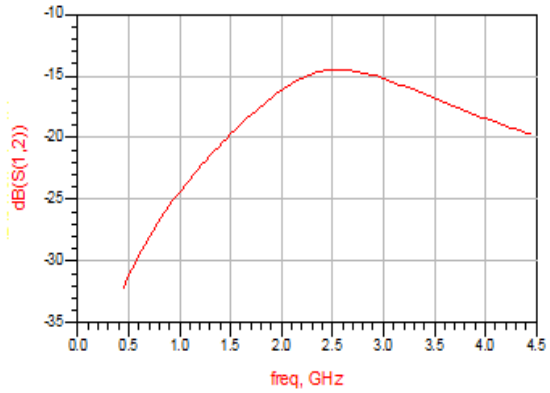


Fig 5 Simulation result of reverse gain coefficient S12

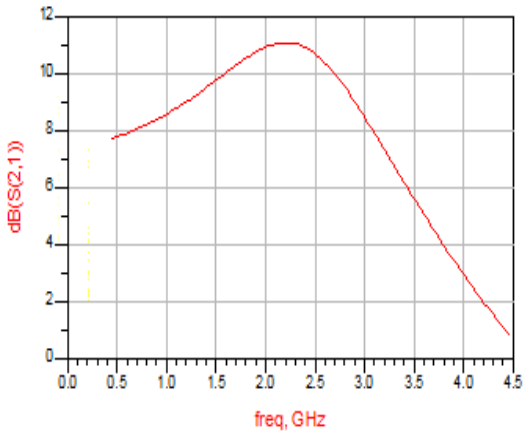


Fig 6 Simulation result of forward error coefficient S21

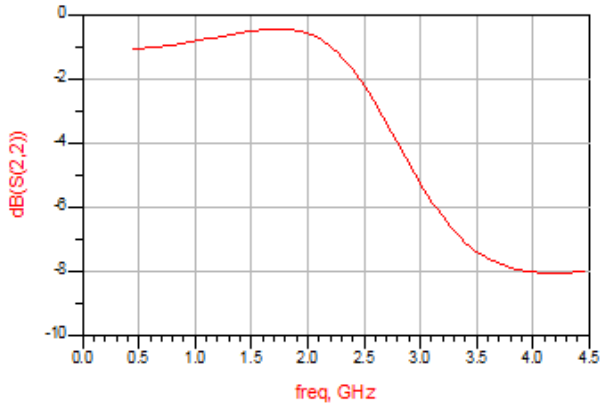
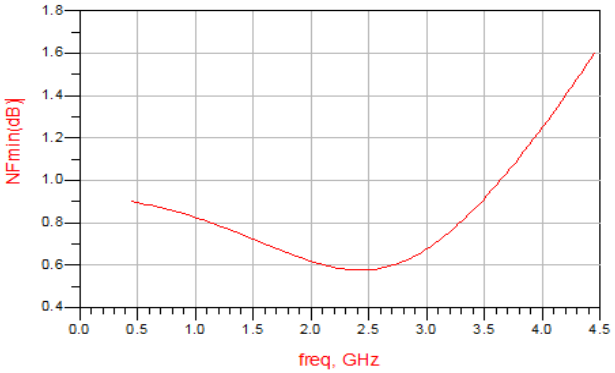


Fig 7 Simulation result of output refection coefficient S22

All the on chip inductors used here are spiral in nature. All the on chip capacitors here are MIM (Metal-Insulator-Metal) capacitors. The parasitic effects of MOSFET have also been considered. When the transistors have been seized it provides good noise characteristics, while allowing a good input impedance matching over the targeted frequency. The measured noise figure is shown in fig(8).



Fig(8) Simulation result of Noise Figure

TABLE: (1) COMPARISON BETWEEN 2.4GHz CMOS LNAs

References	[1]	[4]	[6]	[7]	[10]	This Work
Technology(um)	0.13um	0.13um	0.18um	0.13um	0.18um	0.09 um
Supply Voltage(V)	1.2	0.8	1.8	0.6	1.0	1.5
Frequency(GHz)	2.4	2.4	2.4	2.4	2.4	2.4
Gain(dB)	20.0	22.0	13.7	14	12.92	11.0
S11,S22(dB)	NA	NA	NA	NA	NA	-9.6, -2.2
NF(dB)	4.0	3.6	2.77	3.8	3.8	0.58
Power(mW)	1.32	0.8	18	0.12	13	15.6

Table:1 describes the performance of this proposed LNA and compare it with other published circuit performance. Our proposed LNA achieves low power consumption and noise figure at 90nm technology.

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V. CONCLUSION

The proposed design of LNA in this paper is implemented in 90nm technology. This paper describes a new topology of LNA , we have chosen the inductive degeneration topology in this LNA design which offers a low noise figure 0.58dB and high linearity under 1.5V power supply voltage. The simulation results have shown that the proposed LNA consumes only 15.6mW power while achieving a power gain of 11dB. This proposed design of LNA has relatively small noise figure and power consumption at 90nm technology. This LNA also works in the ISM band application. The simulation results validate peak performance at 2.4GHz that suitable for wireless sensor network.

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