Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 8 Issue 06, June-2019

Design of 876 MSPS, 2.5v, 250nm, 4-Bit Flash ADC using Quantum Voltage Comparator and Pseudo Logic Encoder

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Abstract: **- Nowadays, there is the highest use of converters in the industries. The degradation of power consumption by these converters has great importance. This paper represents a new method to decrease the power consumption of the flash type analog to digital converter with 250 nm CMOS technology by using frequency which is of 1MHz. Flash type ADC requires 2^n-1 Comparator and its power supply voltage 2.5V. The proposed design of ADC using the Quantum Voltage Comparator eliminates the resistor ladder circuit and improves linearity of ADC. For the encoding process, the Pseudo-logic encoder has been used and it provides higher data conversion rate and maintain low power consumption. The proposed 4-bit flash ADC paper having 876 MSPS speed and optimized power consumption by using the pseudo-logic encoder and Quantum Voltage Comparator.**

Keywords: - 4-Bit, Flash type ADC, Quantum Voltage Comparator, CMOS, Pseudo logic Encoder, TANNER EDA.

I. INTRODUCTION

An ADC is a very important feature that converts an analog signal to a digital signal. It provides the bridge between the analog and digital world. There are different types of ADCs pipelined ADC, Sigma-delta ADC, counter type ADC, etc which are affected by noise and power consumption. With the implementation of various technologies in the analog to digital circuits, the noise and power consumption can vary simultaneously [7]. There are three types of technologies used in data converters which are CMOS technology, bipolar technology, and gallium arsenide technology (GaAs) [4]. Among this CMOS technology having a high noise immunity and low static power consumption.

One problem with TIQ is that is noise susceptibility [5]. TIQ has a single-ended input, the comparator is very sensitive to power supply noise and power supply voltage. To overcome this problem, we use a new comparator called Quantum Voltage (QV). It does not use the resistor ladder circuit. The QV comparator is derived from differential comparator [5]. There are different types of encoder like Wallace tree encoder, PLA/ROM and XOR encoders. We use a pseudo-logic encoder which directly converts the thermometer code to binary code. It also provides high conversion data rates while maintaining low power consumption [8].

Thus, we propose a paper with 2.5v, 4-bit flash ADC using the pseudo logic encoder and QV comparator having a speed of 876 MSPS. 4-bit flash ADC has been designed and implemented on the 250nm CMOS process with the help of TANNER EDA tool.

II. PROBLEM STATEMENT

In various types of ADC, it is necessary to optimize the parameters like speed, power consumption, noise sensitivity, and size. The TIQ comparator and FAT Tree Encoder based flash type ADC provides improvement in static power consumption, size, and speed. But Further improvement is necessary for low power devices and SoC applications.

III. FLASH TYPE ADC WITH QUANTUM VOLTAGE COMPARATOR AND PSEUDO LOGIC ENCODER

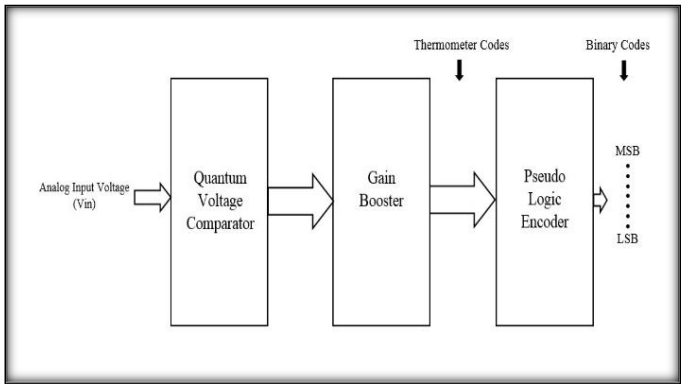

Fig.1: Basic block diagram of ADC

The flash type ADC with Quantum voltage comparator is described in above Fig.1, it encompassed Quantum voltage comparator, gain booster, and Pseudo logic encoder. The quantum voltage comparator induces thermometer code, this code is in the form of 0s and 1s which are then hand over to pseudo logic encoder. There are numerous encoders available, in this paper pseudo logic encoder replaces other encoders as it provides direct conversion of thermometer code to binary code with low power consumption.

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IV. QUANTUM VOLTAGE COMPARATOR

The TIQ comparator eliminates the resistor ladder network in conventional ADC as it generates reference voltage internally, it gives the improvement in static power consumption of a circuit. But the main problem regarding TIQ comparator is noise susceptibility [5]. As it has a single-ended structure, it is more sensitive to power supply noise as well as temperature variation makes the DNL and the INL increased in the TIQ comparator.

To overcome this disadvantage of TIQ comparator, Quantum voltage comparator is introduced. The Quantum voltage comparator uses the same technique as that of TIQ to generate the internal reference voltage.

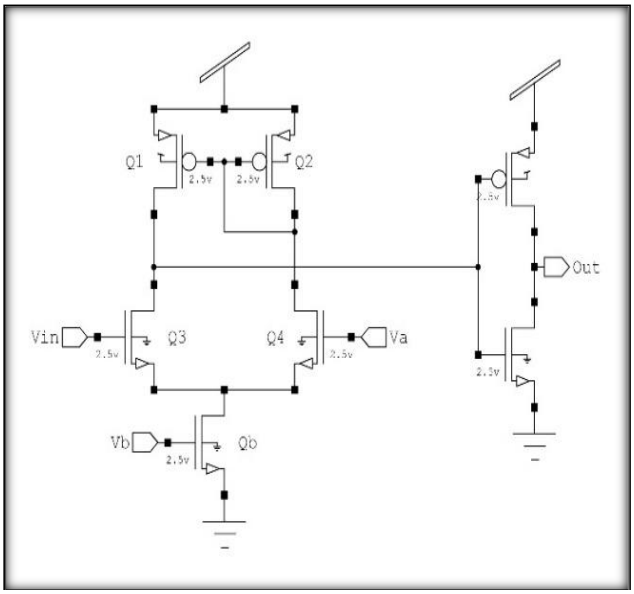

Fig.2: Quantum Voltage Comparator

The Quantum voltage comparator is derived from Differential comparator. In TIQ comparator, the different switching voltages are obtained by changing the size of transistors. This concept of generating reference voltage is used in Quantum voltage comparator. The following fig.2 shows Quantum voltage comparator. Design of various comparator carried out by changing the width of NMOS pair Q3, Q4 while keeping Q1, Q2 self-same. The mismatch in size of transistor provides different switching voltages for different comparators. For 4-Bit ADC 2^n-1 (i.e. 15) different size comparators are designed with different switching voltages. The input analog signal is applied to the 'Vin' terminal of the comparator while keeping 'Va' and 'Vb' constant [6]. Inverter followed by quantum voltage comparator is used to get sharper voltage transfer characteristics curve.

V. GAIN BOOSTER

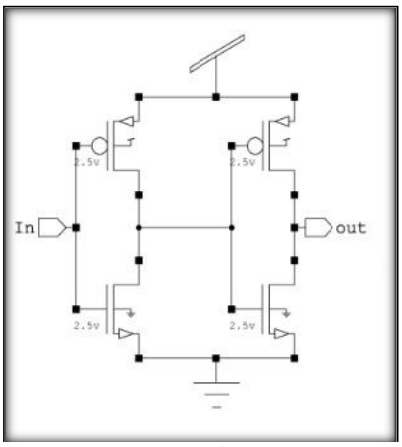

Fig.3: Schematic of Gain Booster

The gain booster circuit uses two inverters which are connected in series as shown in fig.3. The gain booster circuit increases voltage gain of comparator output which provides full digital output voltage swing [7]. The size of both inverters is small and both inverters are self-same. It also provides the sharper switching voltages. For 4-Bit ADC, there is a necessity of 2^n-1 i.e.15 different comparators, hence 15 gain boosters are also required.

VI. PSEUDO LOGIC ENCODER

The Pseudo logic encoder is executed the same as that of PLA design logic. This Encoder design uses AND-OR logic to convert the Thermometer code to Binary code. The encoder logic design for various bits is shown in figures 4, 5 and 6. The basic dissimilarity between PLA design and pseudo logic design is, PLA design gives output bit by making use of all bits of thermometer code but this pseudo-logic encoder makes use of only selective code bits.

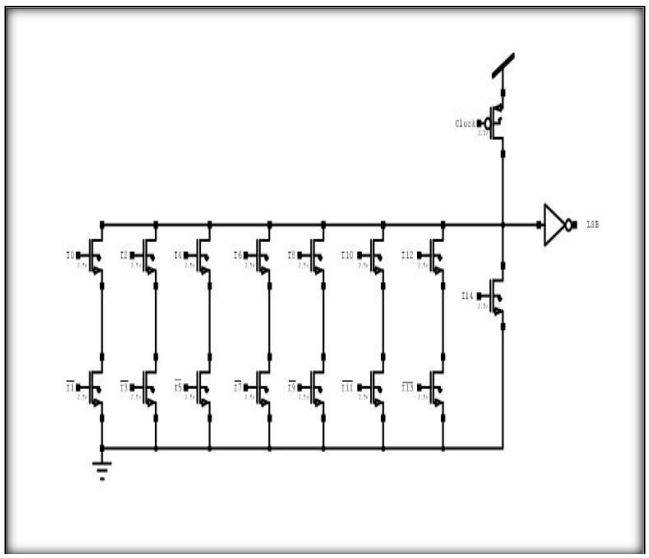

Fig.4: Implementation Schematic of LSB bit

International Journal of Engineering Research & Technology (IJERT)
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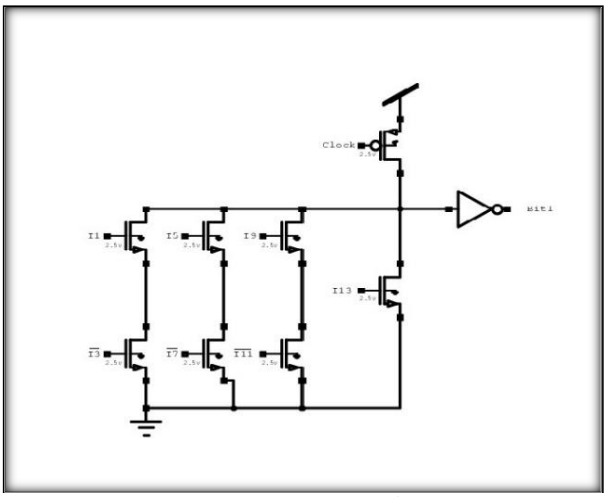

Fig.5: Implementation Schematic of BIT 0

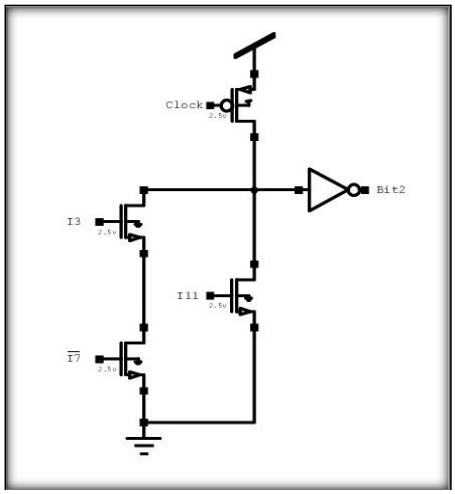

Fig.6: Implementation Schematic of BIT 1

The presented encoder is implemented using the following expressions:

LSB = I_0I_1'+ I_2I_3'+ I_4I_5'+ I_6I_7' +I_8I_9'+ $I_{10}I_{11}'$+ $I_{12}I_{13}'$+
I_{14}.

BIT 0 = I_1I_3'+ I_5I_7'+ I_9I_{11}'+ I_{13}.

BIT 1 = I_3I_7'+ I_{11}.

MSB = I_7.

For an N-bit flash ADC, the most significant bit of binary output is logic high if thermometer code traverse half of the length of thermometer code. Therefore, MSB bit is the same as that of 'I7'. The presented Encoder is executed using NMOS transistors and PMOS are used to the selective discharge of the output node.

Table 1 indicates the truth table of a pseudo logic encoder. The expressions of LSB, BIT0, BIT1, and MSB is obtained by using the following truth table [TABLE 1]. The circuit consists of clock driven PMOS. Inputs that are selective bits of thermometer codes are to be ORed using NMOS design logic which is connected in parallel and to do the AND operation of selective bits these are connected in series.

TABLE 1: TRUTH TABLE OF ENCODER

THERMOMETER CODES [I_{14} TO I_0]	ENCODER OUTPUT
000000000000000	0000
000000000000001	0001
000000000000011	0010
000000000000111	0011
000000000001111	0100
000000000011111	0101
000000000111111	0110
000000001111111	0111
000000011111111	1000
000000111111111	1001
000001111111111	1010
000011111111111	1011
000111111111111	1100
001111111111111	1101
011111111111111	1110
111111111111111	1111

VII. RESULT AND DISCUSSION

The design and simulation are done by using TANNER EDA tools. The designing of 4-bit ADC in the S-Edit window of TANNER EDA tool is shown in fig.6. The process used for designing ADC is 250nm, which is compatible with the manufacturing of various ICs or microchips. The encoder circuit has a composition of PMOS transistor which driven by clock along with a block of NMOS logic which defines the logic operations.

The Quantum Voltage comparator compares the input voltage with an internally induced reference voltage. The pseudo-logic encoder is realized with AND-OR logic. At the output of Pseudo logic encoder, digital data bits are observed as display in fig.8.

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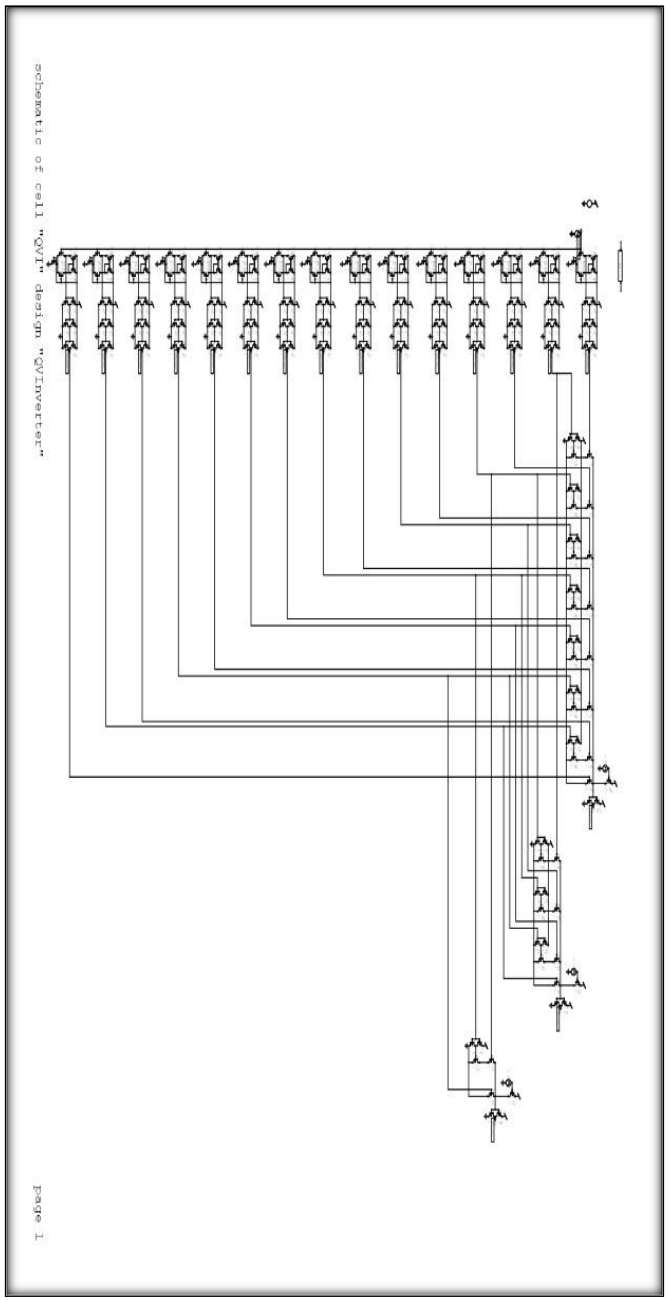

Fig.6: Schematic of 4-Bit ADC using QVC and Pseudo Logic encoder

The simulation results are noticed when the supply voltage VDD is equal to 2.5v. The frequency of input sinusoidal wave signal is 1MHz with input voltage having the amplitude of 750mv (Vin = 1.5VP-P). The fig.7 shows output voltage transfer curves which are observed on W-edit window of the simulation tool.

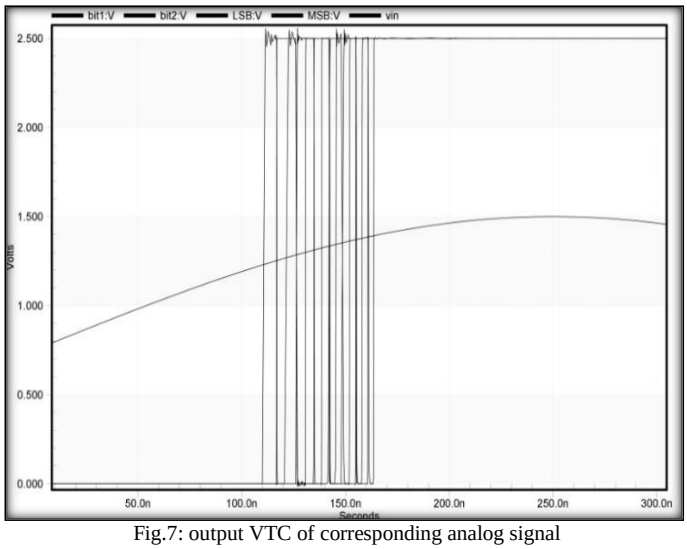

Fig.7: output VTC of corresponding analog signal

The conversion of an analog input sinusoidal wave signal to digital binary bits in the form of a graph is achieved on W-edit. The following Fig.8 represents a prosperous conversion of the analog signal. The TANNER EDA tool is used as a simulation tool because it provides full design flow from schematic design to layout verifications.

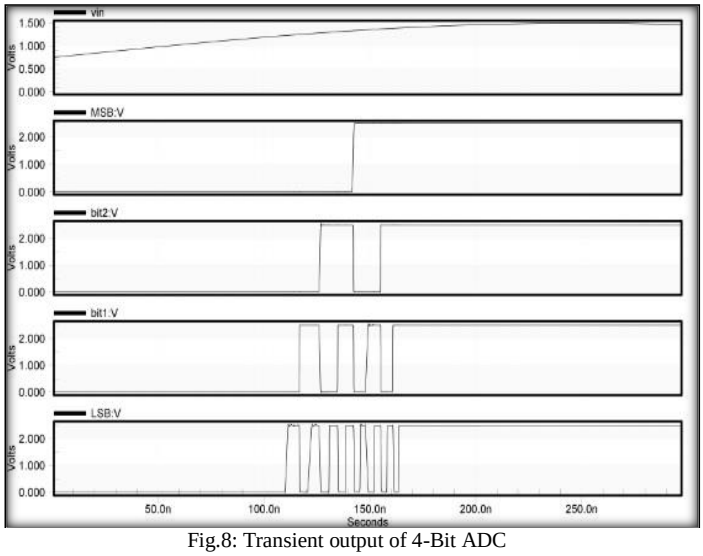

Fig.8: Transient output of 4-Bit ADC

VIII. CONCLUSION

The corresponding technique of reducing power consumption and improvement in the speed is carried out on 250nm CMOS technology and simulated on TANNER EDA tool. The demonstrated pseudo logic encoder with Quantum Voltage Comparator increases the speed and downgrades the power consumption. The Quantum Voltage comparator gives an efficient way to generate reference voltage internally as well as it effectively compares the input analog signal with a reference voltage. The result summary is shown in TABLE 2 which indicates the transistor count of presented design is reduced to 221 and the speed of 876 MSPS is successfully achieved by means of Quantum voltage comparator and Pseudo-logic encoder.

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TABLE 2: RESULT SUMMARY

Architecture	[3]	[4]	[4]	**Proposed**
Resolution (no. of output bits)	4-Bit	4-Bit	4-Bit	**4-Bit**
CMOS technology	250nm	250nm	250nm	**250nm**
Transistor count	-	436	436	**221**
Power supply (V_{DD})	2.5v	2.5	3.3	**2.5v**
Average power consumed	1.9mW	4.0890 mW	9.98 mW	**6.65mW**
Speed	3.0 MSPS	555 MSPS	690 MSPS	**876 MSPS**
Input Frequency	1MHz	1MHz	1MHz	**1MHz**

ACKNOWLEDGMENT

The authors are thankful to Dr. S.S. Khot, Principal of KJ College of Engineering and Management Research for his valuable guidance, support and continuous encouragement during completion of this paper. I am thankful to Prof. Rahimraja Shaikh, BE-Project Co-ordinator of our college for his valuable support, guidance and constant encouragement.

Lastly, we thanks to "KJ College of Engineering and Management Research, Pune" and well-wishers who have contributed directly or indirectly for successful completion of this paper. This is an explore to prove our technical skill for the advancement of social lifestyle.

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