Design of 8 Bit Current steering DAC

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Abstract—**Digital to analog Converter is a device that is used to convert digital signal to analog signal. In this Paper we will go through the analysis, design and simulation from supplies of 2.5volt and 5 volt.8 bit binary input ranges from 0 to 5 volt and clock can be as high as 50Mhz.The fact that current steering topology used for instead of R-2R topology gives good INL as well as DNL.Major glitching issues are eliminated by Register Section. The overall swing of 2 to 3 volt is achieved along with SNDR of 30 Db and LSB step of 8.3mvolt.It works like a interface between analog and digital world. It has four blocks,Register,decoder,current cell array and opamp, that produces analog voltage in form of output. Thus digital inputs are going to convert analog output.Speed,monotonicity and performance would be better than binary weighted ,ladder DAC.**

Keywords— **Current steering Design, Master slave register, Binary to thermometer Decoder, Current Cell Matrix, Current Cell Array, Current to voltage converter using opamp.**

I. INTRODUCTION

As we know that VLSI circuit are more progressing day by day, new technology changes, scenario changes, Design changes. There are many types of DAC are available. In Binary weighted DAC either current source or resistor bit is used for each bit, all connected through a summing point, which provides output.R-2R ladder DAC consist of structure of resistor value ,closely matched, binary weighted, having highly resolution. One New technique Delta and Sigma design is based on noise shaping and pulse density, gives lower resolution in forward path. Segmented design is hybrid design between binary weighted and thermometer decoded logic. It is the fastest and most precise technology.

II DESIGN

Segmentation is more needed when minimize glitches and nonlinearity. Initial topology that was chosen was a segmented one, which consists of binary weighted current cells or thermometer decoded cells. However only one or two bits are segmented.Glitching is not significantly reduced.Also,high resolution DAC are known to occupy less area on the die compared to non segmented counterpart. However it has 8 bit resolution, one should not expect major die area reduction in layout.

III. BLOCK DIAGRAM

Current cell:-The current cell consists of Digital and analog part. The digital part consists of the decoding logic with the clocked pass transistors to control switches and analog part consisting of cascaded current sources with the differential switch pair M1 and M2.The output current of all cells are summed and total current will be supplied to load resistors R1 and R2 converting into the output voltage.

DAC architecture :-The proposed Block diagram shown in figure. This design chooses unit element current steering technology.There are four major portions in this figure. They are register ,Binary to thermometer decoder, current source array, differential opamp. 8-bit digital inputs' glitches can be eliminated after registers, and by decoders, they are changed to 15*15 thermometer signals. These signals perform as controlled codes to determine how many current cells are on/ off and the values of Iout and Iout_neg. Finally, in the last stage, the difference between the inputs of differential amplifiers can be amplified and serve as the analog output. The Block diagram is shown below.
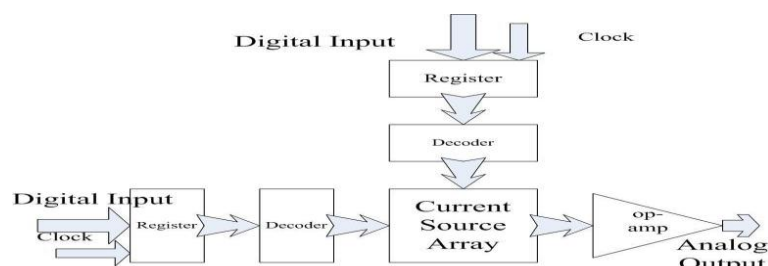
Figure1:Block diagram of current steering DAC

A. Register:-Register is used as a elementary component that is used to store the data. Basically it works as a storage element, where input bit is stored. It depends on the type of DAC, like in 8 bit DAC it is of 8 bit, but in case of 16 bit, it is of 16 bit. Here we are using 8 bit register. After all it is used to increase resolution. Next block is Binary to thermometer decoder that is by binary to analog code generates. So it transfers digital bits to next block i.e. binary to thermometer decoder. Here there are may be many types of analog and digital registers. Without the DAC register, the output of the DAC would change immediately with any changes on the external input bus, due to the real-time feeding of the analog circuitry. The data stays in the DAC register until the user decides to update the DAC register with new code. The DAC register essentially acts like a flip-flop. Register block is shown below in which master slave register configuration is used. Here there are two blocks is used that is on by left and off by right, and vicecersa.It is like the operation of Master Slave register.
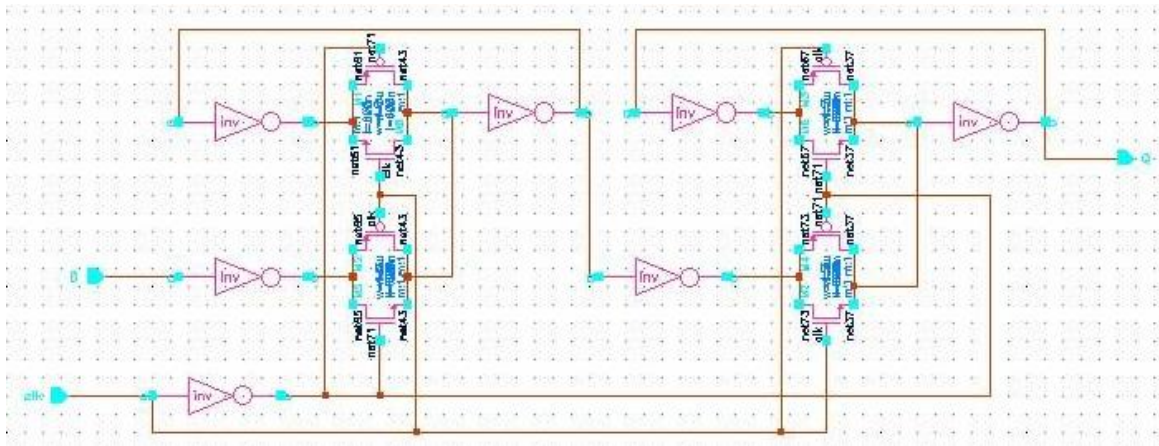

Figure2:-Master slave register

B. Binary To Thermometer decoder:-It is quite difficult to convert the digital to analog signal rather than analog to digital. So to perform this We use one technique or configuration called Binary to Thermometer Decoder logic. Large memory blocks can program the thermometer switching sequence but at a price of doubling silicon area. In this technique we use row or column decoder as a elementary block. There are some important points. To design this we ensure that only one bit changes per state.Multibit changes simultaneously causes big glitches. Use of Row and column decoder keeps layout compact. In this architecture row decoder, column decoder ,array cell and multiple gates are used. The given observation table or truth table is shown below.

Binary	Thermometer
0000	000 0000 0000 0000
0001	000 0000 0000 0001
0010	000 0000 0000 0011
0011	000 0000 0000 0111
0100	000 0000 0000 1111
0101	000 0000 0001 1111
0110	000 0000 0011 1111
0111	000 0000 0111 1111
1000	000 0000 1111 1111
1001	000 0001 1111 1111
1010	000 0011 1111 1111
1011	000 0111 1111 1111
1100	000 1111 1111 1111
1101	001 1111 1111 1111
1110	011 1111 1111 1111
1111	111 1111 1111 1111

Figure3:Truth table

To get the following truth table, we design a decoder circuit. It is not a fixed circuit ,it can be changed by user.
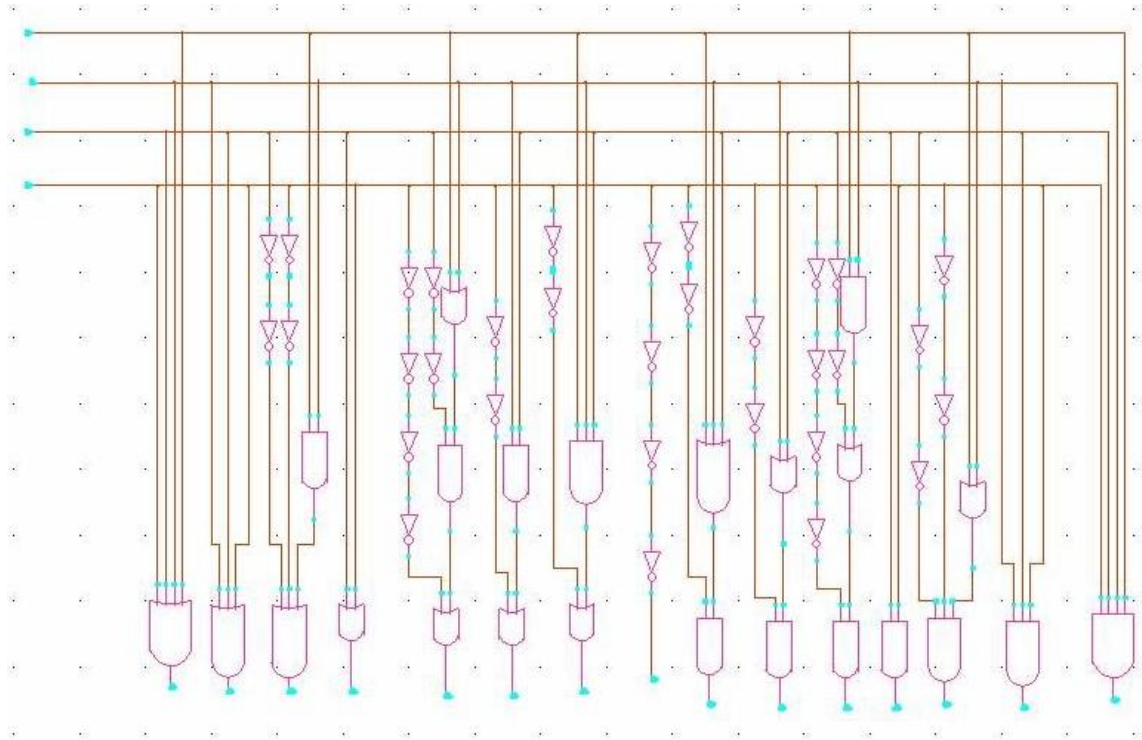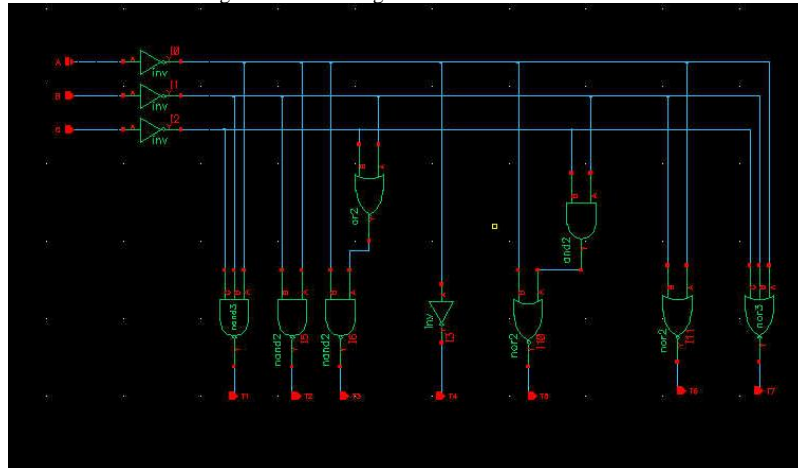
Figure 4**.**Three D/A functions for a DAC, as designed (straight *line*), empirical ideally linear
(Dashed *line*), and empirical (non-*linear graph*, derived from measurements with
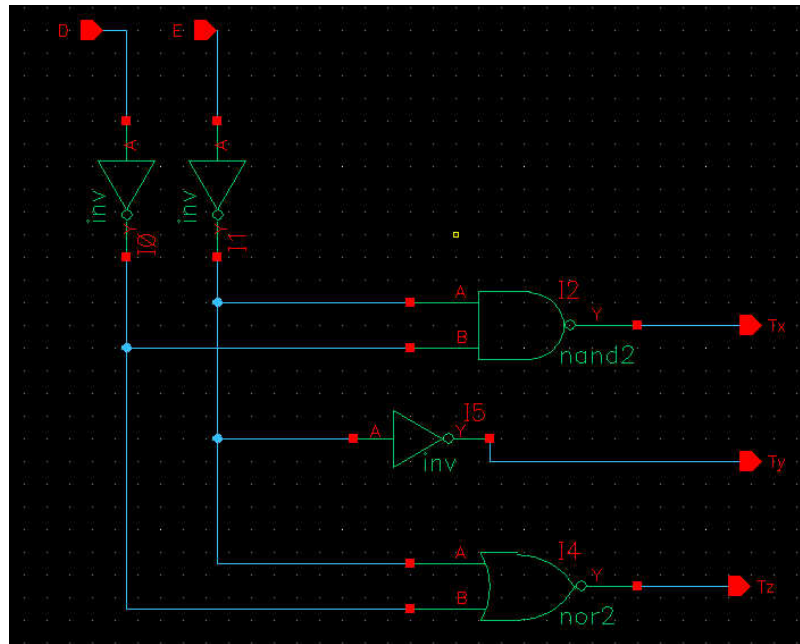
Figure4:-Circuit diagram of Decoder

Figure5(a) Row decoder and Figure5(b) Column decoder

C. Current Cell Array:-Current cell array is used to perform sum of all analog currents .It is basically combination of blocks. In current cell high impedance current mirror will be needed to help reduce the currents, sensitivity to the output voltage and Thus reduce current glitches that might occur because of change in output voltage. It is basically used for amplification purpose.Setting the unit cell's current to 20µA is a good decision because the largest current will end up being 2.56mA according to Eq. therefore the power requirements of the chip can be kept quite low. Another reason for not designing with a lower current is the fact that one would need to implement either a widlar current source or a peaking source to achieve a supply-insensitive current of less than 20µA, therefore for design simplicity, this was the value of the lowest current in the current array.

$$\text{Iout m}= 2^{m}\text{ Iin(In case of Binary current cell array)}$$
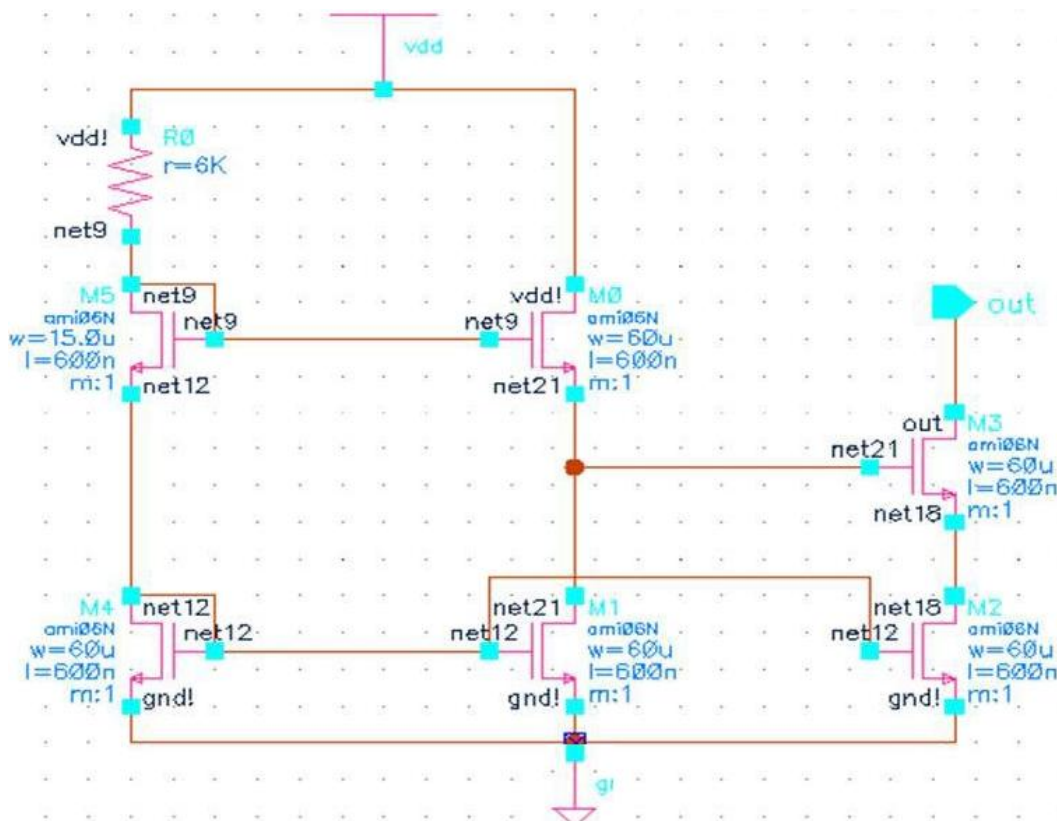
The current cell array is shown below.

Figure6:-Current Cell array

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D.OPAMP:- The input stage of the Op Amp is a standard differential pair with a cascoded tail source to improve the CMRR. It can be seen from Eq. that the higher the r_{tail} lower the CM gain, and therefore the higher the CMRR is.

$$CM = 1/(2*g_m*r_{tail})$$

The resistive bias circuitry is set to run a 100µA tail current in the differential pair. Keeping the tail current low is preferred since the gain is inversely proportional to the square root of the current. Eq. 7 is an expression for the open loop gain of this stage.

It is used as current to voltage converter. The circuit diagram of a current-to-voltage converter is shown in Fig. . The circuit is a special case of an inverting amplifier where the input resistor is replaced with a short circuit. Because the v terminals a virtual ground, the input resistance is zero. The output resistance is also zero. Because i= 0 and vO= iFRF, it follows that the trans résistance gain is given byi1= -RF Figure shows the current-to-voltage converter with a current source connected to its input. Because Rs connects from a virtual ground to ground, the current through Rsis zero. It follows that I and vO= -RFis. Thus the output voltage is independent of R

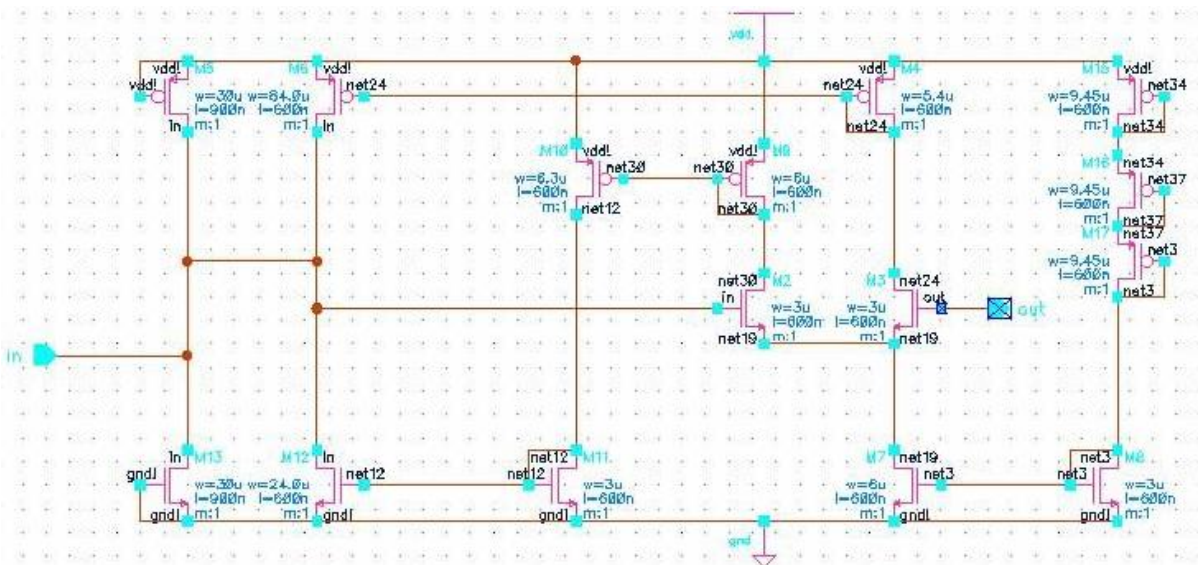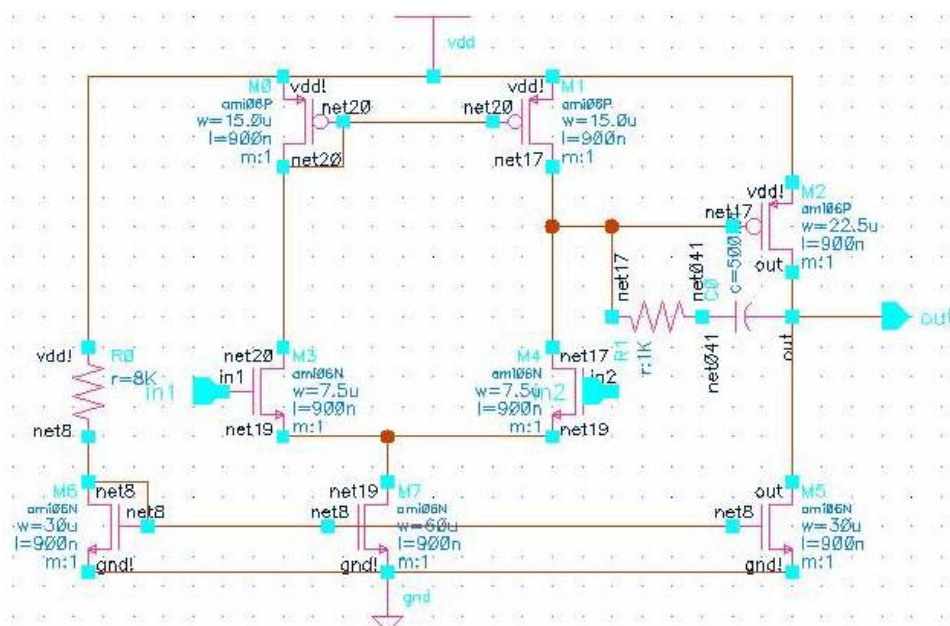Figure7:Opamp Configuration

IVCurrent-Steering DAC Specification

Digital-to-Analog Converters (DACs) implement a Digital-to-Analog (D/ A) con-version function, see Fig.7. The arguments of this function are digital data, reference clock and reference amplitude (unit) .The output of the D/A function is the DAC analog output signal. The input signal is discrete in time and quantized in amplitude, coded in digital bits. The time-reference for the DAC is provided by its input clock signalA. Static Characterization -

For a static characterization, the main representation of the D/A function is given by the D/A transfer characteristic. Figure.8 illustrates a D/A transfer characteristic which is derived from real test-chip measurements with magnified non-linearity by a factor of 150. The plot provides the static relation between the DAC input codes (x axis) and the DAC output analog value (y axis, representing the DAC differential output voltage). The x axis is discrete and is only defined around the possible digital input codes, represented as bins in a plot. The number of bins is usually determined by the DAC resolution. The example of Fig. 8 shows a 12 bit DAC. The y axis is continuous. The maximal value of the D/A function on the y axis represents the DAC full-scale (FS) range.
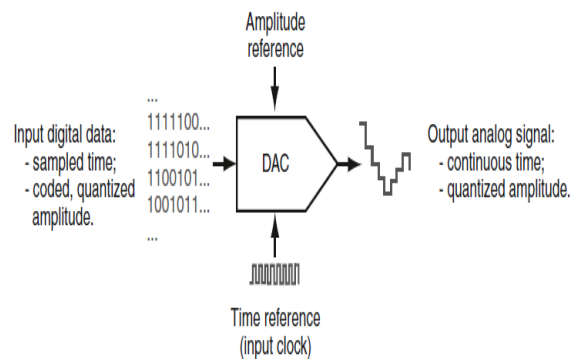

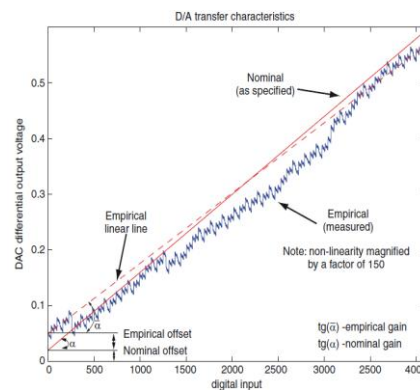Figure 7 the DAC as black box: input-to-output transformation

Figure 8.Three D/A functions for a DAC, as designed (straight *line*), empirical ideally linear
(Dashed *line*), and empirical (non-*linear graph*, derived from measurements with
Non-linearity magnified by a factor of 150)

The difference between the empirical ideal linear line and the empirical D/A transfer characteristic shows the DAC non-linearity. For a proper reading of the DAC non-linearity, usually it is normalized to the LSB step of the DAC output. In such a way the DAC INL (Integrated Non-Linearity), shown in Fig. 9, is defined. The straight line in Fig. 9 is the nominally expected D/A transfer characteristic. It describes the ideal linear relation between the digital input and analog output. Several specifications can be defined, e.g. offset, gain, FS range. The non-linear graph is the actual, e.g. measured, D/A transfer characteristic. For the example of Fig. 9, it is based on real measurement results of a 12 bit DAC with a magnified non-linearity by a factor of 150. The offset, gain and FS specification need to be defined based on the real measurement data. There are a number of ways to define these specifications. These depend on the way the empirical linear equivalent of the actual D/A transfer characteristic is defined. Without loss of generality, in this book the line connecting the initial and final points of the actual D/A transfer characteristic is used.

LSB step of the DAC output. In such a way the DAC INL (Integrated Non-Linearity), shown in Fig. 8, is used.
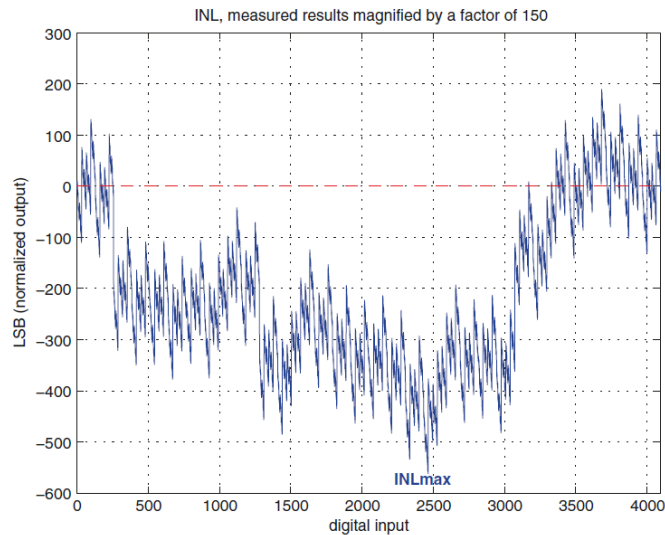
Figure 9.12bit DAC INL

B. DAC DNL -

The evaluation of the INL usually includes two main properties: the global shape of
The graph and its deviation from the straight line. The shape of the graph indicates the dominant order of the DAC non-linearity. For example, the shape shown in Fig.5would suggests a strong second-order non-linearity. The deviation from the straight line indicates how strong the non-linearity is and hence how linear the DAC is. For example, the deviation shown in Fig.10 is about−500 LSB, which suggests a linearity that is 10 bit less than the resolution, i.e. 2 bit DAC linearity.

For many DAC applications, e.g. control and self-calibration as shown further in the book, the local behavior of the INL graph is important, i.e. the linearity between successive DAC code transitions. This can be characterized by the DAC DNL (Differential-Non-Linearity). The DNL characterizes the non-linearity for each LSB step. The DNL at code k equals the difference between the two code-consecutive INL values at codes $k + 1$ and k:

$$DNLk = INLk+1 − INLk \qquad (1.1)$$

Figure6 shows the corresponding DNL characteristic of the D/A transfer characteristic of Fig.4 and the INL characteristic of Fig 10. The DAC DNL is usually used to indicate DAC local errors. For example a large deviation for a given DAC analog unit is directly indicated as a spike in the graph. Another commonly used criterion is the DAC monotonicity. A DAC is monotonic if DNL_k −1 for all k.

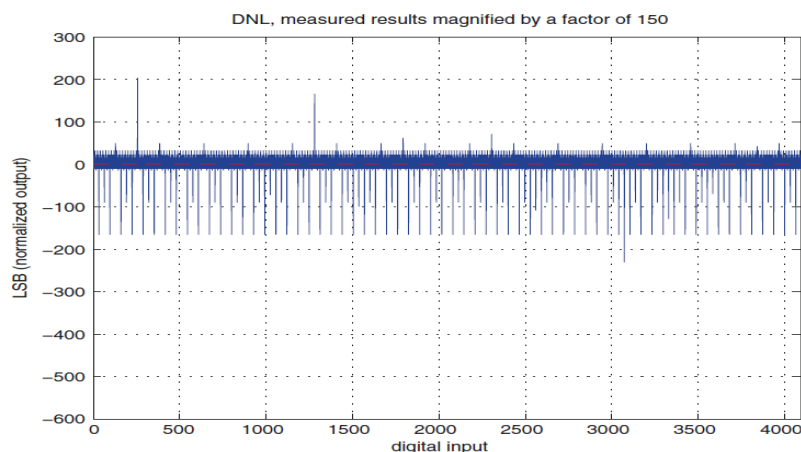
Figure10.12 bit DAC DNL

The opposite, the non-monotonicity, is a strongly non-linear condition of the D/A transfer characteristic featuring a local gain with opposite sign. That is to say that an input digital code $x_1 \square x_2$ is converted to DAC output $y(x_1) \square y(x_2)$, while the overall DAC gain is positive.

C.Dynamic Characterization -

For the dynamic DAC characterization, many figures are widely used, depending on the DAC application and its requirements. For example, audio and video applications require strict specifications for glitch energy between the code transitions; radio-frequency (RF) communication applications require strict specifications for DAC dynamic linearity; digital communication applications require strict specifications on FS high-speed specifications eye patterns. This considers the DAC dynamic linearity group of figures, since they are very important in the RF communication applications. Figure 11 shows an exemplary spectrum of a DAC sine wave output signal.SFDR (Spurious-Free-Dynamic Range), HD (Harmonic Distortion), and

IMD (Inter-Modulation Distortion) are the most important parameter. The most popular implementations include switched-capacitor DACs, resistor-based DACs and current- steering DACs. The charge-redistribution DAC is a switched-capacitor (SC) circuit, implementing DA conversion in the charge domain . Usually, charges stored on a number of capacitors are used to perform the required conversion. Figure shows an example of a differential charge-redistribution DAC. Its output signal is generated by an amplifier, the speed and the linearity of which are usually the main performance limitations. Furthermore, the performance of these converters is also constrained in accuracy due to the finite matching of the capacitors. The R-2R ladder is a simple approach to implement DACs. Its basic principles are outlined. When a voltage is applied to node 6 in the circuit, a binary voltage scale builds up along the upper nodes. The same applies to the currents flowing in the vertical resistances 2R. The binary weighted currents flowing through the vertical resistances 2R can be selected and combined
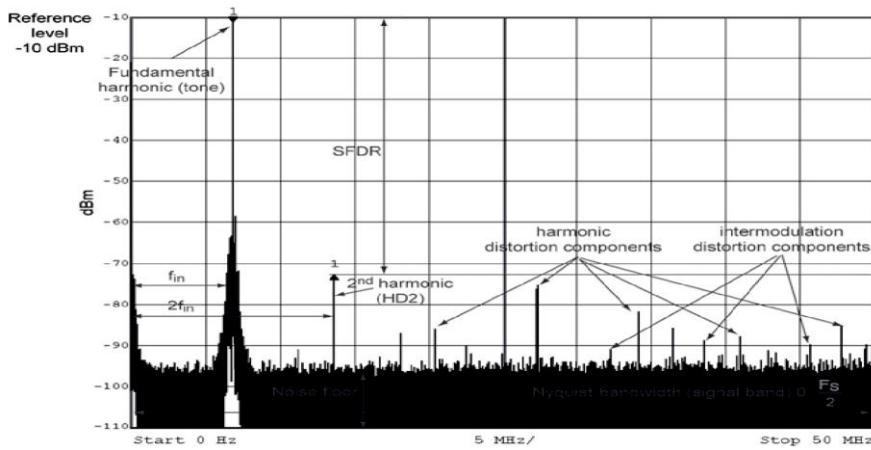

Figure11:Simulation Result of Dynamic chara,

V.RESULT & SIMULATION

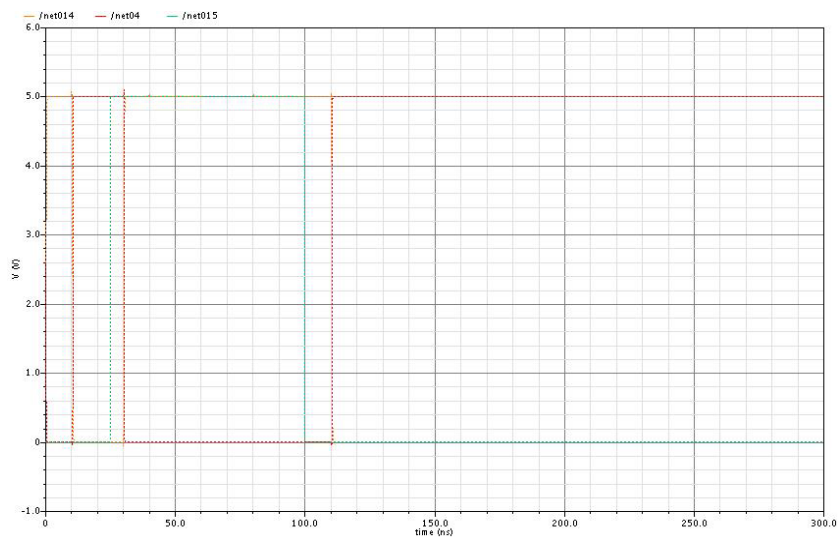1. Master & Slave Register:-The simulation result is shown below.

Figure12:Simulation Result Of Register

Red line shows input and green line shows clock signal ie constant.

2.Binary to thermometer decoder:-Simulation result of inpit and output b15 in one period
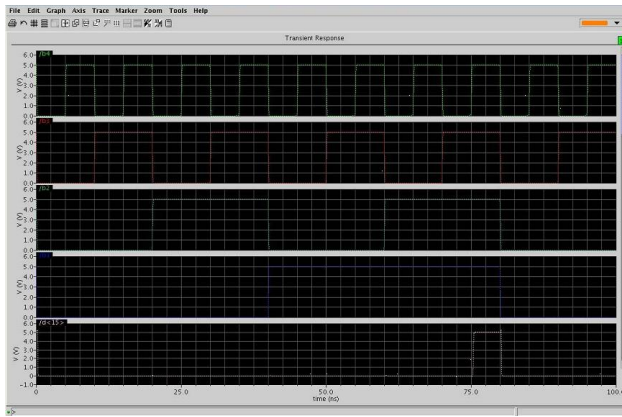
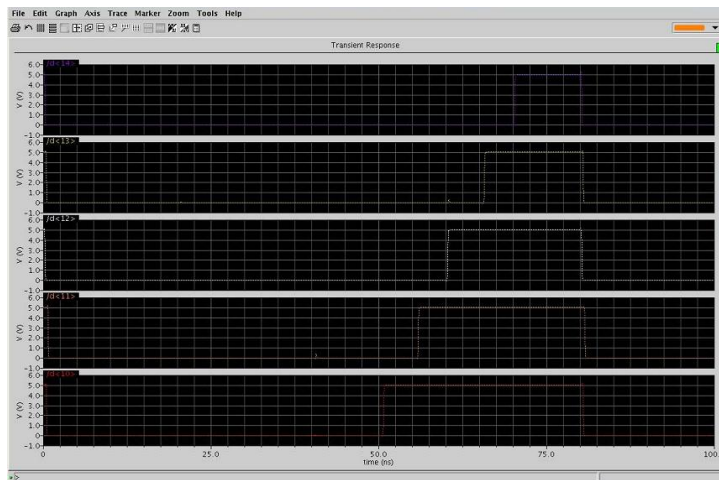Figure13:- simulation result of b10-b14 is shown below.

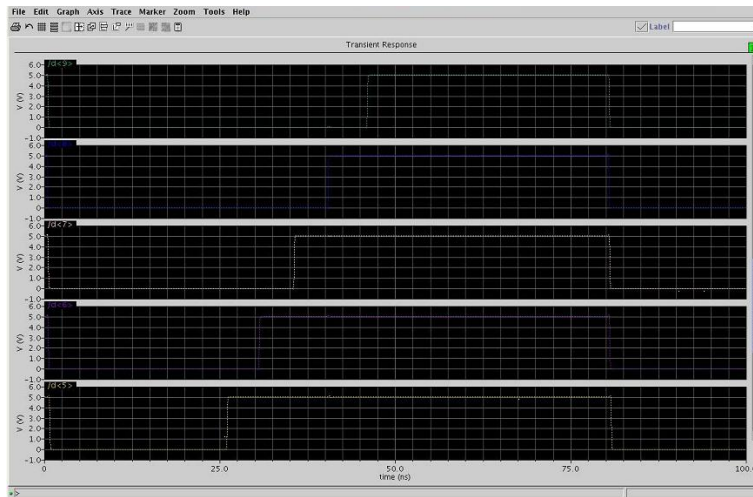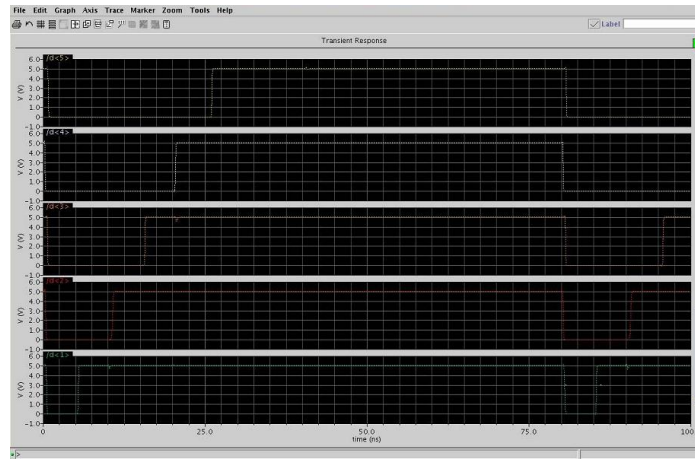Figure 14:-Simulation result of b9-b5 in one period.

Figure15:-Simulation result of b4-b1 in one period is therefore.

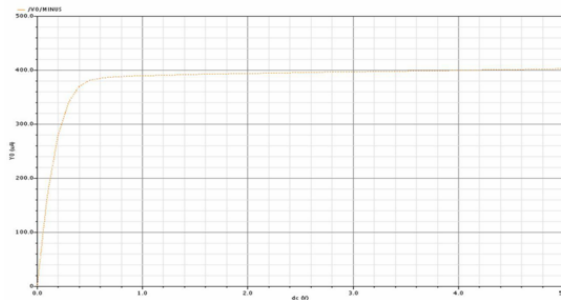C.Current Source array:-The analog simulated current is shown below.

Figure17:Simulation result of Current

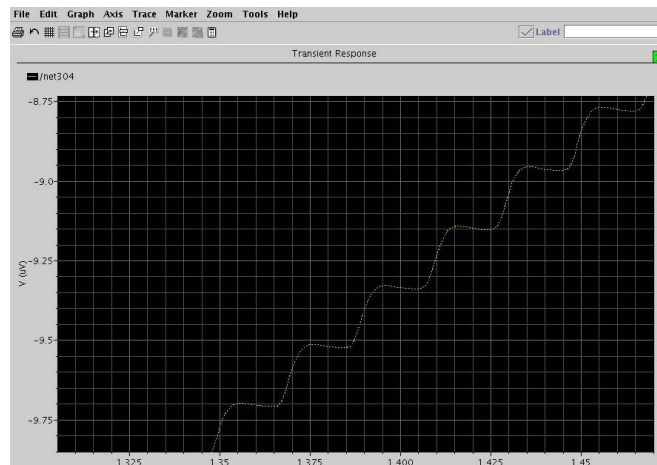D.OPAMP:The analog current is converted in to analog voltage is shown by graph at 50 MHz.

Figure18:-Analog voltage

V.References

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