DESIGN OF 8 BIT 80MHz SAMPLE AND HOLD FOR SAR ADC

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Abstract—**Successive-approximation-register ADCs are frequent architecture of choice for medium to high-resolution applications. SAR ADC operates by using a binary search algorithm to converge on the input signal. SAR ADC contains 80MHz Sample and hold circuit, capacitive DAC, high speed comparator and SAR logic block. Design analysis and simulations presented, demonstrate the sample and hold which conform to the specifications for application in the 8-bit 80MHz SAR ADC converter with supply voltage of 1.2V.**

I. INTRODUCTION

Signals in the real world tend to be analog. In order to process them with a digital circuit, need to convert them to digital signals. Analog to digital converters (ADCs) have relevant significance in all those applications in which, there is an interfacing of analog real world signals with the digital processing of data. An Analog to Digital Converter (ADC) takes an analog input signal and converts it into a digital output signal. The three conceptual steps that occur in ADCs are

1. The signal is sampled
2. The sampled signal is quantized
3. The quantized signal is digitally coded

II. SAR ADC

Successive-approximation analog to digital converters are one of the most popular converter types because of its simple design and relatively high speed. The key to the successive-approximation converter is an algorithm referred to as a binary search[1]. They have relatively quick conversion time, yet moderate circuit complexity [1]. The conventional structure of an SAR ADC, as shown in Figure 1, consists of a sample-and-hold (S/H) circuit, a comparator, a successive approximation register (SAR) and a digital to analog converter (DAC). Overall accuracy and linearity of the SAR ADC are determined primarily by the internal DAC.

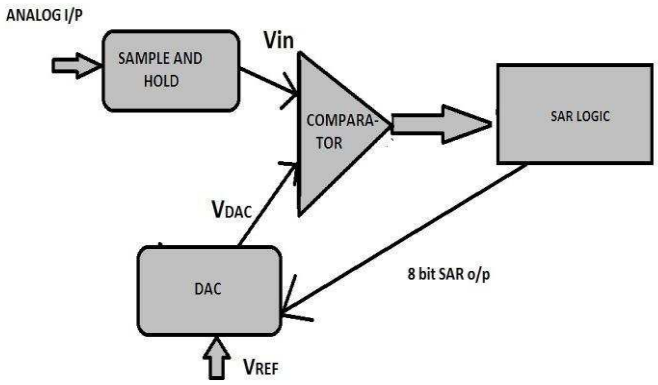

Figure:.1 Structure of an SAR ADC

The analog input voltage (Vin) is held on the track and hold. To implement the binary search algorithm, the 8-bit register is first set to midscale (that is, 10000000, where the MSB is set to 1). This forces the DAC output (VDAC) to be VREF /2, where VREF /2 is the reference voltage provided to the ADC. A comparison is then performed to determine if Vin is less than, or greater than VDAC. If Vin is greater than VDAC, the comparator output is a logic high, or 1 and the MSB of the 8-bit register remains at 1. Conversely, if Vin is less than VDAC, the comparator output is a logic low and the MSB of the register is cleared to logic 0. The SAR control logic then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the LSB. Once this is done, the conversion is complete and the 8-bit digital word is available in the register.

A. Capacitive DAC

The Switched-Capacitor (SC) DAC is best suited for low power application. From the MATLAB analysis, it is clear that binary weighted DAC[2] is advantageous than that of thermometric. An N-bit binary weighted DAC comprises of N capacitors having capacitance value ranging from C, 2C, 4C, 8C… $2^{(N-1)}$C [2] . Binary weighted DAC consists of capacitors in which each higher-rank capacitor is equal to the sum in value of all the lower-rank capacitors. A dummy capacitor having the value of unit capacitance is used to maintain the balance.

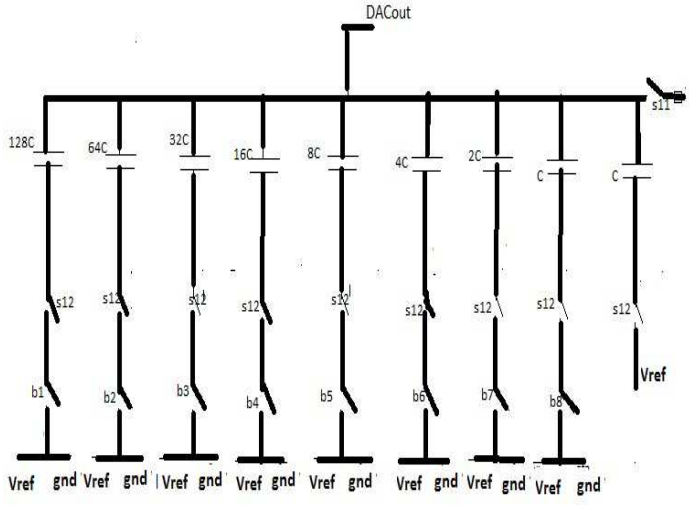

Figure 2: 8 bit Binary Weighted Capacitive DAC

During the sampling mode input signal get sampled at 80MHz frequency and sample so obtained will be kept so until 8 conversion clock cycles. So the operation will takes place in a total of 9 clock cycles. During the sampling mode switch S_{11} is connected to ground (GND). During the holding mode, S_{11} switch get opened and then S12 at the dummy gets connected to GND and S_{12}. switches at other capacitors connected to reference voltage levels Vref or GND according to bits b1,b2,.....b8 from the SAR logic.

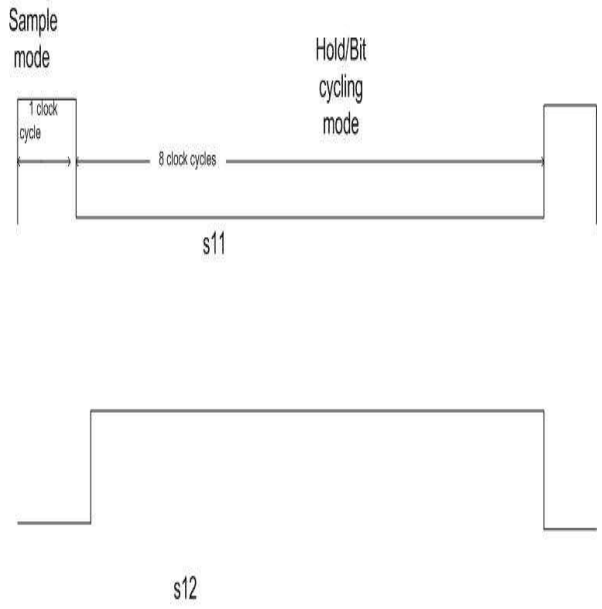

Figure 3: clocks

III. SAMPLE AND HOLD

In many cases, use of S/H (at the front of the data converter can greatly minimize errors due to slightly different delay times in the internal operation of the converter). It is an analog building block with many applications. It samples an analog input signal and hold this value over a certain length of time for subsequent processing. Switched capacitor based sample and hold is implemented here because of the excellent properties of MOS capacitors and switches. Without using sample and hold, the ADC cannot make correct decision because the analog input is changing the value instantaneously. If we are sampling the value of an analog input and holding the value for sometime so that ADC gets enough time to take decision. So we are using sample and hold circuit. There are factors such as dynamic range, slew rate, 3db bandwidth linearity, gain, noise, and offset error which affect the performance of S/H

Clock = 80MHz
V ref = 1.2V
Number of bits = 8
V inp = 800mV
V inn = 400mV
Sampling Frequency=80 MHz
Clock period=1/80 MHz=12.5 ns is available for sampling and holding operation. But for 8 bit SAR ADC sampling operation is takes place in one clock cycle and holding operation takes place in remaining 8 clock cycles.
So sampling clock = 9/12.5ns = 1.38ns
Holding clock= 12.5ns-1.38ns = 11.1ns.

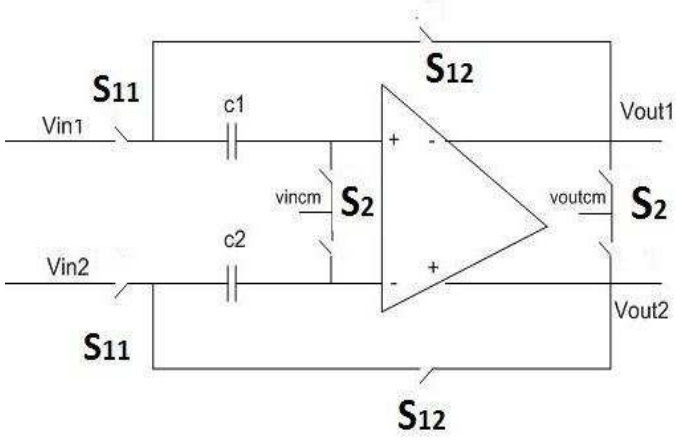

Figure 4: Sample and Hold Circuit

Here we are providing two common modes- input common mode and output common mode. During the sample mode, the switches S_{11} and S_2 get closed and switch S_{12} is opened and the capacitors c1 and c2 get charged to Vin-Vincm. During the hold mode, the switches S_{11} and S_2 get opened and switch S12

gets closed. During this time the output gets charged to Voutcm-(Vin-Vincm).During the sample phase, the switches S11 and c2 get closed at the same time. During the hold phase, the c2 gets opened earlier in order to avoid charge injection. That is during the starting of hold mode there is a chance that a charge packet will move from input to the capacitor causing a change in the stored charge. But if the switch c2 opens earlier, there is no path for the capacitor to get charge, so charge injection effect can be avoided.

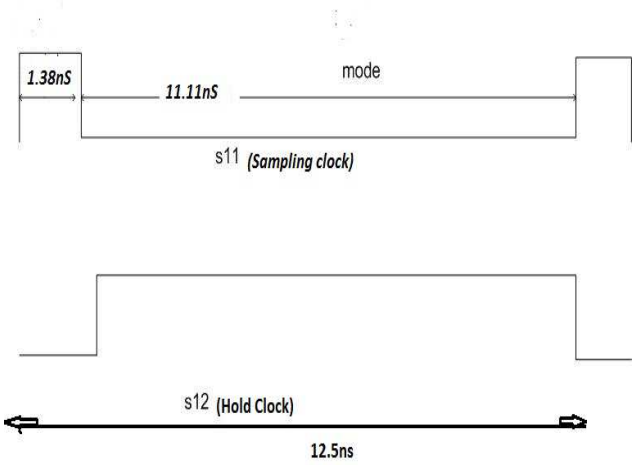

Figure 5: Clock for sample and hold

IV. OP AMPS

A. Op-amp requirement for Sample and Hold (S/H)

The gain and bandwidth characteristics are crucial in the design of S/H circuits in data converters. The op-amp is preferred to have a phase margin of 60º over full load conditions and process variations to avoid second order step response and its associated ringing. Decreasing the phase margin results in an increase of amplitude of ringing and this can increase the settling time. It can be proved that the DC open loop gain of an op-amp used in an ADC must satisfy the condition Aol >= $(2)^{(N+2)}$ Where N is the number of bits of conversion. For example, a 8 Bit data converter needs a minimum DC open loop gain of $(2)^{10}$. The speed of an op-amp is decided by the op-amp used.

B. Op-amp topology selection

Choose the appropriate architecture for op amp, one should first notice the requirements of the system. There are several op-amp topologies possible like Two stage CMOS op-amp, Regulated cascode op-amp, Folded cascade op-amp Telescopic cascode op-amp etc. Folded cascode op-amp provides higher output swing compared to telescopic cascode op-amp and better PSRR and speed over two stage op-amp. Hence folded cascode op-amp is used here.

C. Folded cascode op-amp

The input stage provides the gain of the operational amplifier. Due to the greater mobility of NMOS device, PMOS input differential pair presents a lower transchalf saree bollywood mode
onductance than carrier a NMOS pair. Thus, NMOS transistor has been chosen to ensure the largest gain required.[3]

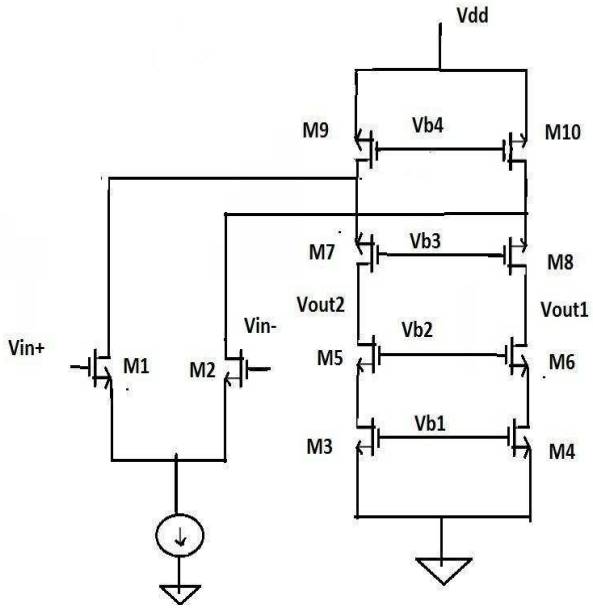

Figure 6: Folded cascode Op Amp

D. Design Procedure

- Power (P) = 2.5mW, Vdd (V) = 1.2V Power = Vdd*I
  ie, I = P/Vdd ie, 2.5 Mw / 1.2V = 2.08mA
  ie, tail current is taken as 2mA
- Required swing is 0 .6V
- A marginal value of 50mV is applied to each transistor on each side 50mv*4=0.2V
- Total voltage available for Vdsat is given as
  1.2-0.4-.2=.6V = 600 mV
  VdsatM9 +VdsatM7 +VdsatM5 + VdsatM3 =600mV
- Vdsat of current mirror transistor = 200 mV
- Vdsat of PMOS = 2* Vdsat of NMOS
- 2*V_{dsatM3} + 2*V_{dsatM5} +V_{dsatM5} +V_{dsatM3} =600mV
- 6* Vdsat = 600 mV
  Therefore Vdsat =100 mV for NMOS

For PMOS Vdsat = 2*Vdsat of NMOS = 200

From this we can calculate the bias voltages and the width and length of each transistor so that each transistor operates in the saturation region. Width and length are calculated with the help of equation of current in saturation region

$$I_D = 1/(2\mu nCoxW/L(V_{GS}-V_{TH})^2)$$

Obtained gain 62dB

Phase Margin 33.88

D. Compensation

The system is unstable since gain crossover lies outside the phase crossover. So we should do compensation. In folded cascode compensation can be easily achieved by increasing load capacitance value. It will increase phase margin also.
Gain=62dB
Bandwidth=1.75GHz
Value of capacitance=3pF
Phase margin after compensation=62.35, so overshoot of the system is reduced

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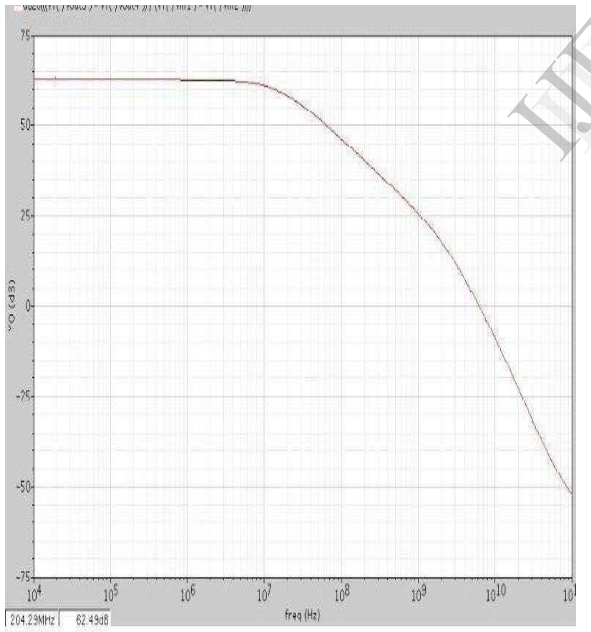

Figure 7: Gain plot

V. COMMON MODE FEEDBACK

The output node voltage should be always constant irrespective of process variation. But due to mismatches, the output node voltage gets shifted from the nominal value. In this condition, to stabilize the output we are making use of common mode feedback. This is usually chosen as a reference voltage yielding maximum differential voltage gain and/or maximum output voltage swing. Here the common mode feedback is achieved by controlling the bias voltage of M9 and M_{10} (V_{B4}) . To overcome Op-amp output swing limitation and to avoid resistive output loading of the op amp, capacitors can be used to detect CM output voltage.[3]

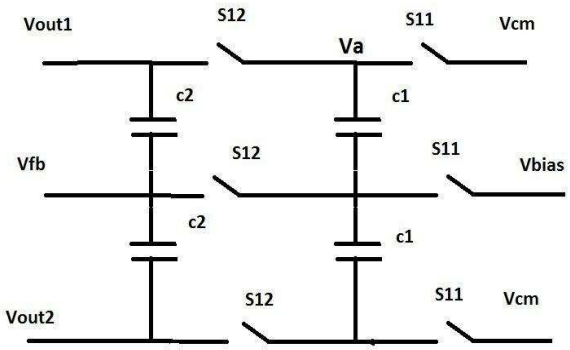

Figure 8 : Switched capacitor CMFB

CMFB Circuit consists of switches S_{11} and S_{12} and capacitors C_1 andC_2. Which sense the CM output voltage and subtract it from desired CM output voltage Vcm. S_{11} and S_{12} are non overlapping clocks where Vbias is the DC bias voltage(Vb4).

C_1 charges to Vcm-Vbias during S_{11}. During S_{12}, C_1 connects between Vfb and Va. Va is constant because applied voltages are DC voltages. C_1 does not transfer charges to C_2, after Vfb become constant[4]. Under this condition charge on these two switches become same.
That is Vcm-Vbias =Vfb-Va :
If Vfb equals the nominal bias voltage required at common mode, Vcm is almost constant with Vfb. Hence Vcm = Vbias

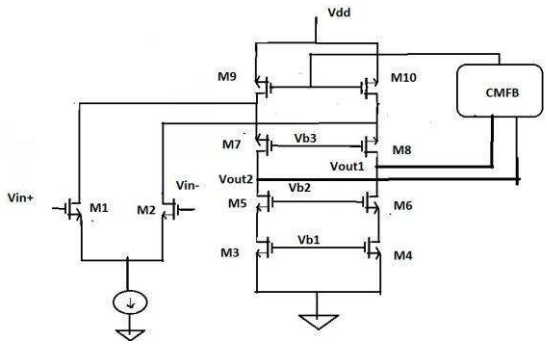

Figure 9: Op-amp with CMFB

Total gain of the op amp is 62dB
Phase Margin is 62.35
Unity gain bandwidth is 1.03GHz

VI. SIMULATION RESULT

Clock generator output which produces S11, S12 (S11 is created by D flip flop and its inverting signal gives S12) and S for 8bit 80MHz SAR ADC is shown below
Period of each clock= 12.5ns
Pulse width of S11 = 1.38ns

Pulse width of S12 = 11.11ns

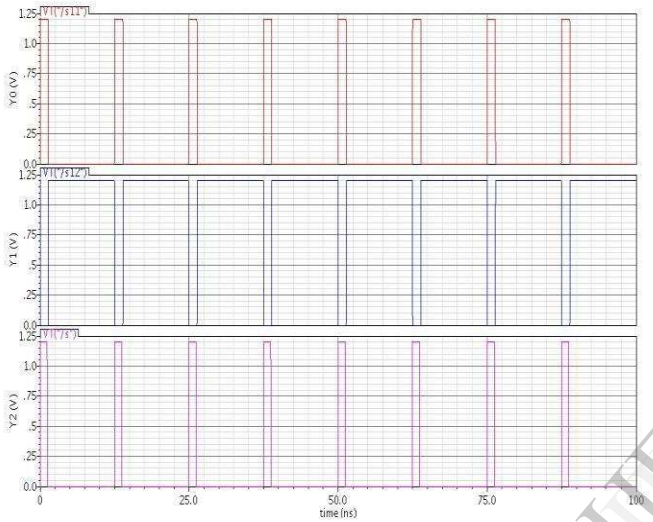

Figure 10: Clock generator

Sample and Hold outputs for 1bit SAR ADC and 8bit 80MHz SAR ADC is shown in succeeding three figures

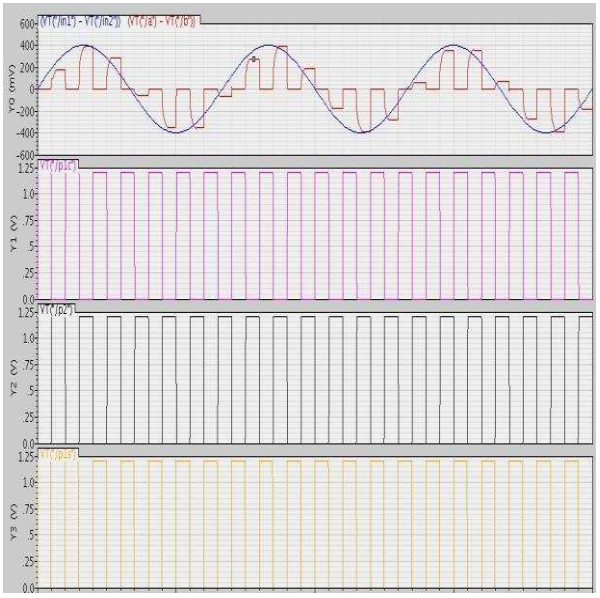

Figure 11: Sample and Hold for 1bit SAR ADC

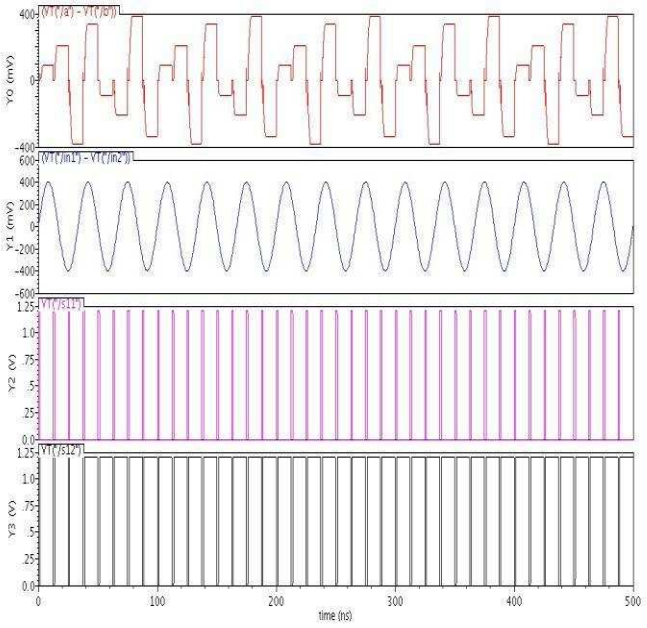

Figure 12: Sample and Hold for 8 bit 80MHz SAR ADC

References

[1] Applying the "Split-ADC" Architecture to a 16 bit, 1MS/s differential Successive Approximation Analog-to-Digital Converter by Chilann, Ka Yan Chan

[2] Split Capacitor DAC Mismatch Calibration in Successive Approximation ADC Yanfei Chen1, Xiaolei Zhu1, Hirotaka Tamura2, MasayaKibune2, Yasumoto Tomita2, Takayuki Hamada2, Masato Yoshioka2, Kiyoshi Ishikawa2, Takeshi Takayama2, Junji Ogawa2, Sanroku Tsukamoto2 and Tadahiro Kuroda1 1Keio University

[3] Design of a High-Gain Single Stage CMOS Differential Amplifier with Folded Cascode and Gain-Boosting By Jimmy Yu , Gary Sun, and Matthew ,The University of Michigan College Ng, Department of Electrical Engineering and Computer Science

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