Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 11 Issue 05, May-2022

Design of 6T SRAM

V. Panduranga Vemula
Department of ECE
CMRCET, Hyderabad, Telangana.

S. Priyanka, Mohammed Raheez, Ale Sairam
Department of ECE
CMRCET, Hyderabad, Telangana.

Abstract -- **The introduction of portable devices raised the need for static random-access memory (SRAM), and SRAM is now widely used in System on Chip and high-performance VLSI circuits. SRAM optimization has been a focus of study due to the fact that memories use 60 to 70% of the chip's space. Adjustment of performance parameters may result in total chip performance optimization. Because of the continual rise in intra-die variability and Vdd scaling, SRAM cell read and write stability are key challenges in nanoscale CMOS technology. SNM fluctuation is also detected when the supply voltage varies.**

Keywords – SRAM, CMOS, Power Dissipation, Read and Write Delay, Leakage Power.

1. INTODUCTION

Due to the huge number of transistors per cell, VLSI systems need a substantial amount of additional capacity for Static Random Access Memory (SRAM). SRAM cells often use small transistors to maximise packing density. Scaling has reduced the size of SRAM cells during the last three decades. When reading and writing data to and from SRAM cells, two design considerations come into play: power dissipation and propagation delay DPD is the power wasted during read and write operations .Mobile devices' battery life may be estimated using this tool.. SRAM speed is determined by the amount of time it takes to read and write data. Nanometre -scale design presents a wide range of design challenges. SRAM cell design has a major issue with stability. MOSFET aspect ratio and operating conditions have an impact on memory stability. Stability of memory refers to its capacity to perform its intended functions. Static Noise Margin measures the reliability of SRAM cells (SNM). When figuring out the SNM, the way an SRAM cell transfers voltage is taken into account. Noise at the lowest voltage level may cause SRAM to change states. In order for the stored value to remain unchanged throughout the read/write cycle, data must be able to be written into SRAM.SRAM's overall power consumption includes both dynamic and static dissipation. As read and write operations, for example, use up the dynamic power of the SRAM, so do standby power consumption. This article's major objective is to create and analyse A stability analysis of a 6T SRAM cell in several CMOS technologies. A PTM model card is utilised in this inquiry to study cell performance in different modes. For a wide range of process variables, it provides model files that are accurate and compatible. It is used for the design and simulations of Cadence Virtuoso Analog Design Environment.

2. ARCHITECTURE AND WORKING OF 6T SRAM CELL

2.1 Architecture

Figure 1 depicts the schematic depiction of the 6T SRAM Cell. Bit storage is the responsibility of P1-N1 and P2-N2 which are cross-coupled CMOS inverters. Reading and writing data to and from the memory is handled by two access transistors, N3 and N4.

To accomplish the read function, two NMOS transistors are coupled in series in this setup. The 6T SRAM cell is seen in Figure 1. The word line is used to activate and deactivate the access transistors. During the write process, the bit line serves as input. Bit lines are used to supply the value that will be written to a memory cell.The bit lines, on the other hand, are used as output during the read process. SRAM memory cells save data until the power is supplied. The word lines are enabled and the bit lines are pre-charged so that you may begin reading. During read mode, the SRAM cell's stored value, which might be 0 or 1, is obtained. Access transistors N3 and N4 are activated when the word line is switched on. 'BL' or 'BLB' voltage decreases are detected by the detecting amplifier. We are able to determine q by using the sensing amplifier. The newly determined value is written into the SRAM cell when the write mode is activeIn order to store new data in the SRAM cell, either a 0 or a 1 must be placed at the 'q' position. When the device is in sleep mode, the word lines are blocked, deactivating access transistors N3 and N4.The SRAM cell's stored value will not change as a consequence of this event.

Figure 1: 6T SRAM cell

2.2 Design Metrics

2.2.1 Power Dissipation: It is essential that portable devices have a long battery life with appropriate performance to be considered portable. In order to have a decent battery, One must first handle the problem of power loss. The sum of static and dynamic power dissipation.During operations of writing and reading, SRAM dissipates power in a dynamic manner, as opposed to the static manner in which power is dissipated while the system is in sleep mode. The total amount of power utilised is the sum of the source's current and voltage. Low

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

power dissipation designs are required for mobile devices. As the technological node grows down, dynamic power dissipation lowers. However, in the deep submicron areas, static power dissipation rises.

2.2.2 Delay: It is defined as the period between when an input is applied and when it returns. Increasing system speed is the major objective of any system design. SRAM's read and write access times are used to gauge its speed.

2.2.3 Power Delay Product: In order to determine the Power Delay Product (PDP), we multiply the average power consumption by the delay. Due to the fact that it quantifies the amount of energy needed during a switching event, it is also known as switching energy (that is, for 0 to 1 or 1 to 0 transition). The Power Delay Product determines performance. The product has an energy-efficient circuit design with a minimum power delay.

3. 6T SRAM CELL DESIGN

The 6T SRAM cell is made up of six MOSFETs, four of which are connected as CMOS inverters, where bits are stored as 1 or 0, while the other two, which operate as pass transistors, control the SRAM cell through the bit line. When the WL (word line) is high, the SRAM cell may be accessed.

3.1 Standby Mode:

The contents of the connected transistors do not change when the system is in sleep mode because N3 and N4 are disabled .This blocks access to the SRAM cell when the system is idle.

3.2 Read Mode:

The technique for reading data from SRAM is shown in the diagram below. The bit lines are linked to the two N3 and N4 pass transistors, which are also connected to each other, are activated while WL is in read mode. Values from nodes A and B have now been shifted across to the bit lines. In the case where node A has been set to 0, The BL supply is drained by the N3 and N1 transistors, and the P2 transistor is responsible for bringing the BL BAR up to VDD. While transistors P1 and N2 are turned off, transistors N1 and P2 function in a state known as linear mode, This is the default mode of operation.

3.3 Write Mode:

The graphic explains the steps that must be taken in order to write to a 6T SRAM. Writing to SRAM grounds the BL BAR or BL. The BL BAR is now dumped to earth. Writing logic 0 links the BL BAR to Vdd and dissipates the BL to ground. WL is turned on whenever there is going to be data entry into the cell. The BL line is activated with 1 logic, which charges node A through the N3 transistor, assuming node A already has a 0 value. P1 is activated as a result of the discharge that occurs at the output of the inverter P2-N2 (node B), which results in N2 coming online. As a consequence, node A is now marked with the value 1.

The schematic of a 6T SRAM Cell is shown below, and we may use it to function in read and write mode. In the schematic design, we employ six transistors, four of which are inverter transistors and two of which are access transistors.

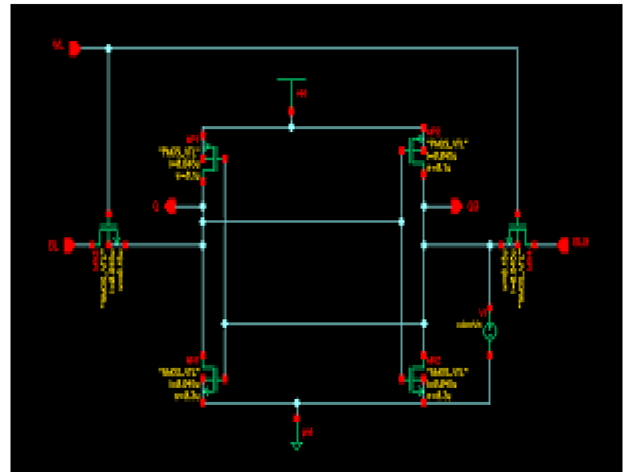

Figure 2: 6T SRAM using CMOS Technology

4. RESULT ANALYSIS

4.1 Read operation:

The word line in SRAM must be high in order for read operations to be executed. In order to perform a read operation, memory must first retain some value. Consider memory with Q=1 and Q=0 as an example. Raise the word line to the highest point to complete the reading. Node voltage Vdd is initially applied to the output lines bit and bit b. Due to the fact that Q and bit are both high, the circuit will not discharge. In the case of Q"=0 and bit as high, there will be a drop in bit b voltage due to the voltage differential between Q" and the node voltage at bit b. There will be a discharge of electrical energy since the circuit will be filled with current. Bit a and Bit b are linked to the detecting amplifier, which functions as a comparator, thus the output is 1 when Bit an is low. As a consequence, the output was 1 when Q=1 was utilised as an input.

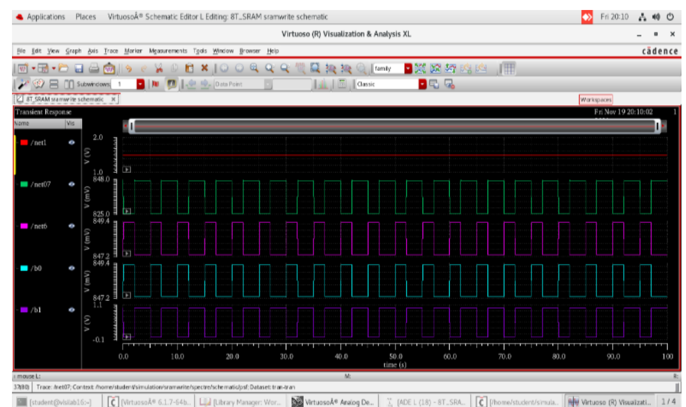

Figure 3: 6T SRAM Read Operation

4.2 Write Operation:

The written value is transferred to the bit lines at the beginning of a write cycle. Set the bit lines to 0 by configuring the BL bar to 1 and the BL bar to 0. To get a 1, the bit line values must be inverted. Following the input of the value to be stored, WL is asserted. Because bit line input-drivers are supposed to be far more powerful than cell transistors, they may easily overpower the cross-coupled inverters' prior state. The write operation is much simpler than the read operation in the proposed approach. The writing procedure starts by rising to VDD while the WL is being pulled down. The second BL is

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

being held at VDD as the first one is being dragged to the ground. When the node is turned on, N1 and N2 go to VDD. When node C is linked to VDD, N1 and N2 are also charged. Memory data is replicated onto the N1 and N2 devices in the same manner that a regular 6T SRAM would.

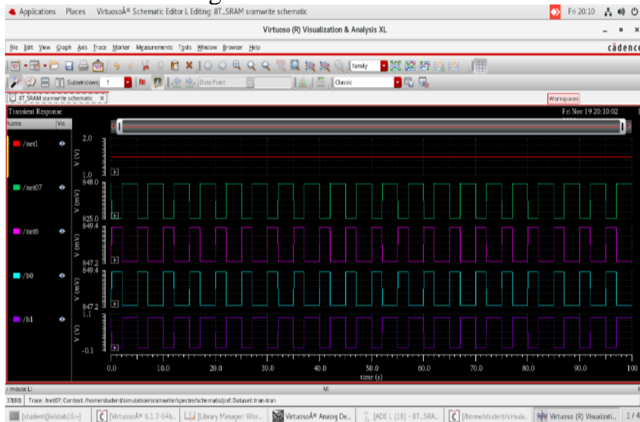

Figure 4: 6T SRAM cell Write Operation

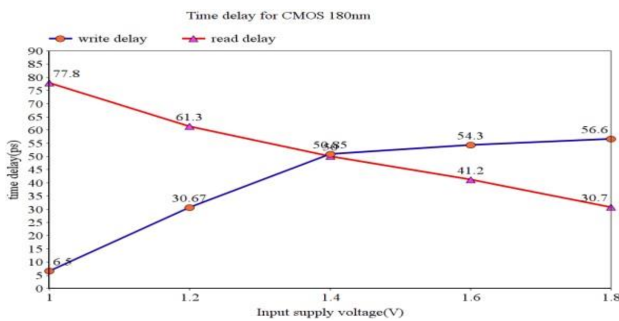

Figure 5: Time delay for CMOS 180nm

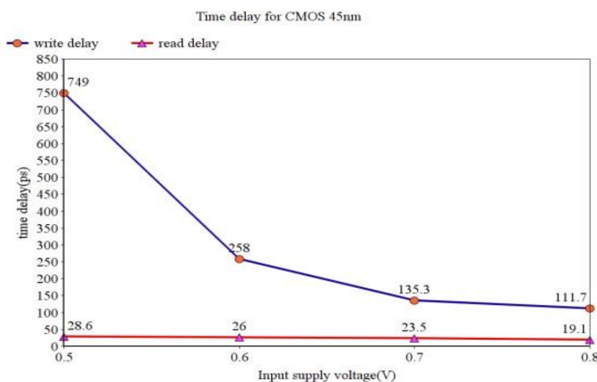

Figure 6: Time delay for CMOS 45nm

Technology	180nm	90nm	45nm
Power (Watts)	519.7n	59.58n	30.68n
SNM for read operation	0.35v	0.17v	0.14v
SNM for write operation	0.31v	0.07v	0.19v

Table: Performance Comparison between 6T SRAM cells with different CMOS Technologies

5. CONCLUSION

In this paper the simulation is done by using Cadence Virtuoso tool. The simulation is done for 6T SRAM cell in 180nm, 90nm and 45nm technology node. The design architecture shows speed improvements along with scaling of technology and delay time also decrease. Power dissipation also decreases with scaling of technology. Simulation and result analysis are done in terms of power dissipation, delay and SNM.

6. REFERENCES

[1] CA Ajoy, A Kumar, CA Anjo, V Raja. Design and analysis of low power SRAM using cadence tool in 180nm technology. IJCST, 5(1), 2014.

[2] X Wang, Y Zhang, C Lu, Z Mao. Power efficient SRAM design with integrated bit line charge pump. AEU International journal of electronics and communications, 70(10), 2016.

[3] VS Baghel, S Akashe. Low power Memristor Based 7T SRAM Using MTCMOS Technique. Fifth International Conference on Advanced Computing & Communication Technologies, 2015.

[4] A Agal, Pardeep, B Krishan. 6T SRAM Cell: Design and Analysis. Journal of Engineering Research and Applications, 4(3), 2014.

[5] S Joshi, S Hadia. Design and Analysis for Low power CMOS SRAM cell in 90 nm technology using cadence tool. International Journal of Advanced Research in Computer and Communication Engineering, 2(4), 2013.

[6] YP Tsividis, Operation and modelling of the MOS transistor, Mc graw Hill Series in Electrical Engineering, Vlsi, Electronics, and Electronic Circuits, 1998.

[7] Ajoy C A, Arun kumar, Anjo C A and Vignesh Raja, Design and analysis of low power SRAM using cadence tool in 180nm technology, IJCST Vol., Jan-March 2014.

[8] Debasish Nayak, Debiprasad Priyabrata Acharya, and Kamalakanta Mahapatra, An improved energy SRAM cell for access over a wide frequency range, Solid-state electronics, Elsevier,14-22, 2016.

[9] B. Kaleeswari, Dr. S. KajaMohideen ,"Analysis of Leakage current in 8T SRAM for low power application "Journal of social, techno-logical and environmental sciences, Sep 2017,Vol No 6 pp601-610.

[10] B. Kaleeswari, Dr. S. KajaMohideen ,"Design, Implementation and Analysis of 8T SRAM Cell in Memory Array"," International Journal of Engineering & Technology,2018,pp-101-105.

[11] Eitan N. Shauly," CMOS Leakage and Power Reduction in Transis-tors and Circuits: Process and Layout Considerations in Journal of low power Electronics(2012).

[12] VaishnaviAgey, Different Types of SRAM chip s for power reduction ,IEEE Conference in 2017.

[13] Tae Woo Oh, Han wool Jeong, Kyoman Kang, Juhyun Park, Younghwi Yang, and Seong-Ook Jung, Power-Gated9T SRAM Cell for Low-Energy Operation" IEEE Transactions On Very Large Scale Integration (Vlsi) Systems(2016).

[14] Neeta Sharma,"Comparative Analysis Of Power Reduction In SRAM 6t And 4t, in International Journal of AdvanceResearch In Science And Engineering, Vol. No.4, Special Issue (01) , (2015) pp-1325-1334.

[15] Atluri .Jhansi rani, K .Harikishore, Fazal Noor Basha,,V.G. SanthiSwaroop, L. VeeraRaju , " Designing and Analysisof 8 Bit SRAM Cell with Low Subthreshold Leakage Power " in International Journal of Modern EngineeringResearch, Vol.2, Issue.3 (2012).

[16] N. Verma and A. Chandrakasan,. "A 256 kb 65 nm 8T sub-Vt SRAM employing sense-amplifier redundancy,"IEEE J. Solid-State Circuits, Vol. 43, no. 1, (2008) pp. 141–149.

[17] Geetika Srivastava, R.K. Chauhan,, 2012"Effect of Technology Scale-Down on Power Reduction Strategies. Int'lConf. on Recent Advances in Information Technology.

[18] B. Zhai, D. Blaauw, and D. Sylvester,"A variation-tolerant sub-200mV 6-T sub threshold SRAM," IEEE J. Solid-State Circuits, vol. 43, no. 10,pp. (2008) 2338–2348 Wutan Huatan Jisuan Jishu Volume XVI, Issue V, May/2020 ISSN:1001-1749 Page No:35

(This work is licensed under a Creative Commons Attribution 4.0 International License.)