Design of 33 Level Asymmetrical Multilevel Inverter with Reduced Value of THD

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***Abstract* - This paper presents a simplified and reduced cascaded H Bridge asymmetrical multilevel inverter in order to generate any number of output voltage levels with reduced number of switching components. In this paper, a 33 level asymmetrical MLI is introduced with different switching angle calculation technique, particularly equal phase method and half height methods are analyzed presented and compared. The main benefits of the proposed 33 level inverter are less number of switching components, lower loss, reduced size and with reduced value of THD using half height switching angle calculation technique. Simulation works are carried out through MATLAB software to demonstrate the performance of the presented 33 level asymmetrical MLI with equal angle and half height switching angle calculation techniques.**

Keywords - Cascaded H Bridge (CHB); Multi Level Inverter (MLI); Equal Phase (EP) Method; Half Height (HH) Method; Total Harmonic Distortion (THD)

I. INTRODUCTION

The word “inverter” comes under the class of power electronic conversion devices which operates under the DC input and converts it into an AC output. The multilevel inverters (MLI) are been the alternative for medium and high power applications. Due to the huge demand and wide utilization of multilevel inverters in industrial applications, renewable energy systems, machine drive systems, HVDC and FACTS drives etc, the power electronic researchers have made efforts in developing the multilevel inverters by altering their structures and topology, in terms of reducing their number of components and decreasing the value of THD, resulting in the decrease in size and reduction in losses.

There are mainly three basic topologies that comes under multilevel inverters listed as

1. Neutral Point Clamped (NPC) MLI
2. Flying Capacitor (FC) MLI
3. Cascaded H Bridge (CHB) MLI

3a. Symmetric source configuration CHB MLI

3b. Asymmetric source configuration CHB MLI

Due to the requirement of large number of clamping diodes in Neutral Point Clamped (NPC) MLI topology and the requirement of huge number of capacitors in Flying Capacitor (FC) MLI and unbalanced DC links limits their application for higher number of voltage levels. Voltage balancing has become the main draw back for both Neutral Point Clamped (NPC) and Flying Capacitor (FC) MLI topologies.

The third basic topology is the cascaded H-bridge (CHB) multilevel inverter which is further separated as asymmetric source configuration CHB MLI (employing same magnitude of DC sources) and asymmetric source configuration (employing different magnitude of DC sources). The requirement of same magnitude of DC voltage sources increases with the increase in the level of output voltage, which was observed to be the major disadvantage of the symmetric source configuration hence the reduction in number of sources and switching components is the main target in the design of asymmetric source configuration CHB MLI employing different magnitude of DC sources.

The proposed 33 level asymmetrical CHB multilevel inverter contains eight switches, four diodes, and five different magnitude of DC voltage sources to generate 33 level output voltage resulting in reduced size and lower loss

For the better performance of the multilevel inverters several switching techniques are used. For the proposed 33 level inverter topology, fundamental switching strategy is used. The switching angles are calculated using equal phase (EP) method and Half Height (HH) method, those two methods are compared for the same 33 level inverter and observed Half Height switching angle calculation technique gives less THD and better performance

II. PROPOSED 33 LEVEL INVERTER TOPOLOGY

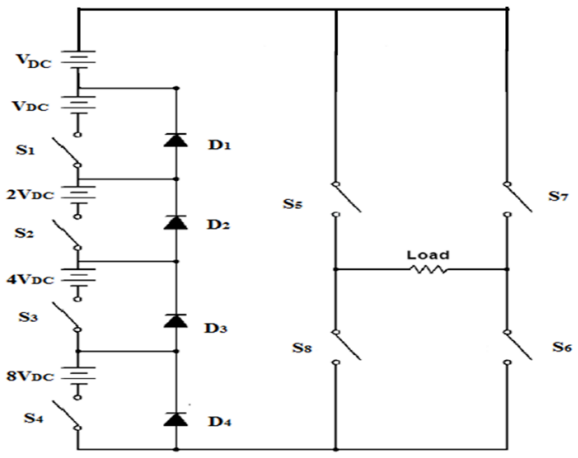


Fig.1. Single phase 33-level asymmetrical inverter topology

The schematic diagram of the proposed 33 level asymmetrical multilevel inverter is as shown in the Fig 1. The proposed circuit consists of eight switches, four diodes and five different magnitude of the DC voltage sources to generate 33 level output voltage waveform. The switching components used in the circuit can be either IGBT or MOSFET with antiparallel diodes

The switches S1, S2, S3 and S4 are switched ON and OFF to generate various output voltage levels hence this part of the circuit is known as level generation switching part.

The switches S5, S6, S7 and S8 forms a H-Bridge circuit and each pair of the switches conducts for every half cycle in order to reverse the polarity of the output voltage waveform. Hence this H-Bridge part of the circuit is known as polarity generation switching part.

TABLE I. SWITCHING SEQUENCE OF THE PROPOSED 33 LEVEL ASYMMETRICAL INVERTER TOPOLOGY

Switching State	Conducting switches								Conducting Diodes				0utput Voltage (V_0)
	S1	S2	S3	S4	S5	S6	S7	S8	D1	D2	D3	D4	
1	1	1	1	1	1	1	0	0	0	0	0	0	16 Vdc
2	0	1	1	1	1	1	0	0	1	0	0	0	15 Vdc
3	1	0	1	1	1	1	0	0	0	1	0	0	14 Vdc
4	0	0	1	1	1	1	0	0	1	1	0	0	13 Vdc
5	1	1	0	1	1	1	0	0	0	0	1	0	12 Vdc
6	0	1	0	1	1	1	0	0	1	0	1	0	11 Vdc
7	1	0	0	1	1	1	0	0	0	1	1	0	10 Vdc
8	0	0	0	1	1	1	0	0	1	1	1	0	9 Vdc
9	1	1	1	0	1	1	0	0	0	0	0	1	8 Vdc
10	0	1	1	0	1	1	0	0	1	0	0	1	7 Vdc
11	1	0	1	0	1	1	0	0	0	1	0	1	6 Vdc
12	0	0	1	0	1	1	0	0	1	1	0	1	5 Vdc
13	1	1	0	0	1	1	0	0	0	0	1	1	4 Vdc
14	0	1	0	0	1	1	0	0	1	0	1	1	3 Vdc
15	1	0	0	0	1	1	0	0	0	1	1	1	2 Vdc
16	0	0	0	0	1	1	0	0	1	1	1	1	Vdc
17	0	0	0	0	0	0	0	0	0	0	0	0	0
18	0	0	0	0	0	0	1	1	1	1	1	1	-1 Vdc
19	1	0	0	0	0	0	1	1	0	1	1	1	-2 Vdc
20	0	1	0	0	0	0	1	1	1	0	1	1	-3 Vdc
21	1	1	0	0	0	0	1	1	0	0	1	1	-4 Vdc
22	0	0	1	0	0	0	1	1	1	1	0	1	-5 Vdc
23	1	0	1	0	0	0	1	1	0	1	0	1	-6 Vdc
24	0	1	1	0	0	0	1	1	1	0	0	1	-7 Vdc
25	1	1	1	0	0	0	1	1	0	0	0	1	-8 Vdc
26	0	0	0	1	0	0	1	1	1	1	1	0	-9 Vdc
27	1	0	0	1	0	0	1	1	0	1	1	0	-10 Vdc
28	0	1	0	1	0	0	1	1	1	0	1	0	-11 Vdc
29	1	1	0	1	0	0	1	1	0	0	1	0	-12 Vdc
30	0	0	1	1	0	0	1	1	1	1	0	0	-13 Vdc
31	1	0	1	1	0	0	1	1	0	1	0	0	-14 Vdc
32	0	1	1	1	0	0	1	1	1	0	0	0	-15 Vdc
33	1	1	1	1	0	0	1	1	0	0	0	0	-16 Vdc

There are 33 different operating modes to generate 33 different output voltage levels for the proposed 33 level asymmetrical inverter topology

The switching sequence of the conducting switches, conducting diodes for different voltage levels are shown in the table I, with 16 positive levels, 16 negative levels and 1 zero level

State condition '1'represents the conduction state and the state condition'0' represents the non-conduction state of the switches and diodes

III. COMPARITIVE STUDY OF THE PROPOSED MULTILEVEL INVERTER TOPOLOGY WITH OTHER RECOMMENDED TOPOLOGIES

Table II presents the comparative analysis between the proposed 33 level asymmetrical inverter topology with the conventional inverter topologies which is indicated in terms of number of switches, DC sources, power diodes and capacitors.

TABLE II. COMPARISON OF VARIOUS MULTILEVEL INVERTER TOPOLOGIES

Inverter topologies	NPC	FC	CHB	[4]	[5]	[6]	Proposed topology
Number of levels	33	33	33	33	33	33	33
Number of sources	1	1	16	16	16	8	5
Number of switches	64	64	64	20	21	18	8
Number of diodes	1056	-	-	16	-	18	4
Number of capacitors	30	330	-	16	-	-	-

From the table II and Fig 1, it can be proved that to generate the same 33 level output voltage waveform the proposed structure requires only eight unidirectional switches, five different magnitude of DC sources and four unidirectional diodes which gives the better result with less number of components, reduced size and also reasonable

IV. SWITCHING ANGLE CALCULATION TECHNIQUE

There are several techniques of switching modulation for estimating the switching angles to generate N level of the output voltage waveform

In this paper, the switching angles are calculated using Equal Phase (EP) method and Half Height (HH) method based on the fundamental switching strategy.

A. *Equal Phase (EP) method*

In this technique the switching angles are distributed averagely over the full complete cycle ranging from 0 – 360 degrees. The equation to calculate the switching angles by Equal Phase (EP) method is given a

$$a_k = \mathrm{k} * \frac{180}{N}$$

Where k = 1, 2, 3, 4 ……2N and N = number of output voltage levels

B. *Half Height (HH) method*

- In this technique the total period (0 – 360 degrees) of the output waveform are divided into four quadrants i.e. the period from 0 to 90 degree is referred as the main switching angle which is calculated as

$$a_k = \sin^{-1}\frac{(2k-1)}{(N-1)}$$

Where k = 1, 2, 3, 4 ……$\frac{N-1}{2}$ and N = number of output voltage levels

- The period from 90 to 180 degree is referred as the second quadrant switching angle which is calculated as

$$a_{\frac{N+1}{2}} = \pi - a_{\frac{N-1}{2}}\ ,\ \pi - a_{\frac{N-2}{2}},\ \ldots\ldots\ldots,\ \pi - a_1$$

- The period from 180 to 270 degree is referred as the third quadrant switching angle which is calculated as

$$a_N = \pi + a_1, \pi + a_2, \ldots\ldots\ldots, \pi + a_{\frac{N-1}{2}}$$

- The period from 270 to 360 degree is referred as the final quadrant switching angle which is calculated as

$$a_{\frac{3N-1}{2}} = 2\pi - a_{\frac{N-1}{2}},\ 2\pi - a_{\frac{N-2}{2}},\ldots\ldots\ldots,\ 2\pi - a_1$$

From the above two methods of switching angle calculation techniques it is observed that the Half Height method gives better performance and reduced value of THD

The switching pulses given to each switches through equal angle method is shown in Fig 2.

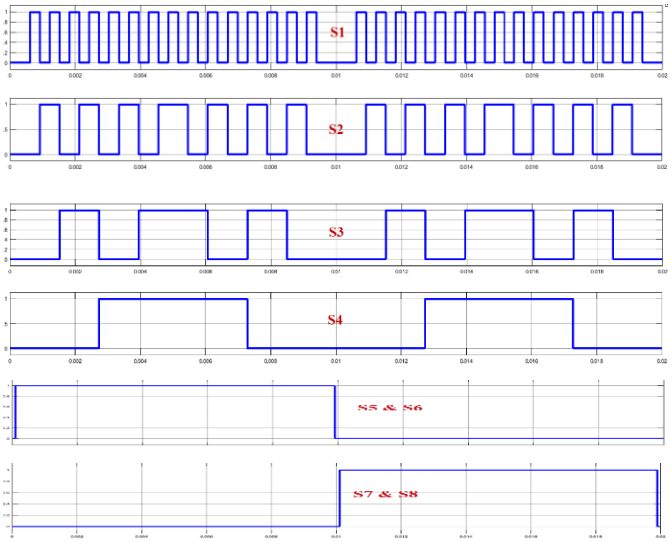


Fig.2. One complete cycle switching pulse pattern using Equal Phase method

The switching pulses given to each switches through Half Height (HH) method is shown in Fig 3.

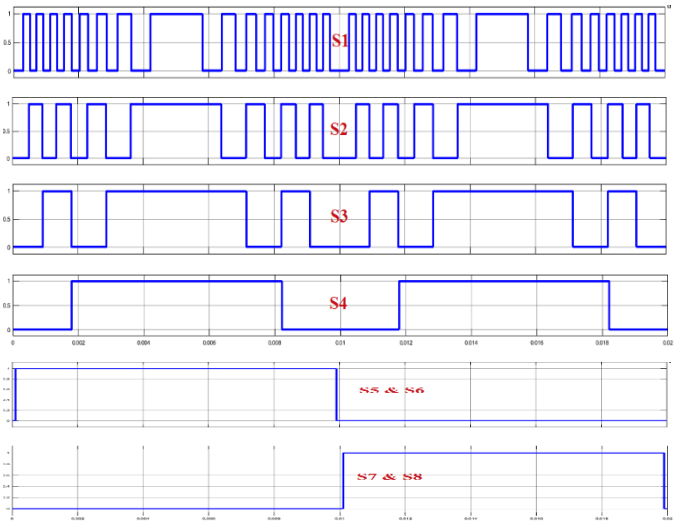


Fig.3. One complete cycle switching pulse pattern using Half Height method

V. SIMULATION RESULTS

In order to prove the ability and the performance of the proposed 33 level asymmetrical multilevel inverter to generate 33 output voltage levels, the presented circuit with Equal Phase and Half Height switching angle modulation technique is simulated through MATLAB Simulink software.

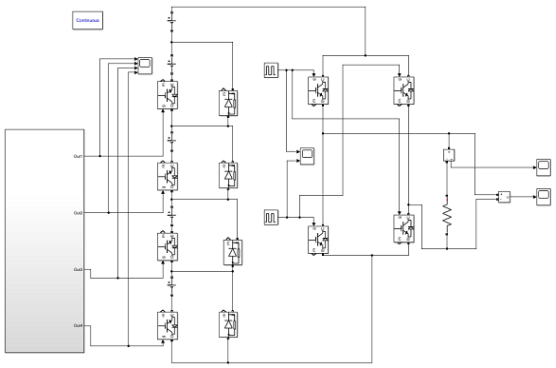
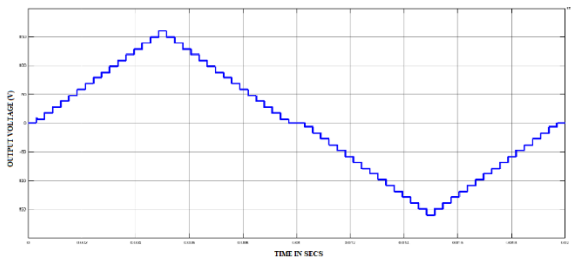


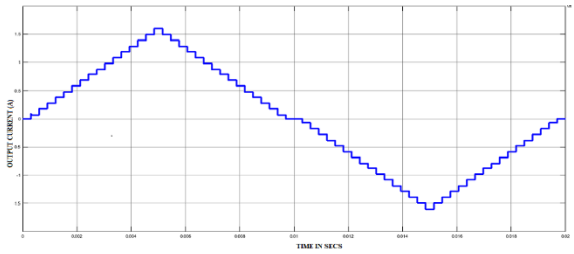
Fig.4. 33 Level Asymmetrical CHB MLI simulation circuit

The magnitude of the DC links used in the simulation circuit are 10Vdc, 20Vdc, 40Vdc & 80Vdc, for which the inverter generates the output voltage with maximum positive amplitude of +160V and with maximum negative amplitude of -160V. The each step of the output voltage is 10 volts, the switches used are IGBT with operate at the fundamental switching frequency of 50 Hz.

The 33 level output voltage waveform and output current obtained for Equal Phase (EP) method is as shown in the Fig 5



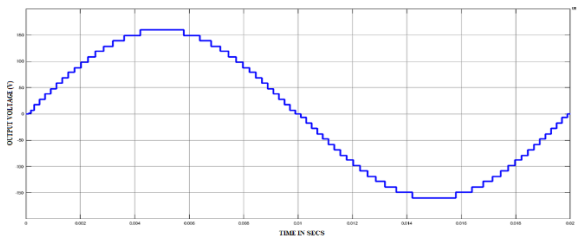
(a)



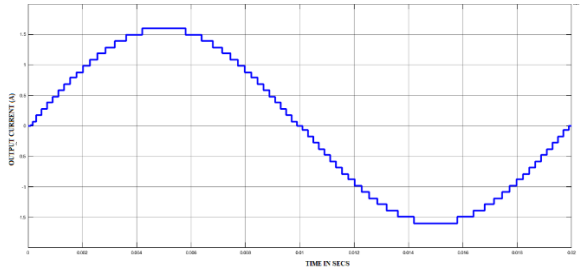
(b)

Fig.5. (a) output voltage waveform (b) output current waveform for Equal Phase method

The 33 level output voltage waveform and output current obtained for Half Height (HH) method is as shown in the Fig 6



(a)

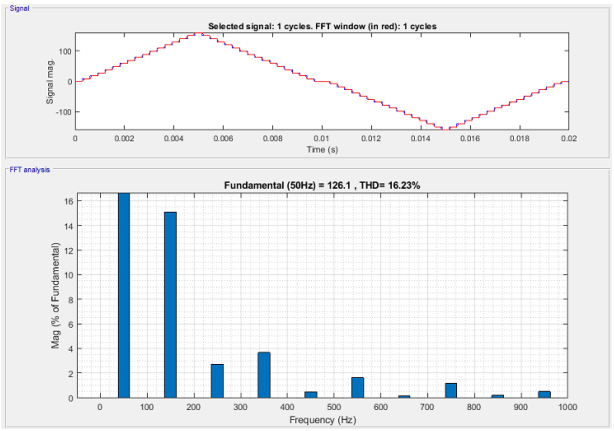


(b)

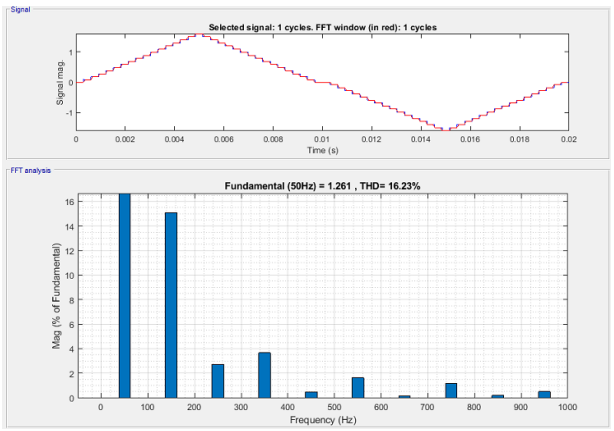
Fig.6. (a) output voltage waveform (b) output current waveform for Half Height method

With the aid of Fast Fourier Transform function (FFT) in MATLAB Simulink the Total Harmonic Distortion (THD) for the output voltage and output current waveform are computed.

Figure 7, shows the THD analysis of the output voltage and output current for the Equal Phase method.



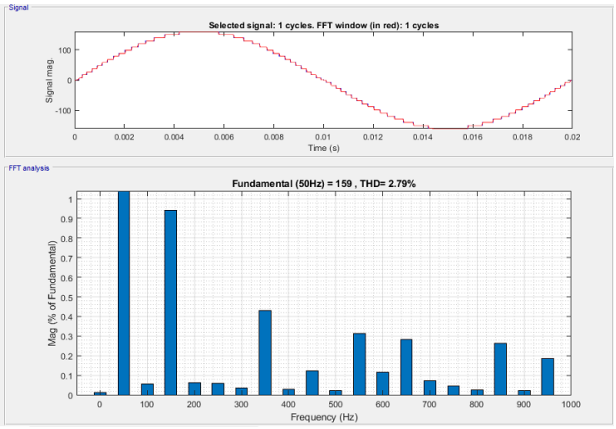
(a)



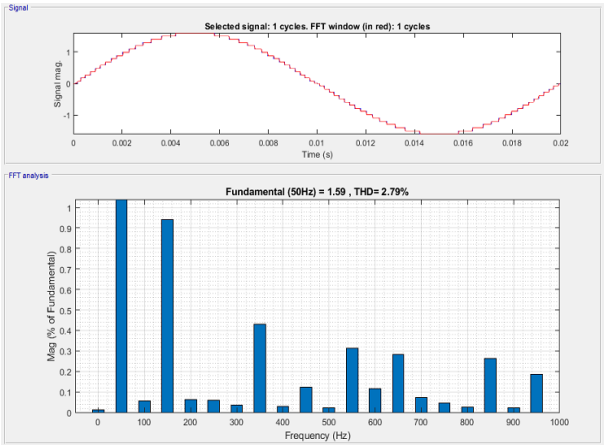
(b)

Fig 7. (a) output voltage harmonic spectrum (b) output current harmonic spectrum for Equal Phase method

Figure 8, illustrates the THD analysis of the output voltage and output current for the Half Height method.



(a)



(b)

Fig 8. (a) output voltage harmonic spectrum (b) output current harmonic spectrum for Half Height method

The Equal Phase switching angle calculation technique and the Half Height switching angle calculation techniques are distinguished in table III, it can be summarized that the Half Height method offers very less value of THD when compared with the Equal Phase method

TABLE III. COMPARISON OF THD BASED ON SWITCHING MODULATION TECHNIQUE

Switching technique	Load voltage THD	Load current THD
Equal Phase method	16.23	16.23
Half Height method	2.79	2.79

ACKNOWLEDGMENT

The simplified and reduced cascaded H-Bridge asymmetrical multilevel inverter is presented which generates 33 levels of output voltage offering minimum number of switching components and DC sources, hence the proposed inverter is resulted in diminished size and low installation cost. From the simulation results the THD offered by the half height method is 2.79% which is very low compared to the Equal Phase method which offered the THD of 16.23%. Therefore the proposed 33 level asymmetrical inverter topology with Half Height switching modulation technique is reasonable for medium and high voltage application

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