Design of 2-D DWT VLSI Architecture for Image Processing

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***Abstract*— The role of the compression is to reduce bandwidth requirements for transmission and memory requirements. For the storage of all forms of data as it would not be practical to display images, audio, video alone on websites without compression. The use of wavelet transform is now well established due to its multi resolution and scaling property. The system is fully compatible with JPEG 2000 standard. It provides in-place computation of the wavelet coefficient also requires fever operations. So architecture is proposed based on Discrete Wavelet Transform (DWT) of 5/3 and 9/7 filter. The proposed architecture includes transforms unit, a RAM-memory unit and bus interfaces. The lifting scheme represents the fastest implementation of the DWT. A VHDL model was designed and synthesized using the memory efficient architecture. In terms of memory access, hardware regularity and simplicity and throughput, the proposed VLSI architecture is more efficient than the previously proposed architectures**

Keywords*— *VlSI Architecture, DWT, Flexible, Lifting Scheme, 5/3 filter, 9/7 filter

I. INTRODUCTION

Image compression requires higher performance due to the increasing use of multimedia technologies. Inorder to address needs and requirements of multimedia and internet applications .Recently many efficient image compression techniques, with considerably different features, have been developed. Traditionally image compression adopts discrete cosine transform (DCT) which possess the characteristics of simpleness and practicality. Discrete cosine transform has been applied successfully in the standard of JPEG, MPEG etc. However, the compression method DCT has several shortcomings that become increasing apparently. One of these shortcomings is too bad subjective quality when the images are restored by this method at the high compression ratios. In recent years, many researchers have been made on wavelets. An excellent study of wavelets has brought to the fields as diverse as biomedical applications, wireless communications, computer graphics or turbulence. Image compression is one of the most visible applications of wavelets. DWT has become a standard tool in image compression applications because of their data reduction capability[1]. In a wavelet compression system, the entire image system has been transformed and compressed as a single data object rather than block by block as in a DCT-based compression system. DCT allows a uniform distribution of compression error across the entire image.

DWT has traditionally been implemented by convolution or the finite impulse response (FIR) filter bank structures. Such type of implementations require both large number of arithmetic computations and a large storage, features which are not desirable for either high speed or low power image/video processing applications. Therefore a new approach is called the lifting scheme based wavelet transform or simply lifting has been proposed by Swelden based on a spatial construction of the wavelet [2]. The architecture lifting-based 2D-DWT developed has regular data flow and low control complexity. Many architectures of DWT are lossy and lossless transform. In the proposed architecture can be modeled and reconfigured for 5/3 and 9/7 wavelet transforms which reduces significantly the required numbers of the multipliers, adders and registers, as well as the amount of accessing external memory, and leads to decrease efficiently the hardware cost and power consumption of design. In this paper architecture is based on memory efficient bi-orthogonal filter it implements 2D-DWT; therefore we get a design of DWT reconfigurable with the multi-levels resolution for the up needs. The architecture of DWT decomposition using lifting scheme structure with distributed control to compute all the resolution levels of DWT. This architecture is reconfigurable and scalable in its totality, since we change the levels and types of transforms (2D-DWT) without changing the design of the control units. The remaining paper is organized in the following manner: the section II provides a brief overview of the lifting scheme DWT algorithm. In section III, the proposed architecture and its processing techniques. In section IV gives the synthetic results of the architecture with compressed image. Comparisons results with 9/7 filter architecture in section V. Finality, conclusions are discussed in section VI.

II. THE LIFTING SCHEME

The Lifting scheme (LS) is a method to simplify performing the wavelet transform in an efficient way. The (LS) has more advantages when compared with classical filter banks method, such as the simpler and fewer arithmetic computations required. In addition, the (LS) is more appropriate for high speed and low power applications such as the image/video

processing applications. The main disadvantages of lifting scheme that the multiplier and adder delays are longer than convolution ones which has longer critical paths.

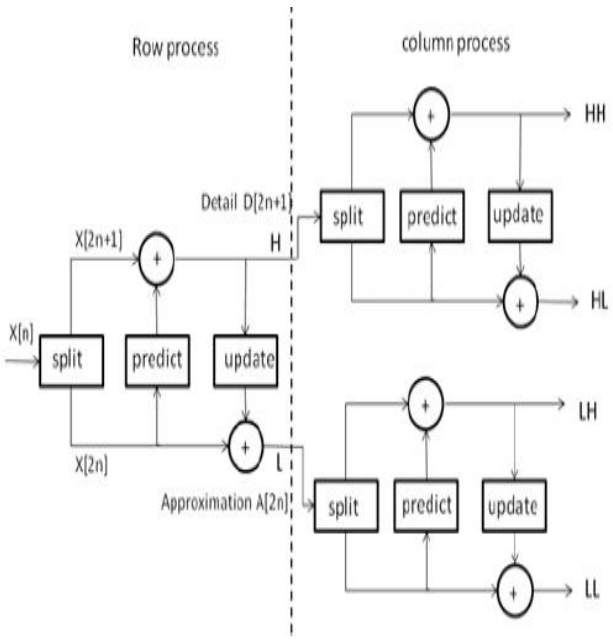


Fig 1: Block diagram of lifting scheme 2-D DWT

The lifting scheme (LS) can be performed by three stages: the split stage, the predict stage, and the update stage[1]. In the split stage the input signal or image is separated into even and odd indexed samples. The predict stage computes the high pass filter coefficients representing the details sub band coefficients. The update stage gives low pass filter coefficients which stand for the approximation subband of the DWT process. For (5/3) wavelet filter the predict and update stages are represented in following equations [4]:

$$Y[2n+1] = X[2n+1] - 0.5(X[2n] + X[2n+2]) \quad (1)$$

$$Z[2n] = X[2n] + 0.25(Y[2n-1] + Y[2n+1]) \quad (2)$$

Where: X[n]: is the input signal. Y[2n+1]: the details coefficients. Z[2n]: the approximations coefficients. From various lifting scheme wavelet transform equations, it is found that hardware design requires only adders and shifters instead of multipliers. In Figure 1 shows the lifting scheme 2-D DWT block diagram.

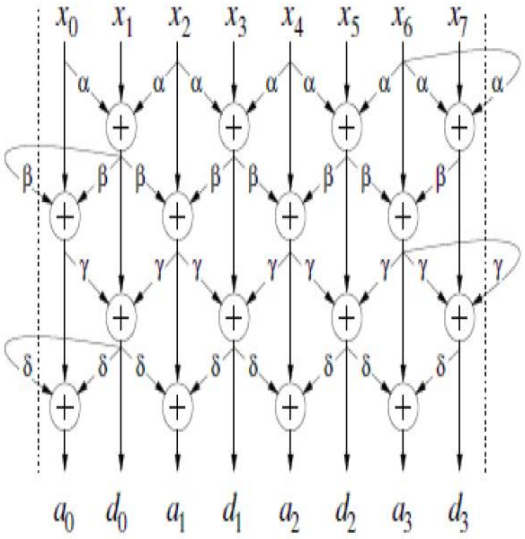


Fig 2: Lifting Version of 9/7 wavelet filters

The lifting-based DWT implementation of 9/7 wavelet filtering as described in is given below. Applying the following steps to the entire input performs the transformation. The input is extended before and after the first and last coefficient, i0 is the index of the first coefficient of the input and i1 is the index of the coefficient immediately following the last coefficient.

Forward transformation

$$Y_{2n+1} = X_{2n+1} + \alpha \times (X_{2n} + X_{2n+2})$$

$$Y_{2n} = X_{2n} + \beta \times (Y_{2n-1} + Y_{2n+1})$$

$$Y_{2n+1} = Y_{2n+1} + \gamma \times (Y_{2n} + Y_{2n+2})$$

$$Y_{2n} = Y_{2n} + \delta \times (Y_{2n-1} + Y_{2n+1})$$

III. PROPOSED ARCHITECTURE

Foe efficient image compression an memory efficient VLSI based architecture be proposed. In this a Bus Interface Unit has been integrated in order to achieve communication efficiently with the external environment. The Control Unit is designed to control the data flow in the design, as well as the data transfer between the bus interface Unit, the Computation Processing Unit and the RAM Unit. A finite state machine is used for this purpose. During initialization phase, the user with the appropriate write commands selects the decomposition DWT type 2D-DWT and with multi-levels decompositions.

The Control Unit coordinates all system operations and processes. After the initialization phase, the control unit is totally responsible for the system operation. The control unit manages the operation of 2D-DWT even-odd filter (Fig.3). It controls the data input, the synchronization of the operations, and the data output. The blocks processing band H and band L are needed in the case of 2D-DWT and multi levels decompositions. These blocks used the arithmetic logic operation of M details and approximation coefficients respectively.

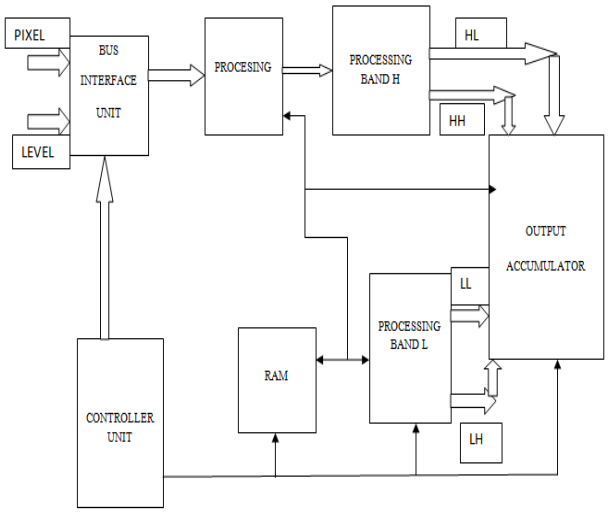


Fig 3: VLSI based 2-D dwt architecture

The RAM block is used for storage of the L and H coefficients for the next transformations types (2D-DWT or multi levels decomposition). The output accumulator is the final block in the architecture. This produces output data by storing the results of different transformations; it is generated under the control of a synchronous available signal. The decomposition scheme is level by level and described as follows:
The 2D-DWT, in first-level decomposition, the bus interface unit selects data (pixels) form input image. The wavelet transform module decomposes to the four sub-bands LL1, LH1, HL1 and HH1, and saves LL1 to the RAM unit. After finishing the first level decomposition, the controller selects data from RAM unit. The LL1 band is then sent to the transform module to perform the second level decomposition. The wavelet transform module decomposes the LL1 band to the four sub-bands LL2, LH2, HL2 and HH2, and saves LL2 band to the RAM module for next level decomposition. This process repeats until the desired N level (last level) decomposition is finished. The 2D-DWT, in first-level decomposition entire image decomposes to LL,LH,HL and HH bands .The second-level decomposition the transformed LL module decomposes to LL1,LH1,HL1 and HH1.

IV. EXPERIMENTS RESULTS

The proposed architecture designed with VHDL is then synthesized, placed, and routed by using Xilinx ISE 12.3 software. The grayscale Lena picture with size (64*64) is stored as an original image in the memory. After that, perform filtering action using 5/3 and 9/7 wavelet filters. Firstly converted the grey scale image to pixels and loaded into memory by VHDL coding and perform corresponding DWT operation. The resulting pixels saved back to the memory location. Then, be converted the obtained pixels back to compressed image.

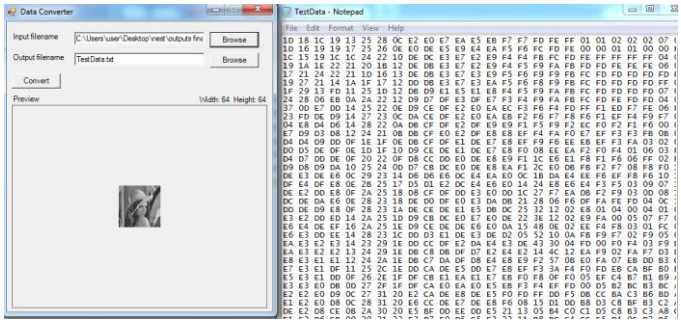


Fig 4: Original Lena image (64*64) and its pixel values

The 2D-DWT is applied on grayscale image which is shown in figure 6. It transforms an image into sub-bands such that the wavelet coefficients in the lower level sub-bands typically contain more energy than those in higher level sub-bands. The first stage of the DWT divides an image into four sub-bands by applying low-pass and high pass filters. The first level of decomposition is consists of two steps.

In the first step, using a vertical analysis filter bank each row of an image is transformed. In the second step of the first level of decomposition, each column of the transformed image is again transformed using same filter bank horizontally. Thus first level of decomposition produces four filtered and sub-sampled images. The result of the first level of decomposition has been shown in figure 4.

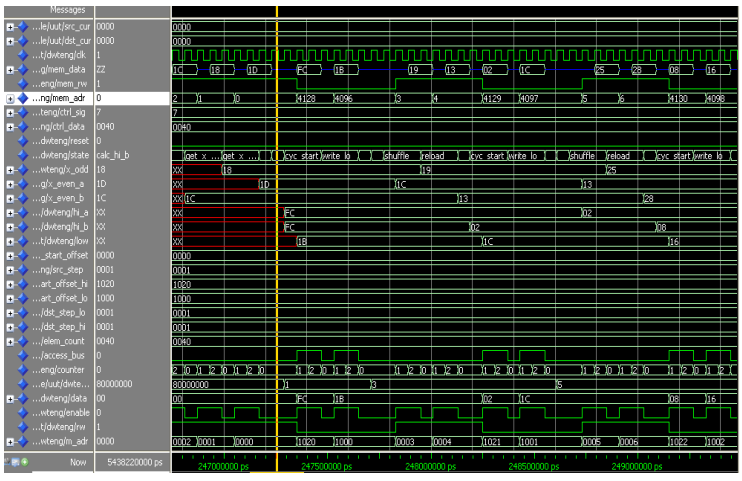


Fig 5: Output of the first level decomposition of Lena image using 5/3 wavelet filters.

For the second level of decomposition, DWT further divides the lowest sub-band pixel values using the same vertical and

horizontal filtering method as above. The lowest sub-band has been decomposed into further four sub-bands. The result of the second level of decomposition has been shown in figure 6. For this DWT block, the clock and reset were the significant inputs.

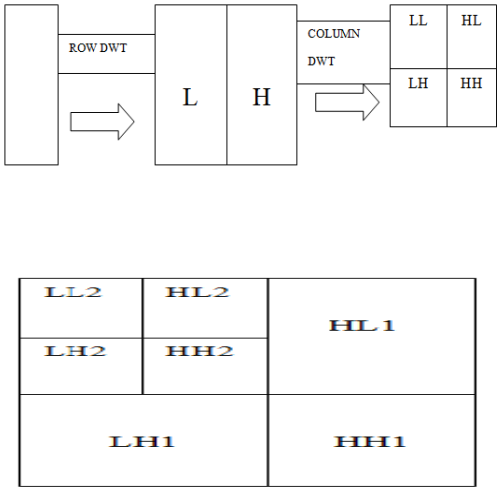


Fig 6: First level and second level decomposition

The pixel values of the image, that is, the input data will be given to dwt block and hence these values will be split in to even and odd pixel values. In the design, this even and odd were taken as a array which will store its pixel values in it and once all the input pixel values over, then load will be made high which represents that the system is ready for the further process. Once the input is send, the data is divided into even data and odd data. The even data and odd data pixels values are stored in the temporary memory registers. When the reset is high the temporary register value consists of zero whenever the reset is low the input data split into the even data and odd data. The 2-D discrete wavelet transform is that the low pass and the high pass again divided into LL, LH and HH, HL.

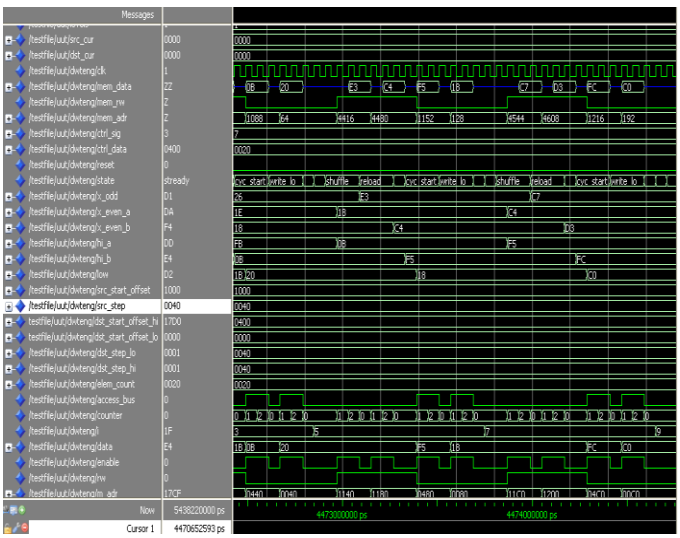


Fig 7: Output of the second level decomposition of Lena image using 5/3 wavelet filters.

The result of the 9/7 wavelet filter decomposition has been shown in figure 8.

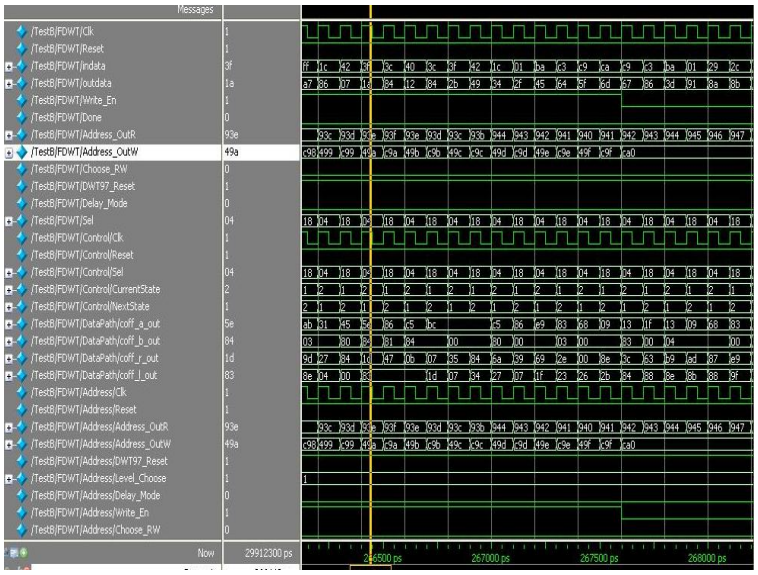


Fig 8: Output of the first level decomposition of Lena image using 9/7 wavelet filters

V.COMPARISON RESULT

Table I: Power comparison

Type of wavelet filter	Power consumption
5/3 wavelet filter	25mW
9/7 wavelet filter	8663 mW

By comparing the both 5/3 and 9/7 wavelet filters the power utilization is less for 5/3 wavelets. The hardware complexity is high for 9/7 wavelet architecture because of the large number of discrete wavelet coefficients. Table 1 shows power comparison of both filter decomposition.

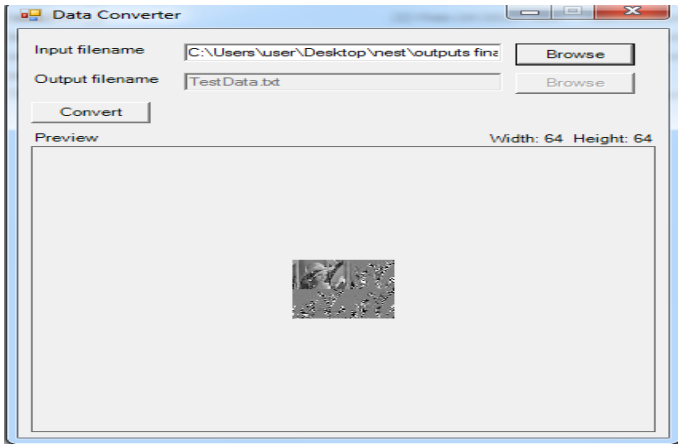


Fig 9: Compressed output for first level decomposition

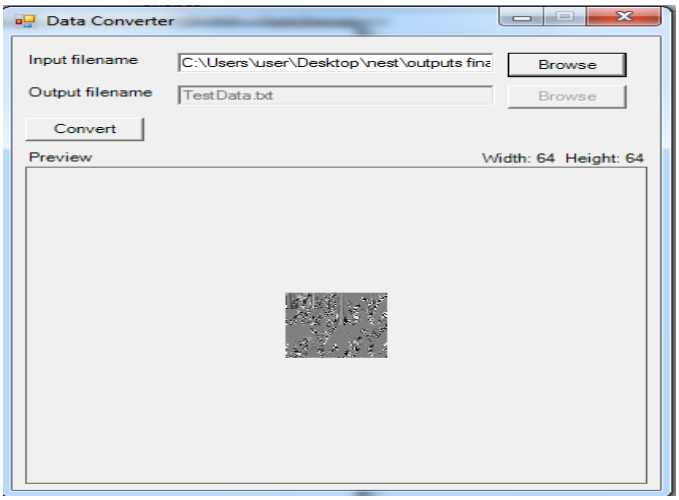


Fig 10: Compressed output for second level decomposition

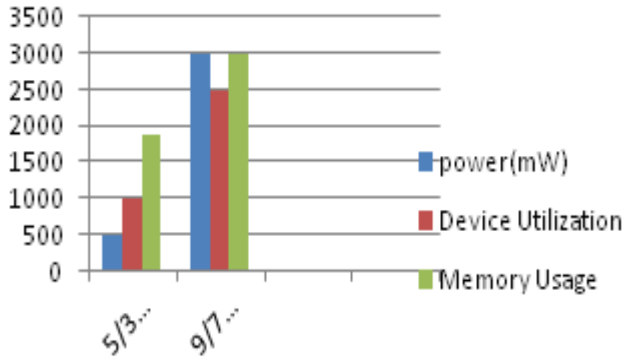
Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	177	3,840	4%	
Number of 4 input LUTs	1,033	3,840	26%	
Logic Distribution				
Number of occupied Slices	599	1,920	31%	
Number of Slices containing only related logic	599	599	100%	
Number of Slices containing unrelated logic	0	599	0%	
Total Number 4 input LUTs	1,042	3,840	27%	
Number used as logic	1,033			
Number used as a route-thru	9			
Number of bonded IOBs	48	173	27%	
IOB Flip Flops	24			
Number of GCLKs	1	8	12%	
Total equivalent gate count for design	9,180			
Additional JTAG gate count for IOBs	2,304			

Fig 11: Device utilization summary of 5/3 wavelets

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	272	3,840	7%	
Number of 4 input LUTs	553	3,840	14%	
Logic Distribution				
Number of occupied Slices	343	1,920	17%	
Number of Slices containing only related logic	343	343	100%	
Number of Slices containing unrelated logic	0	343	0%	
Total Number 4 input LUTs	647	3,840	16%	
Number used as logic	553			
Number used as a route-thru	94			
Number of bonded IOBs	26	173	15%	
Number of GCLKs	1	8	12%	
Total equivalent gate count for design	6,704			
Additional JTAG gate count for IOBs	1,248			

Fig 12: Device utilization summary of 5/3 wavelets

COMPARISON CHART



VI. CONCLUSION

In this work a flexible VLSI architecture for the implementation of multi-level decomposition DWT (2D) by 5/3 filter and 9/7 filters was proposed. A VHDL based methodology has been used for memory efficient design. The results of the synthesis on a Xilinx show a working frequency of 108 MHz allowing the processing of images sized 64x64 pixels. Therefore, implemented architecture has fast computing time and low control complexity. Our works can be adopted for the next generation image and video compression using multilevel decomposition DWT. In Future, this architecture could be implemented in FPGA. It will be also possible to provide multilevel decomposition for 3D-DWT.

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