# Design, Implementation and Characterization of 45nm Standard Cell Library for Industrial Synthesis Flow

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*Abstract*— **The purpose of this paper is to illustrate design a High Density Standard Cell Library with maximum performance attainable in 45nm technology. The intent was to generate a comprehensive library containing core number of necessary combinational and sequential cells, providing detailed layout and transistor-level schematic views of every cell, with characterization under the 45nm process, in order to utilize them as a fully synthesizable library. The library is designed using Cadence.**

*Keywords*—*Standard cell library, 45nm process, layout design, characterization*

## I. INTRODUCTION

The key success factor for the rapid growth of the integrated system is the use of ASIC library for various system functions. It consists of predesigned and preverified logic blocks that help designers to shorten product development time and manage the complexity of a chip having millions of logic gates or more. Standard cell library contains a collection of components that are standardized at the logic or functional level. It consists of cells or macrocells based on the unique layout that designers use to implement the function of their

ASIC.[6] The economic and efficient accomplishment of an ASIC design depends heavily upon the choice of the library. Therefore it is important to build library that full fills the design requirement. This paper will mainly focus on High Density Based Standard cell Library which implies that we mainly concentrate on minimizing the area of every particular standard cell. Reducing the size of each and every Standard cell block will help the Placement and Routing team to reduce the size of every logic block they use in an Integrated Chip, in turn reducing the size of the whole Integrated Chip. We use certain methods to reduce the area with minimum change in performance, which include the following of the Basic Digital Design Flow, Standard Cell

Design Flow and some layout drawing techniques which will be elaborated in the paper. Once the standard cell is completed they are characterized to verify if each standard cell gives the performance it is supposed to give. If not, then the Designer improves the Floor planning such that the standard cell satisfies the performance requirements under the minimized area

## II. DIGITAL DESIGN FLOW

The technology independent, register transfer level description is the usual input of industrially compatible automated digital implementation flows. The mapping of the RTL description into the technology dependent format, namely the gate level synthesis process, is performed based on a library of pre-characterized CMOS logic gates known as standard Cells. These cells are organized in libraries which minimally include an inverter, a NAND and NOR gate, as well as a multiplexer in tri-state buffer. These are most necessary ones, as they can be basis for the implementation of more complex circuit.

The gate-level synthesis stage is divided into two steps. First, the RTL description is mapped to a technology independent net-list of abstract gates. This is an intermediate representation followed by the final technology-aware mapping to the cells of the library used in the synthesis. After this mapping step the synthesizer optimizes the design, Considering the timing, area and power constraints given by the designer, as long as the available cells of the library. Therefore, the synthesis tools should be aware of the cells timing, area and power characteristics. Hence, the standard cells should have been already characterized in terms of performance, area and power dissipation, to enable the synthesis tool's optimization.

Characterization implies that the transistor-level net-lists of these cells should be fed to an analog simulator with various input slews and output load capacitances, as well as

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the operating conditions of voltage and temperature, and simulated. The result of this process is the timing, power and area characteristics for each library's cell, at the specific design corner and operating conditions. These metrics are written in a different file format adopted by different tools. (Generally written in a LIB file) The LIB file is also used at the physical implementation stage, which follows synthesis. At this stage, the place-and-route tools should be aware of the geometry of cells and interconnects, as well as of design rules like the minimum inter-metal spacing, given the technology.
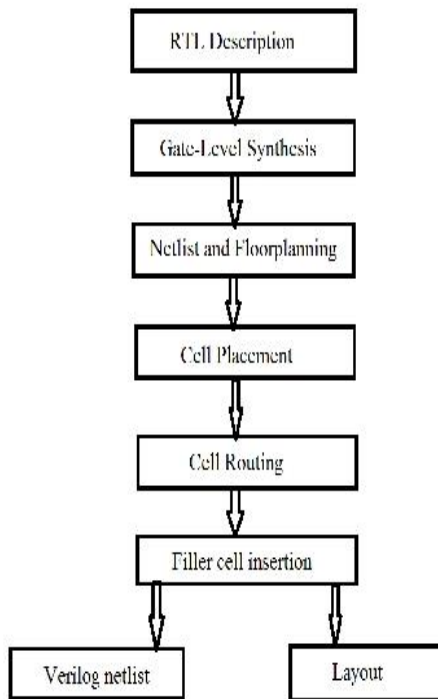


Fig. 1.   RTL to Layout digital design flow

This information is extracted from the physical design (layout) of cells. The place-and-route tools need information about the width and height of cells, as well as the location and the dimensions of their input and output pins. The cell layouts are driven to the Abstract Generator, which produces the Library Exchange Format (LEF) file, which contains this information. In addition to the above, LEF files provide information about the technology's metal stack and the minimum width, spacing and thickness of the available layers. The successful completion of placement and routing is followed by the post-layout simulation step, which verifies the design's functionality. This step requires the information about the functionality of standard-cells, comprising the post layout net-list. This information is produced at the characterization and it is written to a Verilog file, which includes the gate level net-list of each cell, along with the input-to output delay of each path. In the RTL-to-GDSII flow of Fig. 1, the LIB is used for timing and power analysis at both the post-synthesis and the post-layout steps. The information in the LEF file determines placement and routing, by providing the cell and interconnects physical dimensions and the design rules regarding wires and VIAS these two files comprise the core of a standard-cell library. A standard-cell library generation suite should minimally produce both of them, along with the gate-level net-list of

cells, which is given usually in Verilog and it is required for the post-synthesis and the post-layout simulation of designs built with the specific standard-cell library.

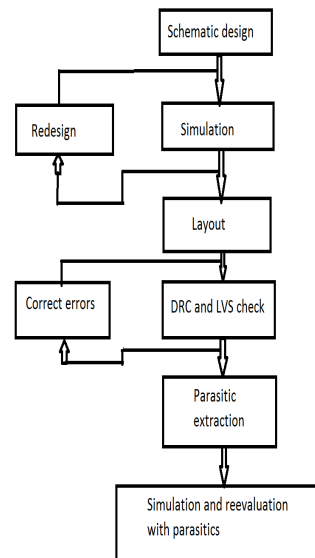## III.   STANDARD CELL DESIGN FLOW

*A). Schematic Design*



Fig. 2.   The flow chart for standard cell design

The Figure.2 shows the design flow for the standard cell. The design starts with the circuit topology of the cell either using schematic or net Wn and PMOS Wp, of the transistor are optimized. Wp and Wn are selected to meet design specifications such as power dissipation, propagation delay, noise immunity and area. The value of Wp and Wn are determined by:

- DC switching point, which is approximately 50% of the VDD.

- Driving capability of the cell, i.e. the number of fan-out that the cell approximately same rise and fall time, Wp is normally three times w simulator is used to determine the switching point

## IV.  LAYOUT METHDOLOGY

If the circuit functions as expected, the physical design for the cell will be created and the parasitic value such as capacitance is back annotated to obtain the actual delay associated with the interconnect. The layout uses the standard cell technique, where signals are routed in poly-silicon perpendicular to the power. This approach result in a dense layout for CMOS gates, as the vertical poly-silicon wire can serve as the input to both the NMOS and PMOS transistor. The row of NMOS and PMOS transistor is separated by a distance specified in the design rule separation between n and p active area. Power and ground busses traverse the cell at the top and bottom respectively. The internal area of the cell is used for routing the MOSFET of specific gates. To complete the logic gate, connections is made in metal, we have used only metal-1 for routing, so this helps the "place and route" tool to use metals with lower resistance for routing, where

metal-1 routed horizontally and metal-2 vertically, this process continues. We use minimum number of poly jumpers as it increases the resistance of the circuit in turn reducing the performance of the standard cell. Reducing the number of poly jumpers helps in maintaining the required performance while designing High Density Standard Cell Library.
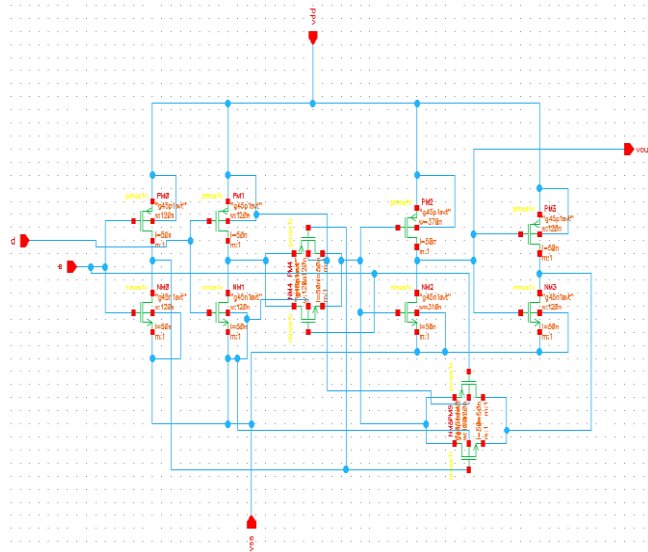

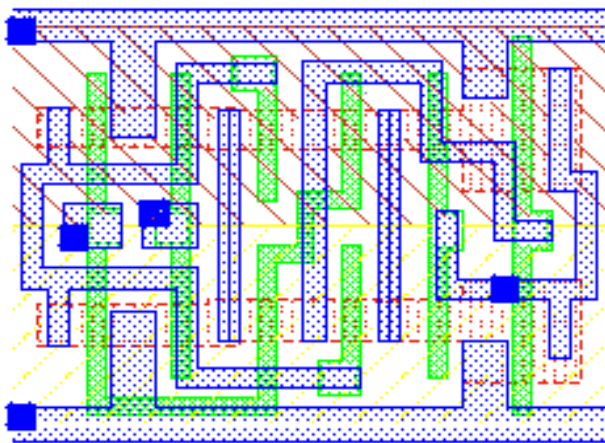
Fig. 3.  Schematic of D-LATCH



Fig. 4.  Layout of D-LATCH

The above Figure shows the layout of D-LATCH, which is implemented using the Standard Cell Design Flow as explained previously. The layout methodology is used here to reduce the area required to implement a Sequential Logic i.e. D-LATCH with the standard height of 1.2µm and area of 2.016µmsq. We can observe that the layout is implemented without any diffusion breaks in turn implies that the area of the Standard Cell is minimized.

## V.  CHARACTERIZATION PROCESS

The cells are simulated to ensure proper functionality and timing. The results from the initial design and extracted values are compared. There are many models which we can use to simulate the nominal process from the fabrication. Measurements of all delay times are at 50% to 50% VDD values. All rise/fall times are 20% to 80% VDD values. To obtain realistic manufacturing process characteristic, circuit simulation is performed with temperature, voltage and process parameter over the range of values that are expected to occur. The critical values at process corner are simulated with minimum and maximum condition. To exercise all input-to-output paths through the cells, input stimulus will be provided to the circuit simulator. Since many repetitive executions of the circuit simulator are required for each cell, the characterization is done using an automatic cell characterization tool.  The characterization flow for std. cell is a major issue. The major steps are given below

### A.  Net-list Extraction

In this, the layout for the cell to be characterized is made using any good layout editor for a specific technology & then verified for the technology rules violations & interconnections. After verifying the design, the parasitic extraction is done in which resistance; capacitance & other physical parasitic are being extracted from the design.

### B.  Specification of Parameters

After the extraction, some default, process & design dependent parameters are defined. For example, doping density, voltage, temperature, Fan out etc.

### C.  Model Selection and Specification

After specifying the parameter values, different models are selected depending on their accuracy, complexity & requirement. A Model estimates the timing, area, power & noise parameters of the std. cell. In real sense, Models are mathematical equations used to calculate the output parameters.

### D.  Measurement

The output provided by the simulator is then measured to extract the required characterization parameters. The output may be in different forms e.g. graphical view, bar chart and plot etc. From these characteristics, different parameters like area, power and timing are calculated for the std. cell.

### E.  Model Generation

Using these parameters, a characterized output model for the std. cell is prepared in a format to which a design tool can understand. All the measured parameters are attached to std. cell.

### F.  Verification

After the characterization of the std. cell, it is verified for different parameters by building a design from it. If it gives the desired result then the library is sign out. But if there is any error then flow is repeated from different stages depending on the severity of the error.

TABLE I.        INVERTER PIN CAPACITANCE

| Inverter Type | C_fall | C_rice |
|---|---|---|
| Inverter_ss | 1.70528e-16 | -1.74423e-16 |
| Inverter_tt | 1.97833e-16 | -2.03708e-16 |
| Inverter_ff | 2.26544e-16 | -2.33695e-16 |

TABLE II.        INVERTER PROPAGATION DELAY

| Inverter Type | -125$\overset{\circ}{}$C | 25$\overset{\circ}{}$C | 125$\overset{\circ}{}$C |
|---|---|---|---|
| Inverter_ss | 6.24785e-11 | 7.78714e-11 | 9.08241e-11 |
| Inverter_tt | 3.51039e-11 | 4.40624e-11 | 5.07018e-11 |
| Inverter_ff | 1.8968e-11 | 2.81106e-11 | 3.4749e-11 |

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## VI. MODEL DEVELOPMENT AND DOCUMENTATION

Before you begin to format your After characterizing, the cells functional description and timing data are transformed to the format required by a specific design tools. Most design tools utilize special-purpose model formats with syntax for explicitly describing propagation delays, timing checks, and other aspects of cell behavior that are required by the tool. The final requirement is a documentation that summaries the functionality and timing of each cell. The functionality is frequently described with truth table, and timing data is presented in a simple format in the datasheet. The documentation for each library contains:

- Setup and hold times
- Minimum cycle time, enable and disable time
- Truth table for small/medium complexity cells
- Operating range of temperature and voltage
- Fan-in and fan-out
- Variation of timing due to temperature and
- Voltage
- Path delays
- Library cell symbol
- Timing diagrams.

## VII. CONCLUSION

In this ever growing world of technology, we expect the size of the systems to be reduced. For this to be possible the Integrated Chips used inside the systems have to be minimized in area. By designing a High Density Standard Cell Library we are providing the Physical Design Department with Standard Cells that are of minimum area so that they can use the pre designed and verified Standard Cells in there project. By using such cells from High Density Standard Cell Library, the total area of the Integrated Chip is minimized.

## VIII. FUTURE WORK

These Standard Cell Blocks can be used in more complex Digital and Analog Design's in Integrated Circuit's and these Standard Cells can be upgraded into lower technologies such as 28nm, 14nm….etc. As our library being open source library the standard cells can be modified to minimize area and operate at optimum performance with minimum leakage and minimum power consumption

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