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Design Approach for a FPGA based Ethernet Bridge for Optical Fiber Communication System

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***Abstract*— The transmission and reception of information such as the data from a sensor, data in form of images, text, voice and videos on Field Programmable Gate Arrays (FPGAs) over ethernet through a coaxial cable, involves attenuation and distortion of signals at certain speed. Since conventional FPGAs do not have an optical fiber interface port, an external optical interface circuits are needed to establish fiber optic communication links between two conventional FPGA's to have a secured and fast communication link. The main aim of this paper is to present an approach to establish optical fiber communication by employing the standard IEEE 802.3 Ethernet and Optical Sensing circuits that can be implemented on an FPGA. The Ethernet MAC transmitter and Receiver modules are designed in Verilog using Xilinx Vivado and verified for the functionality on Xilinx Nexys 4 board. The Optical Sensing Circuits are designed and simulation is done on Multisim and functionalities are verified. The Optical Driver and the Optical Detector circuits are made to operate in Mega Hertz range for a Fast Ethernet (referred as 100Base-T) that enables transmission of data over 100 Megabits per second on Local Area Network (LAN).**

Keywords—FPGA, RTL Design, Optical Sensing Circuit, Ethernet;

I. INTRODUCTION

In telecommunications, fiber optics is one of the major building blocks due to its high bandwidth capabilities and low attenuation, hence making it ideal for the gigabit and beyond gigabit communications [1]. Industry 4.0 refers to industrial development [2] that brings high speed and better efficiency in industrial development process through factory automation. Ethernet is a technology used to connect a number of computers, printers and routers to form a local area network. Industrial Ethernet (IE) is the use of ethernet in industrial environment which helps the devices to communicate in a quicker way by giving the users a better connectivity and transparency through a special connectors and cables.

In industries, huge amount of data is collected, transported and analyzed that required higher bandwidth interconnection between sensors, machines, computers, facilities, data centers and people. The ethernet communication between devices in an industry are dominated by copper connections, where fast ethernet could provide data transfer rates of 100 megabits per second (referred as 100Base-T) and gigabit ethernet provide a data transfer rate of one gigabit per second (referred as 1000Base-T). When the speeds elevated beyond gigabit, the distance between the devices spans from meters to kilometers. The conventional ethernet apparatus cannot support higher data rates at this link distances. The optical fiber communication systems in industries have drawn considerable attentions of the researchers and low cost ethernet topologies are promising in industrial application for the conventional devices with ethernet.

The present work proposes an approach for optical fiber communications between two FPGA, the design implemented on FPGA utilises the standard IEEE 802.3 Ethernet Protocol [3, 4] to complete Ethernet MAC design. A high-speed Integrated circuit has been proposed in order to establish the optical sensing circuits for optical transmission and reception interfaces. Design consist of an RTL for Transmitter and Receiver MAC units, which are simulated for generation of output sequence for a set of data inputs.

II. RELATED WORK

In real time system with ethernet networks, timing and synchronization are the key parameters for the network stability for a system. Ethernet is classified as LAN (Local Area Network) which has the transmission length of up to 100 meters. For packet transmission from Ethernet to Synchronous Optical Network (SONET) with packet format and to have increased transmission rate, a "Two-port to Two-port" synchronized topology is used between an ethernet module and RS485 module. Reduced Gigabit Media Independent Interface (RGMII) is used independently to supply a communication network for Media Access Control (MAC) and Physical (PHY) layers, in which the transmit module will allocates client data from RS485 module to ethernet port module. The client data such as Internet Protocol (IP) length, User Datagram Protocol (UDP) data length and UDP checksum are transmitted from First in First out (FIFO). Simultaneous control signal is sent to the destination ethernet port, where the transmitted packets are

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received by means of ethernet port module into the specified RS485 module. The client data are managed in RS485 module that operated on UDP protocol and verification is done on DE2 development board where the design is operated with baud rate of 115200 Hz [5]. Currently communication between the industrial smart sensor systems and the users are established using an individual optical fiber cable that is uneconomical. This work exploits the approach to send multiplexed data over an optical fiber, where the information data is carried over a 5 km optical fiber cable through a communication module composed of an ethernet interconnection. RGMII is used in order to supply a communication network for MAC and PHY layers, where the parallel client data are sent to RS485 interface with 8-bit serial data produced at the ethernet where the transmission happens with 4-bit nibble data. The receiver takes in 4-bit nibble data and reformates it into the ethernet packet format at the ethernet module and stores them in a memory. The operating frequency, the RS485 and ethernet rate of data transfer are found to be 125 MHz, 115200 bps and 1 Gbps, respectively with data volume of 8-bits, a RAM of 2k bytes and FIFO of 1k bytes [6].

Universal Serial Bus (USB) which is an usual interface for data transmission for PC and peripheral devices and has become a mainstream for computer data transmission interface. The work exploits the design of an Application Specific Integrated Circuit (ASIC) serial interface engine that constructs a packet with serial data and integrates with external USB PHY chip. The data to be transmitted are queued with FIFO memory preceding with serial interface engine that transmits data serially with the USB packet format and later converting it into analog differential signal using cypress's USB PHY chip [7]. PCI Express is the high performance Input-Output (I/O) bus used to interconnect peripheral devices in applications such as computing and communication platform. The work exploits the implementation of PCI express protocol that connects to the physical link on one side and the data link on the other side. Eventually the packets on the data link layer are converted into serial bit and clocked out at 2.5 Gb/s with the developed scrambler algorithm that encodes and transmits the data. At the receiver side the serial bits are given to serial to parallel converter and the 10b signals are converted back to 8b suing 8b/10b decoder [8].

III. PROPOSED METHOD

The proposed design architecture consists of three parts namely Transmitter, Fiber Media Converter and the Receiver. The proposed architecture for FPGA based Optical Fiber Communication system is shown in Figure 1.

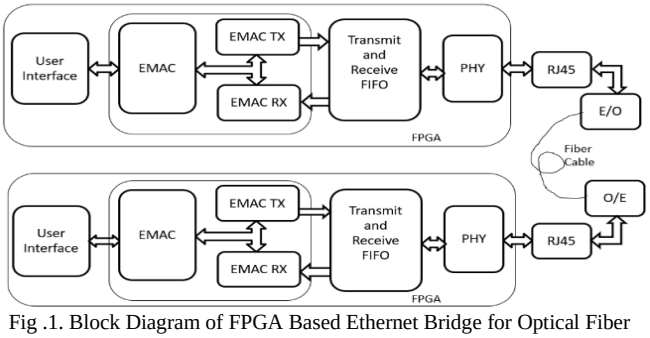

Fig .1. Block Diagram of FPGA Based Ethernet Bridge for Optical Fiber Communication.

In architecture shown in Figure 1, two FPGA's with ethernet transceivers are connected to a fiber media converter in order to establish fiber optic links for the conventional FPGA with ethernet. The data intended to be transmitted by user interface are stored in FIFO memory. Data from FIFO is read at each clock cycles and is sent to the Cyclic Redundancy Check (CRC) block [9] as well as the state machine of the ethernet MAC transmitter module to perform ethernet packet framing and transmit data serially to the PHY layer. The transmitter module is shown in Figure 2 and the transmitter state machine is shown in Figure 3.

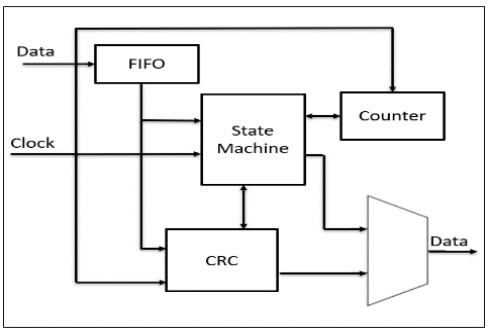

Fig .2. RTL Diagram of Transmitter Module.

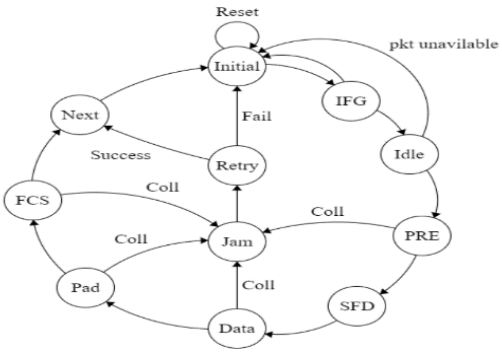

Fig .3. Transmitter Block Finite State Machine.

The received information on the FPGA physical layer over ethernet by a receive state machine. Frame Check Sequence) FCS is verified for the residue of CRC check. The data which are successfully retrieved are stored in a receive FIFO and if the received data is valid, then status signals "ok" is asserted, else status "error" is asserted indicating an error has occurred during the receiving process. The receiver module is shown in Figure 4 and the receiver state machine is shown in Figure 5.

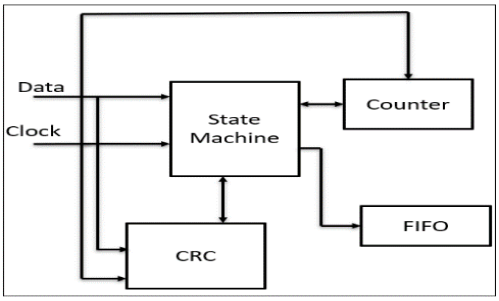

Fig .4. RTL Diagram of Receiver Modul

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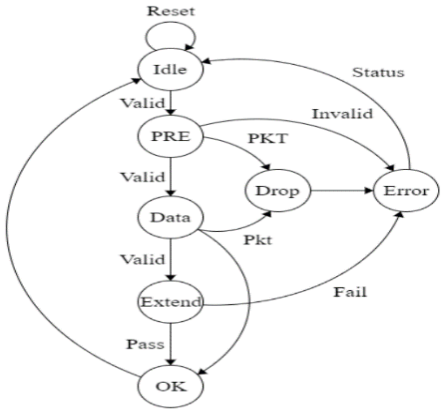

Fig .5. Receiver Block Finite State Machine.

The user data intended to be sent and received over optical fiber cables are transported over a coaxial cable with RJ45 connector and is fed to Fiber media converter, which converts the electrical signal into optical format. Optical signal is converted back to electrical domain with the detectors that performs photoelectric conversions.

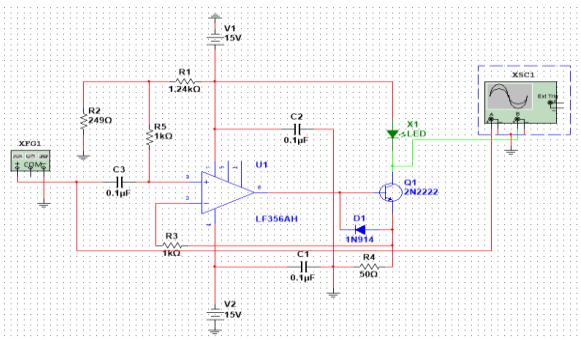

Fig .6. Fiber Optic Driver Circuit.

The optical fiber driver circuitry is shown in Figure 6, which includes a light source where the intensity of the light beam is directly controlled by current depending upon the electrical input signal. This driver circuit is made to operate in megahertz region with the light source biased at 30 mA current and the inputs to the driver are capacitor coupled for the input range of 0V to 5V. The LF356 JFET input operational amplifier has an extremely fast setting time, high slew rate, wide bandwidth with lower current losses makes it excellent for low noise applications.

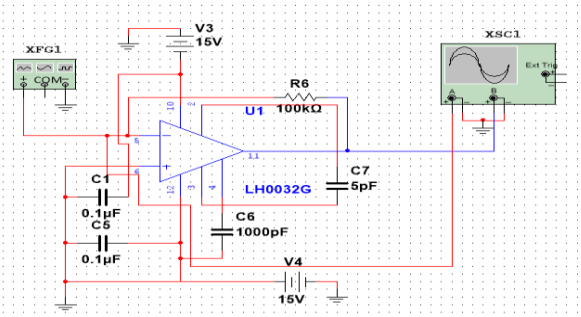

Fig .7. Fiber Optic Detector Circuit.

The receiver circuit is shown in Figure 7, contains a high-speed photo detector HP5082-4220 PIN photo diode that is capable of operating at higher frequencies. When the high frequency light hits the photodiode some proportional amount of current readings is generated which is then converted back into voltage reading with the help of a transimpedance amplifier. Here, LH0032 is an ultra-fast input operational amplifier and is suitable for diverse application at several megahertz.

IV. RESULT

The design has been divided into two sections. The Ethernet MAC implementation and the Fiber sensing circuit implementation.

The implementation of Ethernet MAC transmitter and receiver modules are done using Xilinx Vivado. The simulation of the developed design is performed and verified for its functional operation.

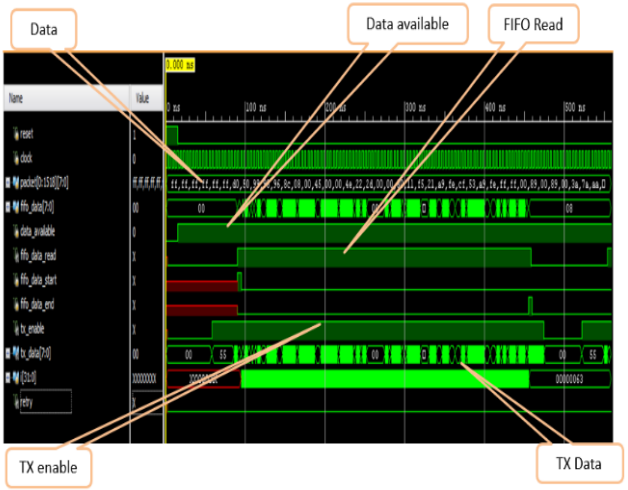

Fig .8. Ethernet MAC Transmission Module Simulation.

Figure 8 shows the Ethernet MAC transmission module simulation waveform. When the data (e.g. Hexadecimal values) is ready to be transmitted, then the “data_available” signal is asserted. Once “fifo_data_read” is enabled, then the data are read from the file and is stored in a FIFO. During the data read process “fifo_data_read” is asserted in order to store information in a memory and once the memory gets filled up the “fifo_data_end” signal is asserted. When “tx_enable” is enabled, preamble and start of frame delimiter are transmitted initially and later follows the data that is stored in the memory. In the meantime, data is also passed through the CRC generator, where a 32-bit frame check sequence is generated and is appended at the end of the data field to be transmitted.

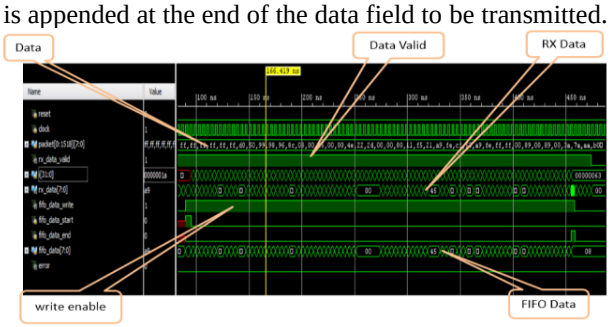

Fig .9. Ethernet MAC Receiver Module Simulation.

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Figure 9 shows the Ethernet MAC receiver module simulation waveform. When the "data-valid" signal is asserted, the receiver module starts responding to the channel and at each clock cycles the sampling of the received data frame is done. Along with the sampling of the received data bits, the information is also checked with the CRC residue in order to make the data to be valid. If the data is valid, then the "data-valid" signal is asserted, and if the sampled data values are proper then the receiver waits until the "fifo_data_write" signal is enabled. Once the write signal is asserted the information received are stored in a FIFO. During the data write process "fifo_data_read" is asserted and once data starts to occupy the memory the "fifo_data_start" signal is asserted, later if the memory gets occupied completely and all the frames are stored then the "fifo_data_end" is asserted indicating that the memory is full.

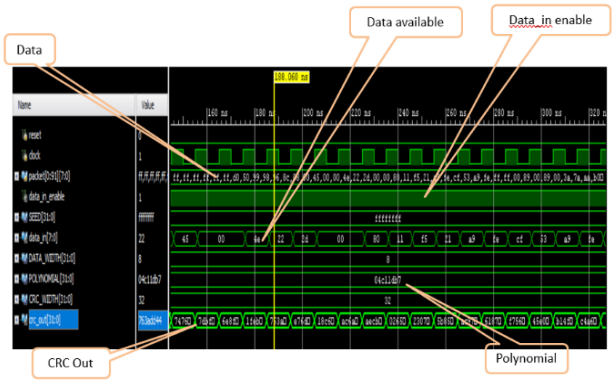

Fig .10. Cyclic Redundancy Check Module Simulation.

Figure 10 shows the Cyclic Redundancy Check module simulation. During each clock cycles, the data from a text file (e.g. Hexadecimal values) is fed as an input to the CRC generator, which takes 8 bits as an input whenever the "data_in_enable" is asserted. Since, Frame Check Sequence (FCS) information is transmitted and presented at the MAC sublayer in a reverse bit order, the input data bits are complemented by loading a value of 32'hffffffff as per the IEEE standard. Within the CRC calculation phase the data under goes many xor operation between registers. Depending upon the generating polynomial of 0x04c11bd7 the "crc_out" contains a bit reversed and complemented MSB of a 32-bit FCS sequence.

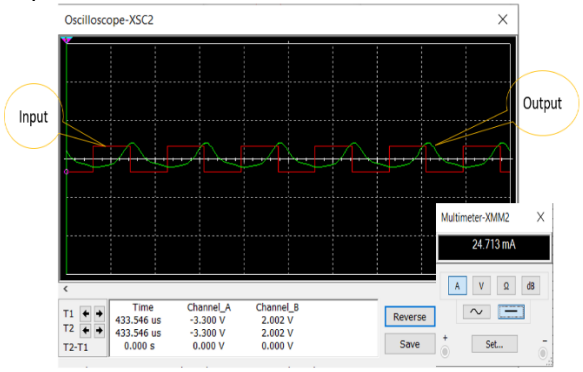

Fig .11. Fiber Optic Driver Circuit Simulation.

The circuit simulation of the laser driver circuit is shown in Figure 11. The electrical pulses coming from the FPGA is fed to the capacitor coupled input of the circuit and depending upon the electrical signal, the laser produces the optical pulses and transmits the pulses through a fiber cable. In order to verify the circuit functionality, the driver circuit is fed with a square pulse of 50% duty cycle at 5 MHz. LF356 which is a high-speed amplifier drives the LED optical source at 25mA and converts the electrical information into optical pulses.

Fig .12. Fiber Optic Detector Circuit Simulation.

The circuit simulation of the detector circuit is shown in Figure 12. Here the output from the driver circuit is fed as the input to the detector. The LF356 IC, which is a high-speed amplifier drives the optical source at 25mA and the output of the driver circuit is fed as the input to the detector followed by transimpedance amplifier circuit developed with LH0032 IC. It amplifies the signal level from 2 V to 3.1 V, and fed to FPGA.

V. CONCLUSION

An Optical fiber communication system between two FPGAs is proposed, simulated and verified. Design and simulation analysis of Ethernet MAC Transmitter and Receiver Modules along with the Cyclic Redundancy Check (CRC) is performed for the packet size of 1500 bytes. The transmitter module consumed 0.01 W of power while utilizing 185 LUTs out of 15,850 LUTs with setup time of 5.504 ns and hold time of 0.086 ns. The Receiver module consumed 0.096 W of power while utilizing 119 LUTs out of 15,850 LUTs with setup time of 3.871 ns and hold time of 0.137 ns. Design and simulation of the developed Optical Sensing Circuits with fast amplifier IC's for optical tansmission and reception is performed.

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